

Architectures of Delay Line ADC and Delay Cells for Digital DC-DC Converters

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Abstract—A survey and classification of architectures is presented in this paper for delay line ADC and its delay cells targeting digital control of DC-DC converters. Previously presented designs are identified as particular cases of the proposed classification. In order to optimize occupied area and power consumption, a general architecture is designed, which includes one delay line and thermometer-decode. And a particular example of the delay line ADC is described. The ADC operates at 4 MHz switching frequency and has low power consumption and small area. Experimental results verify the functionality of the designed delay line ADC.

Keywords-delay line; delay cells; ADC

I. INTRODUCTION

Digital controllers for DC-DC converters with high performance are feasible. Based on custom architectures and microelectronic realizations of the key blocks, including digital pulse-width modulators, A/D converters and compensator schemes, the advantages, such as lower sensitivity to parameter variations, programmability and so on, can be offered by these controllers. The ADC block plays a very important role in the digital control ICs. The research on ADC has been a major topic of academia and industry. In the last century $\Sigma\Delta$ ADC was suggested and developed. Later in the 1970s, SAR ADC was proposed. But the bandwidth is their weakness. In 1987, PR Gray and his students from UC Berkeley were successful in CMOS technology to achieve a pipe line structure of the ADC. However, its shortcoming is the poor robustness. Though FAI ADC and TI ADC have high speed, they can only achieve very low precision. In 2003, J. Patella proposed a delay line ADC. From then on, delay line ADC began to receive widespread attention. Scholars and engineers do much research on the delay line ADC. A variety of structures have been proposed. Therefore, it's necessary to do a survey and classification. This paper presents a summary of the ADC delay line and delay cells, which are published.

Section II presents the principle of voltage-to-delay-to-digital ADC which is the base of delay line ADC. Section III reviews the architectures of delay line ADC and delay cells. An ADC is designed and simulation result is given in Section IV. The last section gives the conclusion.

II. VOLTAGE TO DELAY TO DIGITAL ADC

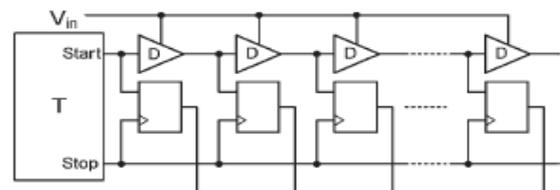


Figure 1. Illustration of voltage-to-delay-to-digital ADC

As shown in Figure 1, the input voltage modulates the delay per cell by $D(V_{in})$. The signal passes through $NQ(V_{in}) = (T/D(V_{in}))$ delay cells in T seconds, where the integer part of x is cared about. $NQ(V_{in})$ ranges from $N(V_a)$ to $N(V_b)$, and $D(V_{in})$ is generally monotone in the range of interest $[V_a, V_b]$. From these, we can depict the number of bits as the equation:

$$R \approx \log_2 T |V_a - V_b| \cdot \left| \frac{1}{D^2(V)} \frac{dD(V)}{dV} \right|_{V=V^*} \quad (1)$$

Where V^* is a constant in $[V_a, V_b]$. Equation (1) shows that to achieve a high resolution, a delay block which is sensitive to the control voltage should have a small delay. More importantly, (1) reveals the basic tradeoff between time and resolution. That is to say, at the cost of a larger time interval T , we can increase the number of bits R for a few kinds of amplification in the time domain. When the resolution becomes the primary concern, for example the weak-signal acquisition, this feature is useful. At the same time, the sampling rate becomes relatively low. In terms of linearity, it is desirable to have delay cells with $D(V_{in}) = (D_0/(V_{in}+V_0))$, in which D_0 and V_0 keep constants. However, it is obvious that we can approximate this relation in a quite small range. For this situation, another tradeoff between linearity and speed becomes much more important: As revealed by (1), the time interval T is required to be small for high conversion speed, while the dynamic range $|V_a-V_b|$ should be small for good linearity.

III. REVIEW THE ARCHITECTURES OF DELAY LINE ADC AND DELAY CELLS

Delay line ADC is a kind of voltage-to-delay-to-digital ADC. And Figure 2 is the basic delay-line ADC configuration. The configuration is very similar with Figure 1. Analog input is converted into delay time of test signal by the delay line. And the sample signal samples the signals

t1...t8. Encoder handles the signals got by sampling and output digital signal e. Analog input decides the delay time of delay cell, and then the A/D converter is achieved. Based on this configuration, much research and study is presented. The conventional delay cell is showed in Figure 3. It consists of a complementary CMOS input stage and a inverter output stage. If the reset signal is necessary, the pmos which is close to supply can be the port of the reset signal and the other one still is the port of IN signal.

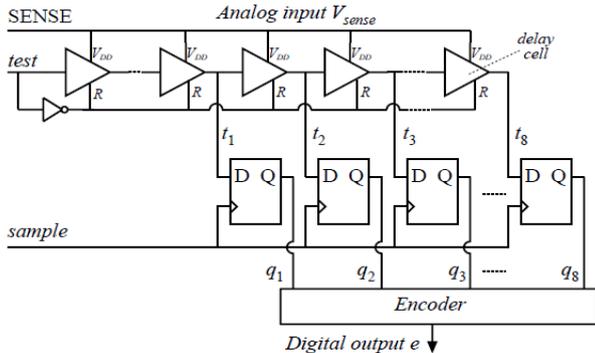


Figure 2. Basic delay line ADC configuration

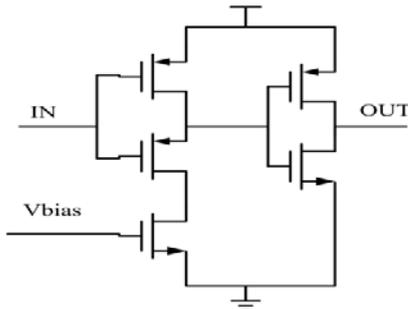


Figure 3. conventional delay cell

A. Architectures of delay line ADC

Reviewing much research, we find delay line ADC has two primary architectures. One showed in Figure 4 has a delay line. In Figure 4 left, the reference and input signals are sent in comparators to get two clock signals. One is for going through the delay line, and the other is for acting as sample signal. In Fig.4 right, the reference and input signals are selected into the delay line.

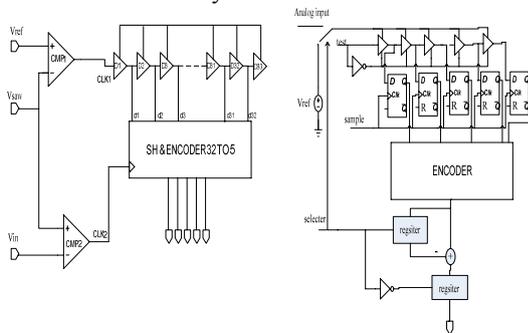


Figure 4. ADC with one delay line

The other architecture showed in Figure 5 has two delay lines, measure line and reference delay line. The input voltage is first converted to a current to decide the delay time. The measure line and the reference line are composed of a chain of these delay cells. The inputs of these delay chains are connected to a clock signal. The reference voltage V_{ref} , is designed to be at a fixed value, hence the time it takes for the clock pulse to propagate to the last delay cell in the reference line is fixed. When the pulse reaches the last delay cell in the reference line, all the latches are triggered to determine the location of the clock pulse in the measure line. Since the propagation time of the pulse in the measure line varies with the input voltage V_{in} , it can be determined by the reading of these latches. The readings are then converted into output using a thermometer decoder.

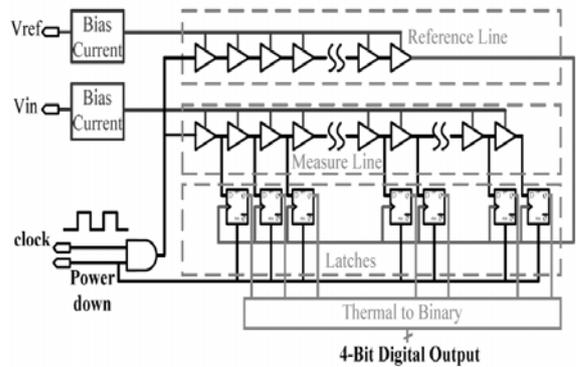


Figure 5. ADC with two delay lines

However, to eliminate process, temperature variation that affects propagation delay, the both architectures always has digital calibration.

Some improvements are presented based on the two architectures. A power down signal is used to stop the delay line work to reduce the power consumption [1]. Differential structure is employed, the measure and reference lines become the fast and slow lines composed by P cells and N cells [2]. Tap selectors replace the decoder [3]. A programmable architecture is proposed [4]. Every improvement is for the specific application. A interleaved N-block and P-block forming voltage-controlled variable-delay transmission line is adopted [5].

B. Structures of the delay cells

The most major point is the structure of the delay cell. A small change is showed in Figure 6 (a) compared with the conventional one. A capacitance is inserted in the normal structure. The delay time can be bigger by this. And a gate capacitance can also be used to achieve the capacitance.

Then a slow current starved delay cell in Figure 6 (b) is applied. It has a complementary CMOS input, a dummy transistor, a transmission gate and a starved current inverter output. When the cell is triggered and induces the current through controlled current sources M1 and simple current mirror transistor, transistor M3 resets the cell, and transistor M2 operates as a NMOS inverter. Not only the equivalent capacitance C_{eq} but also the transmission gate (M4, M5) and dummy transistor M6 decide the propagation delay of

this cell. Biasing voltages V_p , V_n and V_c can control the resistivity and capacity of the transmission gate and dummy transistor.

A subsequently proposed architecture is showed in Figure 6 (c). It only needs a INVERTER and a NOR. The structure is suit to standard cells

A programmable delay cell is designed in Figure 6 (d). Enabling/disabling differently-sized transistors $Q1_a$ to $Q1_d$ can digitally program the discharge current and make it much smaller. The discharge current is set to fixed value by the 2b binary delay control input.

To achieve interleaved transmission line, N-block and P-block is designed for delay cell in Figure 6 (e). Different from the other delay line architectures changing the delay by varying power supply, this design a PMOS and NMOS current starved interleaved method is introduced in this one, which produces enough linearity. The sampled signal is used to "CONTROL" pin.

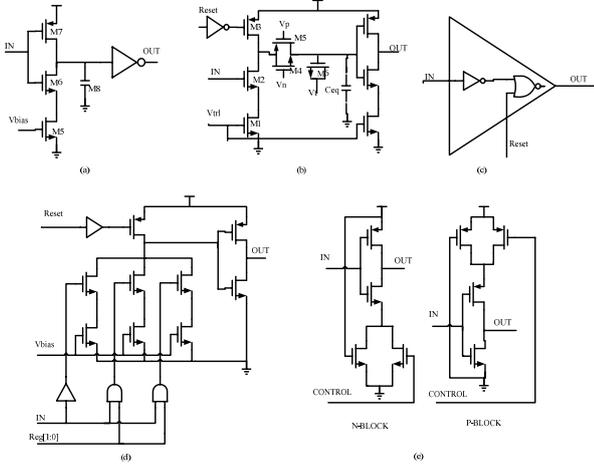


Figure 6. delay cells

IV. IC IMPLEMENT OF ADC AND SIMULATION RESULT

The architecture of the designed ADC in Figure 7, whose LSB is 3mV, voltage sensing range is 1.352V to 1.448V, sampling frequency is 4Mhz, has a delay line comprised current control delay cells. The delay cells are susceptible to supply voltage, process and temperature, which results in that the delay time of the delay cell changes dramatically in different working conditions and the total delay changes larger after the accumulation of delay line. The longer the delay line is, more obvious this effect is. So the digital control circuit is indispensable. In the calibration and the quantization process, the digital control logic is to ensure proper operation of the delay line.

In the calibration process, the reference voltages of the comparators CMP1 and CMP2 are V_{REF1} and V_{REF2} , respectively ($V_{REF2} > V_{REF1}$, $V_{REF1} = 1.352V$, $V_{REF2} = 1.448V$). The purpose of the calibration is to keep the right relationship between the clock signal CLK1 and the clock signal CLK2 generated by V_{REF1} and V_{REF2} compared with the saw signal respectively. The fixed delay time is exactly equal to the length of one system clock cycle. At the rising

edge of CLK2, D flip-flops sample the last two delay signals. The judgment and feedback control logic works to adjust the delay time after sampling.

In the quantization process, V_{REF} and V_{IN} are fed into the two comparators and then compared with the saw respectively. CLK1 goes through the delay line and the delay cells pass CLK1 in turn and output d1-d32 signals. According to the value of V_{IN} , the delay between the rising edge of CLK2 and that of CLK1 varies and the signal is different. Then SH & ENCODER module gets the different sampling results from D flip-flops which are controlled by CLK2 and output the codes. Then the quantization is achieved. And the simulation result is showed in Figure 8.

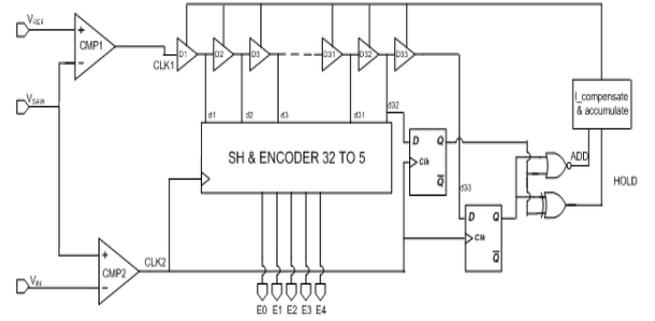


Figure 7. the designed ADC with one delay line

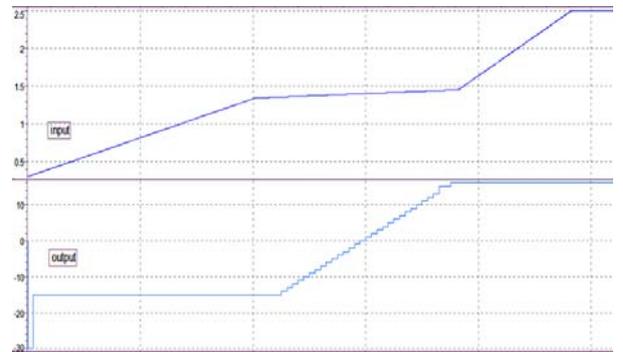


Figure 8. simulation result

V. CONCLUSION

This paper presents a survey and classification of architectures for delay line ADC and its delay cells targeting digital control of switching DC-DC power converters. The classification is based on the numbers of delay lines. It is easy to see that the previously presented designs belong to the proposed classification.

In this paper, an ADC with one delay line is designed. Its LSB is 3mV, voltage sensing range is 1.352V to 1.448V and sampling frequency is 4Mhz. Furthermore, digital calibration module is designed to eliminate process, temperature variation that affects propagation delay. The functionality of the designed delay line ADC is validated by experimental results.

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