Strategy and Implementation of Multi-mode Control in Switch-Mode Power Supply

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***Abstract*-In order to reduce the standby power and increase the efficiency of the SMPS (Switch-Mode Power Supply), a multi-mode control strategy is presented and implemented in this paper. Three different modes are applied in the strategy and the optimization is achieved according to different load. The SMPS can work adaptively in different modes according to variable load. A chip is designed and fabricated on BCD 700 technology and a 12W (12V/1A) laboratory prototype is built in order to verify the proposed strategy. The experimental results have shown that the average efficiency of the proposed SMPS is 84% and the standby power consumption is 90mW, which both meet the requirements of the latest Energy Star specification with margin.**

Keywords-component; standby power, multi-mode, Quasi-Resonant modulation, Energy Star

I. INTRODUCTION

Due to the low cost, universal input, simple structure, and high efficiency, AC/DC is widely used in adaptors, chargers and power units of household appliances such as set top boxes, air-conditioners and so on [1]. Recently, with increasing concerns about environment and energy, more and more attentions are paid to the power efficiency and consumption, especially the standby power consumption. Individual device standby power may seem insignificant, but when it is multiplied by the number of households, the number of devices in a household and the amount of time each spends in standby, the problem adds up quickly. According to Lawrence laboratory, all of the standby power consumption accounts for 1% of the world electricity production [2]. To increase the average efficiency and curtail the standby power consumption of the SMPS, a multi-mode control strategy is presented. The SMPS can work adaptively in QR (Quasi-Resonant) mode, PFM (Pulse Frequency Modulation) mode and PSM (Pulse Skipping Modulation) mode according to variable load. Compared to the conventional PWM (Pulse Width Modulation) mode, the novel strategy can greatly reduce the no-load power consumption and increase the average efficiency which follows the trend of green power technology [3].

II. POWER ANALYSIS OF SMPS

Fig. 1 shows the presented structure of SMPS. The PMIC is the designed chip that integrates the logic control circuit, start-up circuit, current sensing circuit and power FET.

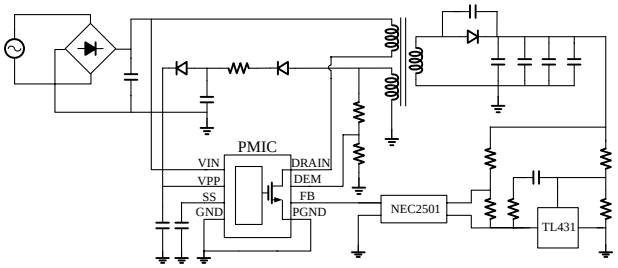

Figure 1. Schematic of SMPS

According to Fig. 1, the overall power consumption contains the switching loss, the charge and discharge loss of the gate of the power FET, the conduction loss of the FET, the control circuit loss and other loss. The switching loss PSW and the charge and discharge loss PCH are as follows:

$$P_{SW} = C \cdot f \cdot V_{DS}^2 \quad (1)$$

$$P_{CH} = V_{GS} \cdot Q_G \cdot f \quad (2)$$

The loss of those two types is dominant of the overall power consumption. To curtail the loss, a multi-mode control strategy is presented. In PFM mode, the switching frequency f decreases as the load becomes lighter. In PSM mode, through skipping some pulse cycles, the power FET doesn't switch during these cycles so the loss is avoided. In QR mode, the power FET is on at the valley of V_{DS} and so the loss P_{SW} is further decreased.

The conduction loss P_{CON} is described as:

$$P_{CON} = D \cdot I^2 \cdot R_{DS(ON)} \quad (3)$$

In (3), D is the duty radio. The loss can be decreased by limiting the conduct current I to a lower value that can meet the minimum power requirement. $R_{DS(ON)}$ is related to the technology we adopt and we can decrease it by increase the area properly.

The control circuit loss P_{CTRL} is:

$$P_{CTRL} = V_{PP} \cdot I_{TOTAL} \quad (4)$$

From (4), we can see that lowering V_{PP} contributes to decreasing the loss. Furthermore, in our design, the chip can work in PSM mode and some circuits shut down to reduce I_{TOTAL}, so the loss is also decreased.

III. PROPOSED MULTI-MODE STRATEGY AND CIRCUIT IMPLEMENTATION

Fig. 2 is the sketch map of multi-mode control. The Y-axis stands for frequency while the X-axis stands for feedback voltage which depends on the load. When the load is heavy, the feedback voltage V_{FB} is high and if $V_{FB}>V_{TH2}$, the system works in QR mode. When the load becoming lighter makes $V_{TH1}<V_{FB}<V_{TH2}$, the system turns into PFM mode. So, it decreases the switching loss and increase the efficiency of the whole system. To avoid the audible noise issue, a PSM mode is applied that the frequency is clamped at a level about 25kHz and the system skips some pulses.

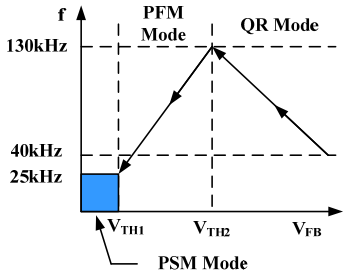

Figure 2. Sketch map of multi-mode control

A. QR mode description

As we know, there is a conduction resistance R_{DS} in the power FET and when the FET is on, it leads to some conduction loss. The bigger the voltage V_{DS} is, the more obvious the loss is. A valley detection circuit is designed to detect the voltage valley of the drain and turns the power FET on at the valley so the conduction loss decreases and the efficiency increases [4]. As demonstrated in Fig. 3 (a), the time to turn on the power FET M_0 is decided by the valley detection circuit I_4.

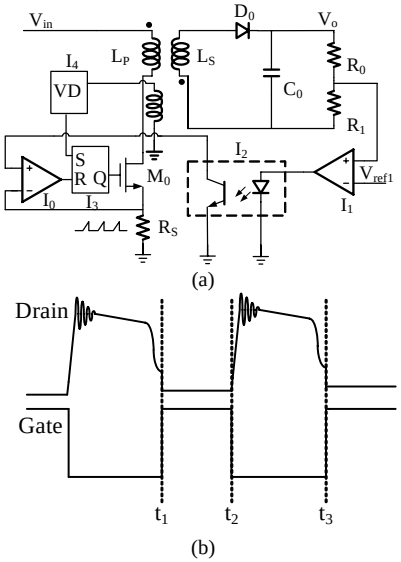

Figure 3. (a)Schematic of QR mode (b)Waveforms of the drain and gate

Fig. 3 (b) is the waveforms of the drain and gate of the power FET. At the time t_1, the valley detection circuit detects the voltage valley of the drain and turns the power FET on, so the conduction loss is much smaller. As the FET is on, the voltage on R_S rises, and when it rises to a threshold at the time t_2, the power FET is turned off and the drain voltage rises. After a while, the drain begins resonating again and a valley is detected to turn the FET on at the time t_3 and the cycle repeats.

B. PFM mode description

In order to solve the problem that the system efficiency is low as the load becomes lighter, the PFM mode is applied. Fig. 4 (a) is the schematic of the PFM mode. In this mode, the on-time of the power FET is fixed and the off-time is variable. The lighter the load is, the longer the off-time is, and so the switching frequency turns lower [5].

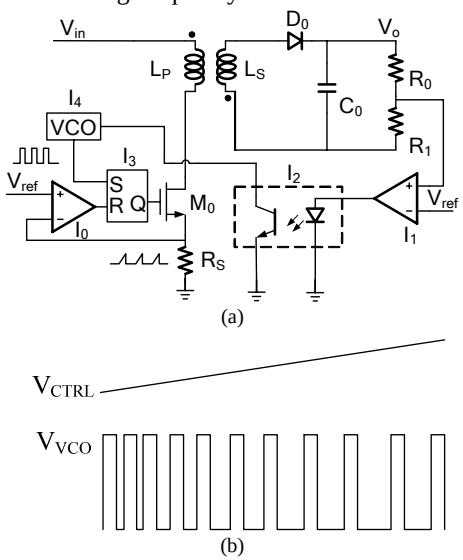

Figure 4. (a)Schematic of PFM mode (b)Control and output of VCO

In Fig. 4 (b), V_{CTRL} is the control signal of the VCO and the V_{VCO} is the output. The detailed working process is described as follows: the change of the output voltage, reflecting in the input of VCO I_4 through comparator I_1 and optic coupler I_2, causes the frequency of the pulse output of VCO to change. When the load is light, V_{CTRL} is high and the frequency is low, and vice versa. The pulse output V_{VCO} turns the power FET M_0 on through RS flip-flop I_3. As M_0 is on, the voltage on R_S increases linearly, the V_{in} constant, the rising slope changeless, and M_0 turns off as soon as the voltage reaches V_{ref}. Because the on-time is fixed, the power transferred from V_{in} to V_o is a fixed value. If V_o rises, the open frequency of M_0 falls, so the power transferred to V_o decreases and V_o falls, otherwise the change reverses.

C. PSM mode description

The PSM mode is generally used to regulate the output voltage under either light- or no-load condition [6]. Before the output voltage falls to a set point, the power FET and

some circuits don't work during many cycles, as a result, the power consumption decreases [7].

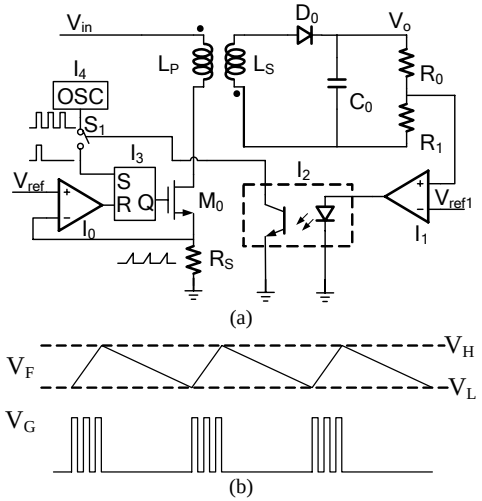

Figure 5. (a)Schematic of PSM mode (b)Feedback and gate driver signal

Fig. 5 (a) is the schematic of PSM mode, and the feedback signal V_F and gate driver signal V_G are depicted in Fig. 5 (b). The detailed working process is described as follows: the pulse signal that turns M_0 on is produced by oscillator I_4 and is in the control of switch S. While V_o decreases, V_F steps down and as soon as it reaches the set point V_L, the switch S is on, resulting in that the pulses produced by I_4 transfer to S port of I_3 and turn M_0 on. The cutoff of M_0 is controlled by the voltage on R_S. After some cycles, the output voltage rises to the target value and V_F reaches the high threshold V_H, then the switch S turns off and the pulses produced by I_4 can't transfer to I_3, so M_0 is off and V_o begins to fall down. Accordingly, the feedback signal steps down, so repeat in cycles.

As the efficiency is different with variable load, we integrate all the three modes within one chip. As a result, the efficiency is optimal in the full range of the variable load and the standby power decreases observably.

IV. MEASUREMENT RESULTS

A. Chip and laboratory prototype

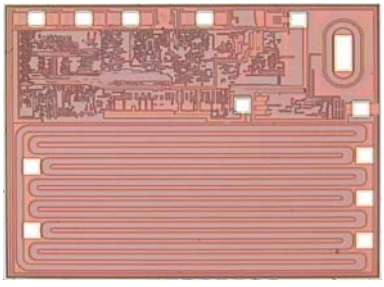

Figure 6. Die photograph of the chip

The proposed multi-mode control circuits are integrated in a chip and the chip is fabricated in the technology of 700V BCD. Fig.6 is the micro photo of the die and the area is about 2.7*2.2mm^2. The chip is encapsulated in the form of DIP-8. As seen in Fig. 7, a laboratory prototype with universal input and 12V/1A output is built with the chip to verify the proposed multi-mode control strategy. The chip is signed in bold white frame in Fig.7.

Figure 7. Laboratory prototype of SMPS with the chip

B. Measurement results and analysis

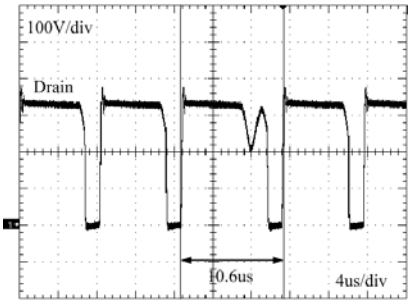

Figure 8. Waveform of drain in QR mode

By connecting a variable load to the output port, we observe the different working modes at different load. From Fig.8 to Fig.10, we can see that the SMPS works in QR, PFM and PSM mode and transmits stably from one mode to another. Fig.8 is the waveform of drain in QR mode, and we can see that the period is 10.6us and the relevant frequency is 94kHz which is in the designed range of 40kHz to 130kHz. Fig.9 is the waveform of drain in PFM mode and the frequency is 88kHz, meeting the range of 25kHz to 130kHz. Fig.10 is the waveform of gate and V_F in PSM mode, and we can see the period is 68ms and the frequency is 15Hz. Such a low frequency ensures the low power consumption in the light- or no-load condition.

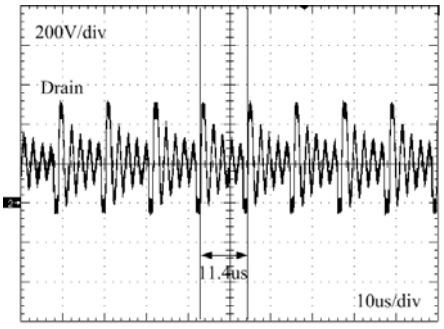

Figure 9. Waveform of drain in PFM mode

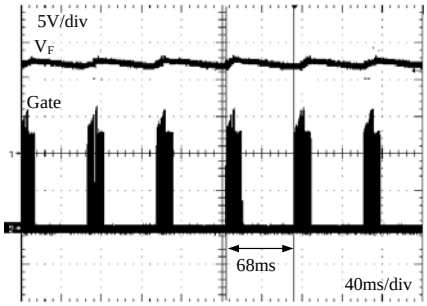

Figure 10. Waveform of gate and V_F in PSM mode

C. Performance comparison

To verify the validity of the proposed strategy, an experiment and test is performed. In the condition of 25%, 50%, 75% and 100% of the rated output power, we measure the efficiency of proposed multi-mode control strategy and conventional PWM control strategy separately. The efficiency curves of different strategies are depicted in Fig. 11 and from it we can see that the proposed strategy can greatly increase the efficiency compared with the conventional strategy especially when the load is light. Conventional strategy uses constant PWM frequency throughout the entire load range, suffering from poor efficiency in the light-load condition. The test results show that the average efficiency of the proposed SMPS is 84% and the standby power consumption is 90mW, which are both better than conventional strategy.

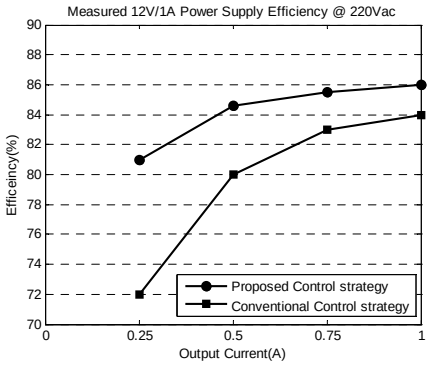

Figure 11. Measured efficiency

V. CONCLUSIONS

A low standby power consumption and high efficiency multi-mode control strategy is proposed and a chip that integrates the multi-mode control circuits is fabricated in 700V BCD technology. A laboratory prototype is built to verify the validity of the proposed strategy. From the test, we can see that the SMPS can work in QR, PFM and PSM mode and can transmit from one mode to another stably and smoothly. The proposed strategy can reduce the standby power consumption and increase the efficiency in the full range of load. Both the standby power consumption and the average efficiency meet the requirement of latest Energy Star specification with margin.

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