Impact of Process Variations and Defects on RF Front-end in Nanoscale CMOS

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***Abstract*— The scaling of MOSFET causes various process variations and defects which result in increasing performance loss of nanoscale integrated circuits. Major sources of process variations and defects in nanometer CMOS technology are studied. Then, their impact on MOSFET characteristics and on VCO circuit performances is analyzed. Finally, the paper proposes a novel self-healing circuit structure for VCO, which is able to work robustly against process variations.**

Keywords- nano-scale integrated circuits; CMOS process variations and defects; device characteristics; RF front-end

I. INTRODUCTION

With continued minimized scaling of MOSFET devices and entering nano-scale, the increasing performance loss of nano-scale integrated circuits, caused by various process variations and defects, is becoming more intolerable. The existence of various process variations and defects causes performance deterioration of signal delay and power consumption and creates a big challenge to traditional design method of VLSI. Because of the limit of various process variations and defects, the optimization of circuits with traditional method can hardly solve the problem caused by random process variations. Therefore, it is of great necessity to study the impact of process variations and defects in nano-scale CMOS technology on RF front-end and thus improve the circuit design methodology.

The main source and affected factors of nano-scale process variations and defects is firstly studied in this paper. Then, the impact of process variations and defects on characteristics of nano-scale VLSI is analyzed and described the impact in probabilistic range. Finally, with the instance of voltage controlled oscillators, the principle of impacts of variations of critical elements characteristics on performance of RF front-end was studied and corresponding improving circuits were presented. These circuits have ability of self-checking and self-healing.

II. IMPACT OF VARIOUS PROCESS VARIATIONS AND DEFECTS ON THE CHARACTERISTICS OF ELEMENTS

A. Source of Nano-scale Process Variations

The main source of process variations is the equipments of all kinds of technology and IC fabrication process. Chips with architecture of plane CMOS were taken as an example. All parameters of elements can cause different degree of variation. Most of the critical parameters studied presently are threshold voltage of transistors, the length and width of MOS, the width and thickness of wiring. The fundamental reason for causing these parameters' variations is probably internal variation source of Random Dopant Fluctuation (RDF) and Line Edge Roughness (LER). The reason may also be graphic distortion of subwavelength photoetching technology. This problem can be solved by Resolution Enhancement Techniques (RET). Shallow Trench Isolation (STI) has little impact on previous application. However, it has obvious impact on advanced CMOS technology. New materials such as k dielectrics and their performance enhancing technology have added additional source of process variations. One of the examples is that power supply voltage will drop when mobility is enhanced with various kinds of force technology. It is difficult to provide enough protecting band to ensure the predicted change of performance and characteristics when power supply voltage drops.

B. Impact of Process Variations and Defects on Elements

The impact of process variation and defects on the performance of elements is presented by phase noise. Phase noise has direct impact on short-term frequency stability of the circuits. Phase noise is defined as decibel of power rating of noise divided by average carrier power rating per frequency band at a certain amount of offset carrier frequency. That is expressed in (1) [1].

$$L(\Delta f) = 10\log\frac{P_{SSB}}{P_C} \tag{1}$$

Where, $L(\Delta f)$——Single band phase noise at a certain amount of Δf of offset carrier-frequency f_c.

P_{SSB}——Power rating of noise with per frequency band at a certain amount of Δf from offset carrier-frequency f_c.

P_C——Power rating of average carrier, its unit is mW.

The impact of process variations and defects on elements is presented by phase noise. Phase noise is an important parameter to evaluate the characteristics of VCO. Many modules were proposed to analyze the phase noise of oscillators. At present, the most practical module of negative-resistance LC oscillators is Real Module.

$$L[\Delta\omega] = 10\log\frac{2FkT\omega_0}{\left(\frac{4I_{SS}}{\pi}\right)^2 LQ^3\Delta\omega^2} \tag{2}$$

Where, the noise factor F is expressed as

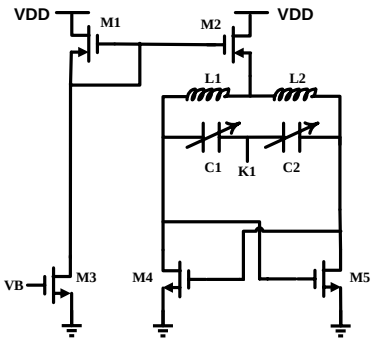

Figure 1. Basic architecture of oscillators of negative-resistance LC

$$F = 1 + \frac{4\gamma R_{\tan k} I_{SS}}{\pi V_o} + \gamma \frac{4}{9} g_m R_{\tan k} \qquad (3)$$

$\Delta\omega$ is the difference from the central frequency，γ is the noise factor of the transistor channel，L is the inductance of the resonant network，R_{tank} is the parasitic resistance of the whole circuit and V_o is the output range of the oscillator.

III. THE PRINCIPLE OF IMPACT OF PR CIRCUIT

A. The Working Principle and the Basic Architecture of Voltage Controlled Oscillators of Negative-resistance LC Model

1) The Working Principle and the Basic Architecture of Voltage Controlled Oscillators of Negative-resistance LC Model. Fig. 1 shows the basic architecture of oscillators of negative-resistance LC.

When the negative resistance of cross coupling M4 and M5 is equal to the resonance resistance of parallel resonance loop, Rp, the transferring energy of negative resistance counteracts the consumption of resonance loop exactly. The stability of the oscillation at this moment is reached.

$$R_p = \frac{L_\Sigma}{C_\Sigma \cdot r} \qquad (4)$$

Where L_Σ is the inductance value after inductance connected in series with the unit nH; C_Σ is the capacitance value after capacitor C_1 and capacitor C_2 connected in series with the unit pF; r is the parasitic resistance in the circuit of inductance L_1 and inductance L_2 in series with the unit mΩ; and R_p is the resonance resistance in the parallel resonance loop with the unit mΩ.

Equation (4) represents the relationship between parallel resonance resistance and the parasitic resistance r in inductance. This equation is approximate equation in resonance when Q value is high. Therefore, (4) is suitable for High Q value circuit. Equation (5) the stable oscillation condition of negative-conductivity LC model oscillation circuit. The circuit can output stable oscillation signal if and only if the negative-resistance provided by cross coupling transistors is larger than or equal to conductivity of resonance network.

$$\left|G_m\right| = \frac{g_{m1} \cdot g_{m2}}{g_{m1} + g_{m2}} = \frac{g_m}{2} \geq G_P = \frac{1}{R_P} \qquad (5)$$

Where, G_m the total negative conductivity provided by the two cross coupling transistors, the unit is S; g_m is the conductivity of the single transistor, The unit is S; G_p the total conductivity of LC resonance network. The unit is S.

The resonance frequency of the circuit is f_0. f_0 is expressed with (6).

$$f_0 = \frac{1}{2\pi\sqrt{L_\Sigma \cdot C_\Sigma}} \qquad (6)$$

2) The Parameter Setting of Negative Resistance LC model Voltage Controlled Oscillator. Process: 180nm CMOS process of TSMC.

Central frequency: f_0=6.77GHz.

Power supply voltage: V_{DD}=1.8V.

Inductance L_1 and L_2: L_0=0.166045nH.

Parasitic resistance in series: r_0=1093mΩ.

Variable capacitor C_1 and C_2：C_0=6.10203pF.

Current mirror: the bias voltage of M_3 V_B=1.8V, bias current I_{Bias}=22.89mA.

The output of circuit is shown in Fig. 2 when using transient simulating with the circuit. The circuit could oscillate normally.

B. Impact of Capacitance Bias on Oscillation Circuit

The most important electric characteristics of voltage controlled oscillator is oscillating frequency, phase noise and output power rating. The fundamental frequency of output of voltage controlled oscillator is shown in Fig. 3.

$$f_0 = \frac{1}{2\pi\sqrt{L_\Sigma \cdot C_\Sigma}} \qquad (7)$$

Where, L_Σ is the total inductance in inductance L_1 and inductance L_2 series. The unit is nH. C_Σ is the capacitance value in capacitor C_1 and C_2 series. The unit is pF. $f0$ is the output frequency of oscillation circuit. The unit is GHz.

The oscillation frequency is inversely proportional to the square root of parallel inductance multiplied by capacitance. Therefore, variation of the capacitance in the circuit can cause the variation of oscillation frequency. The variation of oscillation frequency is shown as jitter noise in time domain. This impact can be described by phase noise in the circuit.

TABLE I. DESIGN PARAMETERS OF MOSFETS

Design Parameters	Transistors				
	M_1	M_2	M_3	M_4	M_5
Finger #	20	20	15	15	15
Parallel #	10	10	13	13	13
Total W/L	222	222	217	217	217

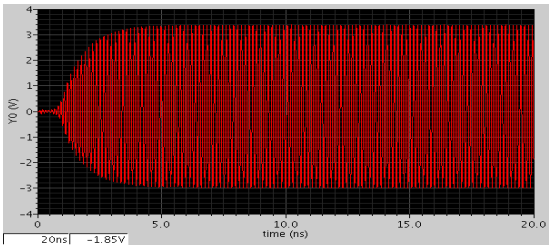

Figure 2. The output of circuit when using transient simulation

There are capacitance among wiring and coupling capacitance among elements. Therefore, there is a bias between the real capacitor value and labeled capacitor value. This causes the variation of electric characteristics of oscillators. Impact of the bias on electric characteristics of oscillators is specifically analyzed as follows.

1) Impact of Capacitance Variation on Oscillating Frequency: Oscillation frequency is inversely proportional

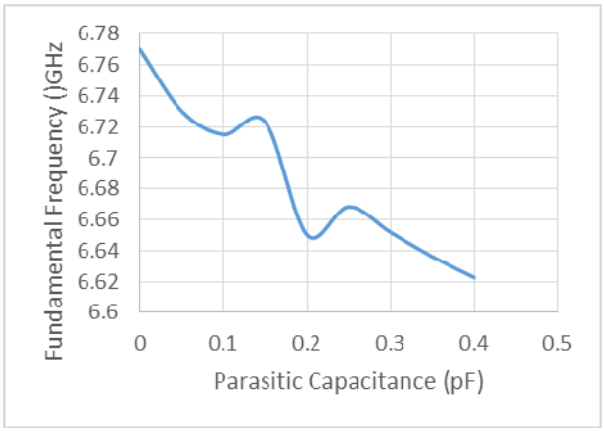

Figure 3. Impact of parasitic capacitance on fundamental frequency

to square root of capacitors. Therefore, the oscillation frequency is getting lower when the value of capacitors in the circuit is getting larger. In order to make the analysis easier, the parasitic capacitor at output terminal is assumed to be the equivalent of capacitors at different places in the circuit. This small capacitor is in parallel with C1 and C2. Therefore, the parasitic capacitor will make the total equivalent capacitance larger. The distribution of output frequency will shift lower.

2) Impact of Capacitance Variation on Phase Noise: The following can be known from impact of capacitance variation on oscillation frequency. When there is capacitance variation in the circuit, the noise power rating at a certain frequency near the carrier frequency is getting larger, the power rating of carrier is getting smaller and phase noise in the circuit is getting larger. The stability of frequency in the circuit is lowered.

3) Impact of Capacitance Variation on Fundamental Frequency: Because of restrain of nonlinear elements in the circuit and impact of parasitic capacitors, the output frequency spectrum of the oscillator not only consists of useful fundamental frequency (carrier frequency), but also consists of many high order harmonic components. These high order harmonic components usually become the output noise of oscillators. As is mentioned above, capacitance variation in the circuit will cause increasing proportion of harmonic components in the spectrum, greatly reducing the proportion of useful output power, i.e. the spectrum purity deteriorates.

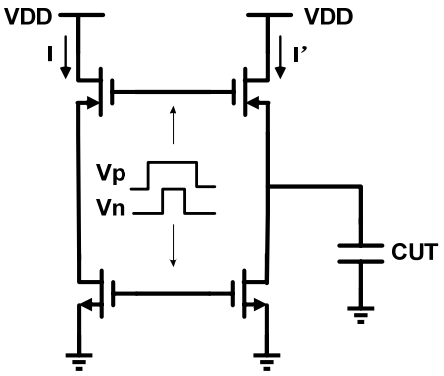

Figure 4. The architecture of CBCM measuring circuit

C. Improvement on Oscillator Circuit

The following is known from above description. Capacitance variation and mismatching among threshold voltage of MOSFETs have great impact on the performance of oscillators. It is necessary to reduce that impact by improving the oscillation circuit.

1) Reducing the Sensitivity of Oscillation Frequency from Capacitance variation: The output frequency of oscillation circuit becomes lower when parasitic capacitor on the output terminal of oscillation circuit in Fig. 1 increases. The curve gradient, df_0/dC, is the sensitivity of oscillation frequency from capacitance variation. The larger the sensitivity is, the bigger the oscillation frequency variation caused by the same capacitor is. The derivation of two sides of (7) to C is the expression of the sensitivity of oscillation frequency from capacitance variation.

$$\frac{df_0}{dC} = -\frac{1}{2} \cdot f_0 \cdot C^{-1} \tag{8}$$

Where, f_0 is the output frequency of oscillation circuit. The unit is GHz. C is the capacitance value of oscillation circuit. The unit is pF. We know from (8) that the sensitivity of oscillation frequency to capacitance variation becomes smaller when the capacitor value is getting larger. Therefore, as to certain oscillation frequency f_0, a larger capacitance value should be chosen to reduce the impact of capacitance variation.

2) Self-testing and Self-healing of Capacitance Variation: The oscillator can maintain the variation of oscillation frequency in a small range with the existence of capacitance variation by above method of reducing the

sensitivity of oscillation frequency from capacitance variation. However, in order to fundamentally reduce the impact of capacitance variation, we have to carry out the self-check and self-calibration of capacitance variation in the circuit and realize self-healing of capacitance variation in the circuit.

We first measure parasitic capacitor of drain region of cross coupling transistor with the method of Charge-Based Capacitor Measurement (CBCM). Then, we compensate the bias caused by parasitic capacitor by regulating variable capacitors in the circuit and finally realize self-regulation of characteristics of output frequency, phase noise, etc. of the oscillation circuit.

a) Basic Principle and Measuring Circuit of CBCM . CBCM for measuring capacitance [2] is first proposed by Chen, J. C., Sylvester, D. and Chenming Hu at UC Berkeley in 1998. Many improving circuits were proposed to enhance the measuring accuracy in recent years [3-6]. The traditional CBCM circuit consists of two pseudo inverters shown in Fig. 4 [2]. The only difference between the left inverter and the right one is that the right one has a capacitor for measuring in the drain region. Meanwhile, in order to ensure that there is only one transistor on, the clock signals for PMOS and NMOS cannot overlap. When PMOS is conducted, the current will go to the capacitor from DC power supply and charge the capacitor. Later, the PMOS will close and NMOS will be conducted. The electric charge stored in the capacitor will discharge from NMOS to earth. In order to measure the capacitor with CBCM method, only does the average direct current that passes through each inverter need to be measured. The difference of the two currents can be used to calculate the value of the capacitor for measuring. The calculating equation is as follows.

$$C = \frac{I' - I}{V_{dd} \cdot f} \tag{9}$$

Where, I' is the direct current that passes through the inverter with the capacitor for measuring. The unit is A. I is the direct current that passes through the inverter without the capacitor. The unit is A. V_{DD} is the power supply voltage of the circuit. The unit is V. f the frequency of output clock. The unit is Hz.

Because of using CBCM method for measuring capacitor, the direct current is only needed to be measured. Therefore, it is convenient for measurement and the accuracy is high. The accuracy can reach 0.1fF (10^{-16}). Therefore, the capacitance variation and parasitic capacitors in oscillation circuit can be measured with this method.

b) Self-testing and Self-correcting Circuit Architecture. As is analyzed above, CBCM has features of ease of measurement, high precision, suitable for measuring faint capacitance, etc. Therefore, we combine the oscillator and the CBCM measurement circuit. Basic data processing circuit is introduced to form a system of self-measurement and self-correction. The system is shown in Fig. 5. Fig. 6 shows the DSP algorithm. The direct current that goes through the two inverters in the CBCM testing circuit is converted to digital signal by the ADC and is recorded in the DSP. Parasitic capacitance in NMOSFETs M4 and M5 i.e. C_{M4} and C_{M5} can be derived according to (6) in the DSP. The serial connection of the two parasitic capacitances in series is the capacitance variation that is introduced into the LC resonant circuit by the cross-coupled transistors M4 and M5. Therefore, the value of variable capacitors C1 and C2 in series should be the ideal value detracted by the variation, i.e. C-ΔC, in order that the capacitance in the LC resonant circuit is C. Finally, the voltage posed on C1 and C2 is derived by (10) and feeds back to K1.

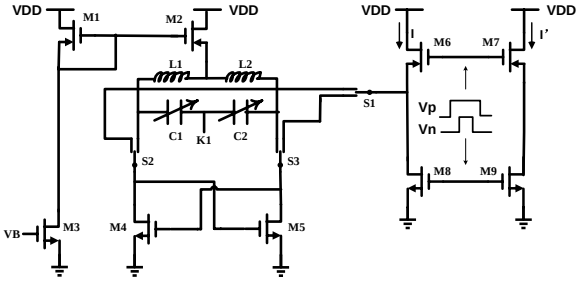

Figure 5. Circuit of the Self-testing Oscillator

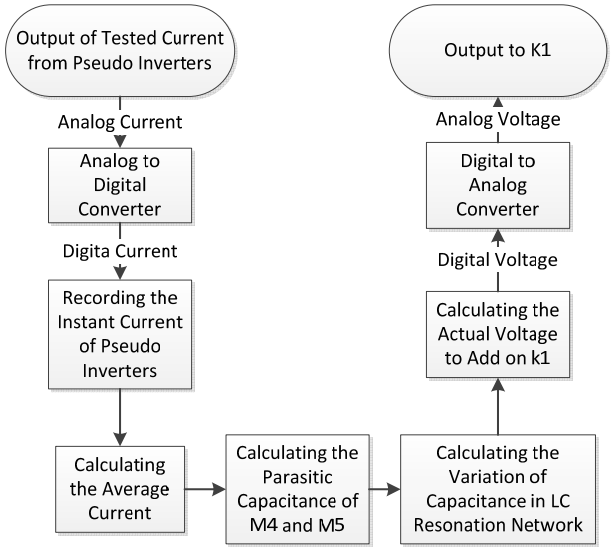

Figure 6. Diagram of the Self-Healing DSP Algorithm

$$2(C - \Delta C) = \frac{C_{j0}}{(1 - \frac{V_D}{V_B})^n} \tag{10}$$

Where C_{j0} is the value of the variable capacitance at zero bias, unit: pF; V_D is the voltage on the plates of the capacitor, unit: V; V_B is the potential barrier voltage of

variable capacitance, unit: V； n is index of variable capacitance (determined by process).

IV. CONCLUSION

The major sources and objects of process variation and defects in nano-scale CMOS is introduced. Then, the impacted properties of devices are analyzed. Finally, the VCO is taken as an example for the study of the impact of capacitance variation on RF front-end. An improved circuit is proposed which has functions of self-test and self-correction and it is testified that this circuit has a significant rise in performance.

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