Study on 2000V SiC JBS Diodes

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***Abstract*—High voltage 4H-SiC Ti schottky junction barrier schottky (JBS) diode with breakdown voltage of 2000V and forward current of 2A has been fabricated. A low reverse leakage current below 1.9×10^{-6}A/cm^2 at the bias voltage of -2kV has been obtained. The forward on-state current was 2A at V_F = 1.9V and 5A at V_F = 3V. The chip is 2.3mm×2.3mm. The turn-on voltage is about 1.0V. The on-state resistance is 19.3mΩ·cm^2. The doping and thickness of the N-type drift layer and the device structure have been performed by numerical simulations. The SiC JBS devices have been fabricated and the processes were in detail. The die was packaged with SMB mode. The thickness of the N-epilayer is 17μm, and the doping concentration is 4.6×10^{15}cm^{-3}. A floating guard rings edge termination have been used to improve the effectiveness of the edge termination technique. By using Ti/Ni/Ag multilayer metal structure, the double side Ag process of 4H-SiC JBS diode is formed. We use the PECVD Si_zN_y/SiO_2 as the passivation dielectric and a non photosensitive polyamide as the passivation in the end.**

Keywords- 4H-SiC; JBS ; Floating guard rings

I. INTRODUCTION

The breakdown electric field in SiC, 3 MV/cm, is one order of magnitude higher than that in Si. Hence, the SiC Schottky barrier diode (SBD) is expected to have better steady loss and switching loss, compared to Si pin diode [1]. In order to obtain the high reverse voltage with the low leakage current, the development of 4H-SiC SBDs is junction barrier Schottky (JBS) diodes. The Junction Barrier Schottky (JBS) rectifier is a device, which combines a PiN diode and a Schottky diode making use of the advantages of both types [2]. In Silicon, the difference in barrier voltages in a PiN diode and Schottky diode are small. The similar forward voltage is about 0.8V. The JBS structure in Si is mainly used to lower the recovery transient losses. By operating the diode at a forward voltage where the p+ regions are injecting but at the same time having current conduction through the Schottky contact the reverse recovery current is lowered with only a little sacrifice in forward voltage and leakage currents. When the JBS diode is operated in this mode it is usually referred to as the Merged Pinch Schottky (MPS) rectifier. In these SiC JBS diodes, Schottky regions alternate with implanted p+ regions. Schematic cross section of a JBS structure is shown in 0.

The forward current flows through the Schottky regions, so that the metal/SiC Schottky contact determine the on-state resistance of this kind of diode. The distance between the p+ regions is made so narrow that the space charge regions of neighboring *p–n* junctions in a reverse biased diode merge at a certain voltage, which must favor a decrease in leakage currents. Many authors have investigated the properties of SiC Schottky rectifiers on SiC and Cree, Rohm, Infineon have produced commercial 4*H*-SiC SDs which are intended for reverse voltages of 600, 1200, and 1700 V. However, there is also demand for higher voltage fast diodes [3]. We have already reported a high-voltage (>1.1kV) Ti/4H-SiC SBD fabricated on 12um thick 4H-SiC epilayer with B^+ implantation edge termination and field plate technology [4].

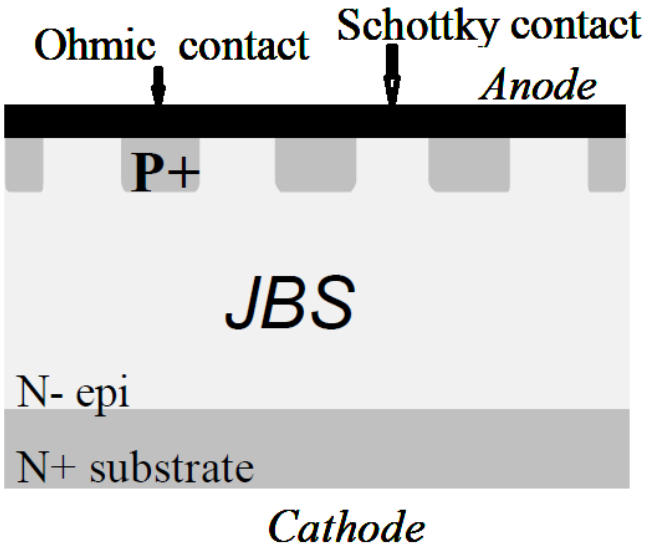

Figure 1. The schematic cross section of a JBS structure

In this paper, we reported the design, fabrication and the measurement on electrical characteristics of SiC JBS devices. TCAD simulations have been performed to select the doping concentration and the thickness of the drift layer and the effectiveness of the guard ring termination technique. The epilayer properties of the N-type are 17 μm with a doping of 4.6×10^{15} cm^{-3}. The diodes were fabricated with a 17 floating guard rings edge termination. The diodes can block a reverse voltage of at least 2kV, and the on-state current was 5 A at V_F = 3V. The measured leakage current and breakdown voltage are close to the calculated value.

II. DESIGN AND FABRICATION

The electric field in the plane of the metallic contact reaches values of 10^6 V·cm^{-1} in 4H-SiC SBDs at high reverse biases [5], such strong fields can cause bulk leakages. In the JBS structure shown in 0, forward current flows through the Schottky regions, the width of the p+ region is chosen to be small in order to provide the larger ratio between the areas of the Schottky regions and p+ region, thereby minimize the on-state resistance of the diode. The inner p+ fingers under the Schottky metal were formed simultaneously with the guard rings, the implantation was performed with Al ions doping into the *n*-layer. By TCAD simulation, the number of floating guard rings was 14 in a chip, the width of each guard ring was 3μm, distance between the rings was 2μm. The simulations result was shown that it can block a reverse voltage of 2kV and higher.

The SiC JBS devices have been fabricated at Science and Technology on Monolithic Integrated Circuits and Modules Laboratory, using 4H-SiC wafers purchased from CREE and epitaxial layers provided by CETC 55. In the device, the n- 4H-SiC epitaxial layer is grown on the n+ 4H-SiC substrate. The active layer doping level and thickness were the following: N_d=4.6×10^{15}cm^{-3}, and d=17um, respectively.

The SiC wafer was given a typical clean. After cleaning the sample, the processes began with the formation of the mark. Then we formed the p+ regions and the p+ guard ring edge termination by using the multiple energy Al implantation at room temperature with maximum energy 320kev and dose 5.4 × 10^{13}cm^{-2}. Post implantation annealing to activate the implanted Al dopant was done in an Ar ambient in a furnace at 1850℃ for 3min. Before the anneal process, the wafer was coated with 8μm thick photo resist and carbonized at 700℃ for 2h. The carbon layer was removed by sacrificed oxidation. And then the large area Nickel back-side ohmic contact was evaporated and annealed in N_2 atmosphere at 950° C for 5 min with the SiO_2 layer mask on the SiC front-side. Removing of the SiO_2 layer was performed using 1/10 HF/H_2O etchant. A Schottky contact is designed to cover both the p+ implanted regions and the n- unimplanted ones. Squareness Ti Schottky contacts with length of 1mm were evaporated. The anode Schottky contacts was formed by thermal evaporation of Ti with thickness of about 150 nm, with the subsequent annealing at 400 °C for 10 min. After annealing at the temperature 400℃ in N_2, the reverse current decreases one order of magnitude. The forward I–V characteristics do not undergo a change after the annealing. It signifies that Schottky barrier height has the same value prior to and after the process. Observed phenomena are determined by defects in the interface between metal and semiconductor, which are generated near the semiconductor surface when the metal contact is deposited on this surface. The annealing has no influence on forward I–V characteristics, but the reverse leakage current is reduced as a result of decreasing number of surface states. This phenomenon decreases generation of minority carriers due to reduction of the number of available discrete energy levels in the band gap of investigated material. As the passivation dielectric, the 500nm Si_xN_y/SiO_2 was deposited by PECVD. By using Ti/Ni/Ag multilayer metal structure, the double side Ag process of 4H-SiC JBS diode is formed. A non photosensitive polyamide is as the final passivation. The SiC JBS die and the packaged device with SMB mode are shown in 0 and 0.

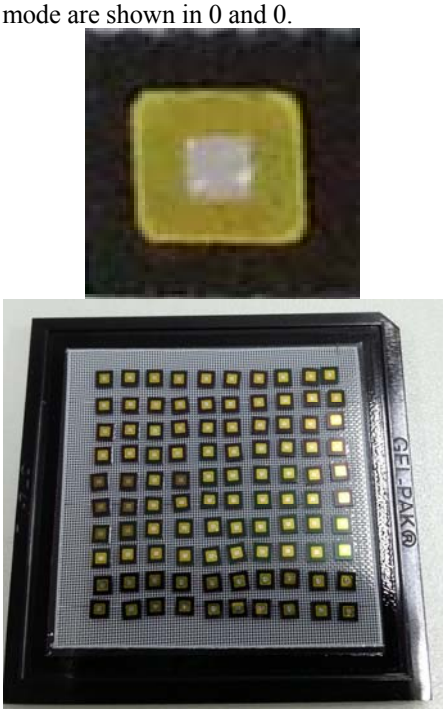

Figure 2. The schematic diagram of diode JBS die

Figure 3. The schematic diagram of diode JBS device with SMB package

III. RESULTS AND DISCUSSIONS

The forward characteristics were tested with an Tektronix 371 curve tracer and the reverse characteristics were tested with an Tektronix 370 curve tracer when the devices are packaged with SMB mode. All tests were performed at room temperature.

Reverse I–V Characteristics

0 shows typical room temperature reverse current-voltage (I–V) characteristics of the 4H-SiC JBS diodes. It can been seen that the guard ring edge termination effectiveness is good. When the breakdown voltage of JBS get to 2kV, the leakage current is about 0.45μA (leakage current density 1.9×10^{-6}A/cm^2). In the future work, we will choose the suitable distance between the guard rings based on JBS fabricated to

improve the edge termination effectiveness and the forward current.

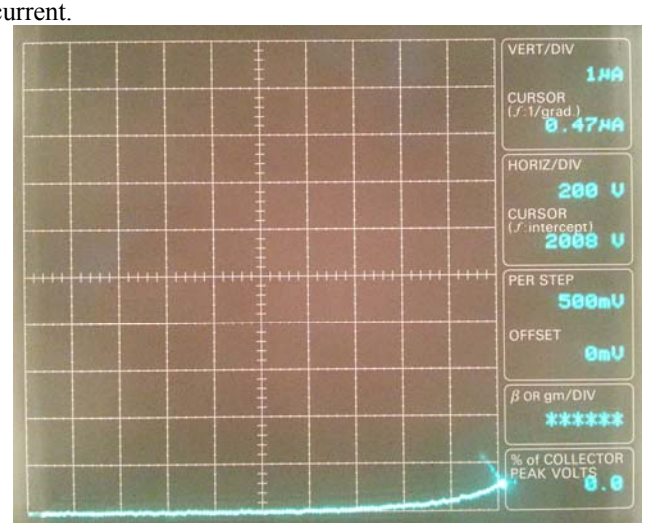

Figure 4.Reverse I-V characteristics of the fabricated 4H-SiC JBS diodes.

Forward I–V Characteristics

The points in 0 show a forward I–V characteristic of JBS in the open state. The on-state current is 2A at V_F = 1.9V and 5A at V_F = 3V, the turn-on voltage is about 1.0V. The simulation result and the test result are almost the same. The chip is 2.3mm×2.3mm. The on-state resistance is 19.3mΩ·cm^2.

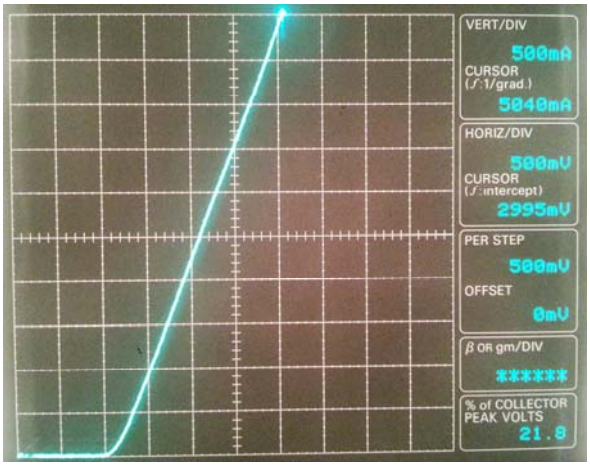

Figure 5. Fitting of forward I-V characteristics in room temperature

IV. CONCLUSION

In summary, we have fabricated SiC JBS devices on n+ conductive 4H-SiC substrates. The processes of the SiC JBS were developed and high performance of the SiC JBS device was reported. By employing a high energy ion implantation and high temperature annealing technique, excellent characteristics were obtained. The breakdown voltage improved from 1100V to more than 2000V depending on device guard ring termination structure. A low reverse leakage current below 1.9×10^{-6}A/cm^2 at the bias voltage of -2kV has been obtained. The forward on-state current was 2A at V_F = 1.9V and 5A at V_F = 3V. Further study is to optimize the fabrication in order to get a lower reverse leakage and higher forward conduction.

ACKNOWLEDGMENT

We would like to thank all the members of wide band department and Science and Technology on Monolithic Integrated Circuits and Modules Laboratory. Helps received from the silicon devices department are also acknowledged. The work was supported by the National 863 Program (Grant No. 2011AA050401) from the Chinese Ministry of Science and Technology.

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