Simulation Study on Internal Transparent Collector IGBT Using Superjunction Drift

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Abstract—**The super junction (SJ) drift is used in internal transparent collector IGBT. The influences of position of local carrier lifetime region, local carrier lifetime, and buffer layer doping level on the devices' trade-off characteristics have been simulation studied. The results show that for given local carrier liftetime, the turn-off losses may have a valley value E_{offmin}. The higher local carrier lifetime is, the higher E_{offmin} will be. Several factors are at work. Competition effects for excess carrier extraction through reverse biased super junction and forward biased collector may be one reason. Infinite excess carrier recombination velocity in local carrier lifetime control region leads to the back-emitter injection efficiency γ_e be no less than certain value. In addition; increasing buffer layer doping level appropriately could win better trade-off and wider trade-off range.**

Keywords- superjunction; local carrier lifetime; internal transparent collector; IGBT

I. INTRODUCTION

MOSFET is widely used in low and mid voltage application. But as a unipolar device, the specific drift region on-state resistance sR_{don} has 2.5-power dependence on breakdown voltage[1]: $sR_{on} \propto (BV)^{2.5}$. So the on-state resistance becomes so large for high voltage MOSFET. This limits its application in high voltage fields. To overcome this limitation, superjunction (SJ) drift region based on charge balance is proposed [2] and first used in CoolMOS[3]. SJ drift region makes the drift region resistance is nearly linear dependent on blocking voltage[4-5]. This makes the resistance of high voltage MOSFET reduced greatly.

Around 2002, SJ concept is used in planar PT-IGBT[6]. Simulation results show SJ FS-IGBT has the best tradeoff performance in its class. But for 600V IGBT, FS-IGBTs need super thin wafer technology. So most studies on low voltage SJ FS-IGBT are focused on simulation research[7-10].

Internal transparent collector (ITC) IGBT is a new type of IGBT proposed for low voltage IGBT (for example 600V)[11]. It based on PT-IGBT technology, but a local carrier lifetime control (LCLC) region is introduced in the collector region near the buffer-collector junction. This changes the collector from non-transparent to internal transparent. The device has similar performance to that of transparent collector IGBT, but needs no thin wafer technology for low voltage IGBT. In this paper, SJ drift region is introduced in ITC-IGBT, and SJ ITC-IGBT is obtained. Though SJ ITC-IGBT may have some similar behaviors to SJ FS-IGBT, finite recombination rate of local carrier lifetime region makes its performance be influenced by local carrier life and the position of LCLC region. Thus, SJ ITC-IGBT has its own characteristic and particularity. In this paper, trade-off performance of 600V SJ ITC-IGBT under different local carrier lifetime and LCLC position will be simulation studied. In addition, the influence of buffer layer doping level are also studied.

II. STRUCTURE OF SJ ITC-IGBT

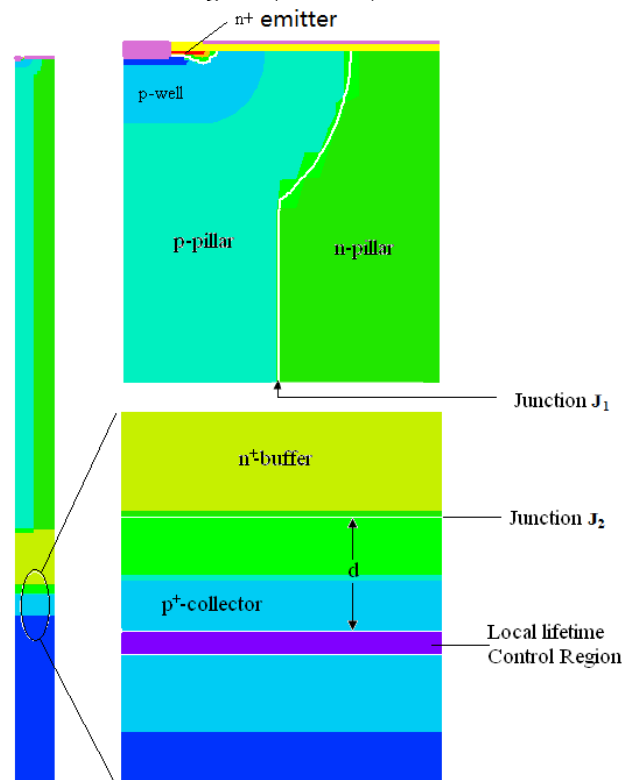Simulation used structure of 600V planar gate SJ ITC-IGBT is shown in figure 1(half cell).

Figure 1 Cross section of SJ ITC- IGBT

The channel is 1.5μm long, SJ drift region is 50μm long, buffer layer is 5μm thick, and p$^+$ substrate doping level is 5

$\times 10^{19}\text{cm}^{-3}$. Local carrier lifetime control region is 0.3μm wide. The width of p- pillar and n-pillar are equal. The pillar doping level is determined by (1):

$$N \cdot w \approx \frac{\varepsilon_s E_m}{q} = \frac{\varepsilon_s \cdot (4010 N^{1/8})}{q} \tag{1}$$

Where N is pillar doping level, w is pillar width, ε_s is silicon permittivity, and E_m is maximum electric field of silicon. For 3um pillar width, the pillar doping level is about $8 \times 10^{15}\text{cm}^{-3}$, and $6 \times 10^{15}\text{cm}^{-3}$ doping level is for 4um pillar width.

III. DEVICE SIMULATIONS AND DISCUSSION

Simulations were carried out by using TWB [11]. During dynamic simulation, area factor 0.1cm^2 was multiplied. The DC link voltage is 300V. Turn-off losses were estimated under inductive load at 27ºC. The turn-off current is 20A.

ITC-IGBT is characterized by local carrier lifetime control. The position of LCLC region and local carrier lifetime play important role in determining device performance. Simulations focused on their influence on device trade-off performance.

A. Influence of Position of Local Carrier Lifetime Control Region

First, the 4um-wide with $6 \times 10^{15}\text{cm}^{-3}$ doping level SJ pillar, and 1ns of local carrier lifetime are used for the device simulation. The dependence of key parameters(including blocking voltage BV, on-state voltage V_{on}, turn-off losses E_{off}, and short circuit current I_{SC}) on the position of LCLC region(labeled as distance d between LCLC region and buffer-collector junction J_2 , also see figure 1) is depicted in figure 2. It shows that the device's BV and V_{on} decrease, and yet the E_{off} and I_{SC} increase as the distance d between LCLC region and buffer-collector junction is increased, owing to the back-side emitter (p-emitter, collector) injection efficiency γ_e (defined as the ratio of hole current to total current at buffer-collector junction J_2) increases with d. These follow well-known rule of the device.
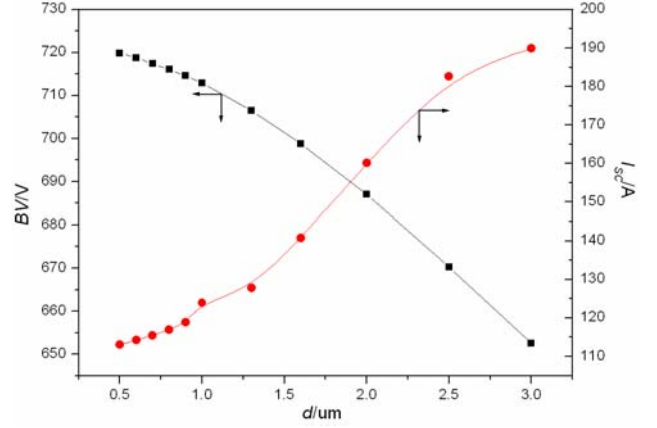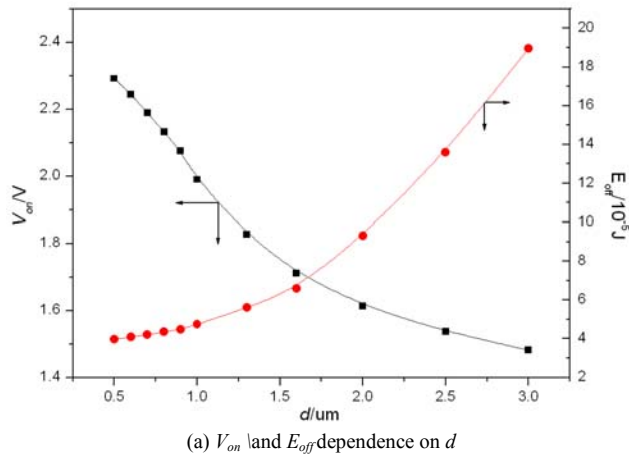

(a) V_{on} \and E_{off} dependence on d

(b) BV and I_{SC} dependence on d

Figure 2 Dependence of key parameters on d

B. Influence of Local Carrier Lifetime

To clarify the influence of local carrier lifetime, device trade-off performances under different local carrier lifetime were simulated and the results are shown in figure 3.
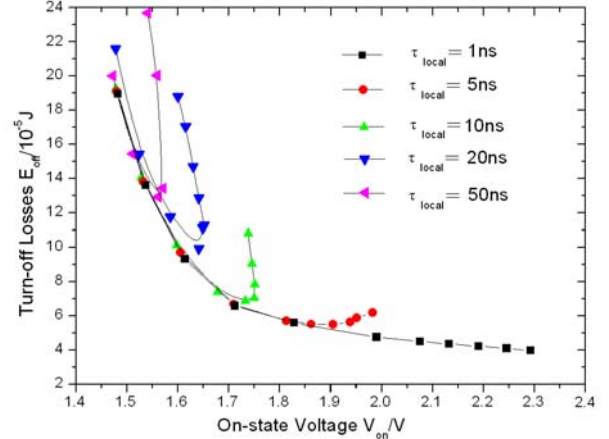

Figure 3 Trade-off curves between V_{on} and E_{off} under

different local carrier lifetime

The figure shows that: (1) When the local carrier lifetime is short enough, the trade-off curve follows the normal rule that the on-state voltage V_{on} increased and turn-off losses E_{off} decreased when the distance d between LCLC region and buffer-collector junction is decreased; (2) When the local carrier lifetime increased to some value (for example 5ns), the on-state voltage V_{on} increased with d decreased, but the turn-off losses decrease first and then increase with d decreased. E_{off} has a minimum value; (3) Increasing local carrier lifetime further (>10ns), both on-state voltage and a turn-off loss has an extreme value when the d varies. The maximum on-state voltage V_{onmax} and minimum turn-off loss E_{offmin} changed with the local carrier lifetime. So does the corresponding distance d_{min} and back-side emitter injection efficiency γ_{emin}. Their relationship is shown in figure 4.

A valley value of E_{off} also appeared in SJ FS-IGBT[12]. It was explained that this phenomenon was due to SJ IGBT

operation mode change (from bipolar to unipolar). But back-emitter injection efficiency controlled by local carrier lifetime is unique to SJ ITC-IGBT. To clarify the mechanism, the back-emitter injection efficiency γ_e variation with d is plotted in figure 5.
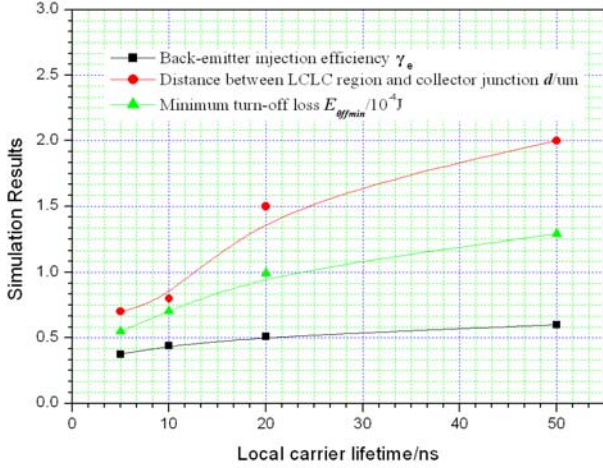

Figure 4 Variation of E_{offmin}, d_{min}, and γ_{emin} with local carrier lifetime
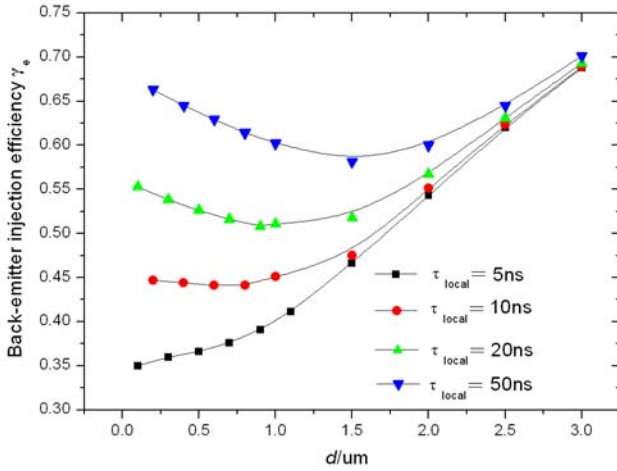

Figure 5 Back-emitter injection efficiency γ_e changes with d.

Figure 5 shows that:

(1) When local carrier lifetime is short (less than 5ns) enough, device back-emitter injection efficiency γ_e will decreases with d. But only the device with 5ns local carrier lifetime has a turning point at γ_e=0.38. The device with 1ns local carrier lifetime has no such point even though the back-side emitter injection efficiency is as low as 0.15(not plotted in figure 5). So operation mode change may not the only reason which leads to valley turn-off losses. The competition effects for excess carrier extraction through two junctions——reverse biased super junction and forward biased buffer-collector junction, may also influence the turn-off loss. This will be discussed in other paper.

(2) When local carrier lifetime is longer, owing to the finite excess carrier recombination velocity in local carrier lifetime control region, the back-emitter injection efficiency γ_e has a minimum value. This leads to the minimum E_{off} and maximum V_{on}. To obtain faster switching speed, the modification of LCLC region position is not enough. Other method such as buffer layer doping level control should be taken. Next section will discuss such question.

In summary, for given local carrier lifetime, the position of LCLC region has an optimum range. Too near of LCLC region to buffer-collector junction may leads to either higher turn-off loss (for longer local carrier lifetime) or higher on-state voltage (for shorter local carrier lifetime).

C. Influence of Buffer Layer Doping Level

The buffer layer of IGBT normally has two roles, one is for field stop and the other is for injection efficiency (back-emitter) control. Keeping buffer layer thickness unchanged and increasing buffer layer doping level from 5×10^{16}cm^{-3} to 7×10^{16}cm^{-3}, simulation study the trade-off performance of SJ ITC-IGBT with 10ns local carrier lifetime. The results show that trade-off performance has a little improvement and lower minimum turn-off loss could be obtained comparing to lighter buffer doping level (see figure 6). Increasing buffer layer doping level appropriately could win better trade-off and wider trade-off range.
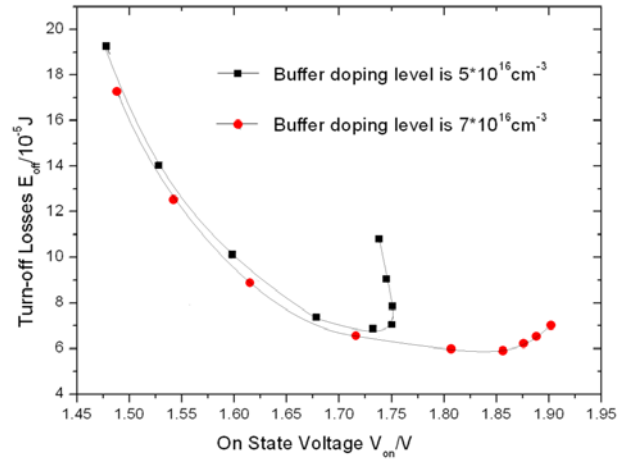

Figure 6 Trade-off curves between V_{on} and E_{off} with different buffer doping

IV. CONCLUSION

Simulation study was performed for SJ ITE-IGBT. The influence parameters on the trade-off performance of the device includes the position of local carrier lifetime control (LCLC) region, local carrier lifetime, and buffer layer doping level. For given local carrier lifetime, the position of LCLC region has an optimum range. Too near of LCLC region to buffer-collector junction may leads to high turn-off loss. The finite excess carrier recombination velocity in local carrier lifetime control region leads to the back-emitter injection efficiency γ_e has a minimum value. This leads to the minimum E_{offmin} and maximum V_{onmax}. And the longer local carrier lifetime is, the higher E_{offmin} will be. Increasing

buffer layer doping level appropriately could win better trade-off and wider trade-off range. All these results could provide helpful references for device design.

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