Research and Design on the Key Technology of DVB-T Baseband System

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Abstract—**DVB-T standard has been one of the most important standards for terrestrial transmission in the world. According to investigate the principle of DVB-T baseband system, this paper focus on the key module of DVB-T modulator and synchronous module. Firstly, this paper establishes a complete DVB-T transmitter system, then detailed analysis, improves and simulates the synchronization algorithms based on existing algorithms. At last, we build a platform of this system, debug and verify the module through the FPGA chip of Xilinx. As the test results given at the end of this paper, this system meets the requirements of DVB-T and has a good performance.**

Keywords-DVB-T; Channel Coding; Synchronization; FPGA

I. OVER VIEW OF DVB-T TRANSMISSION SYSTEM

Digital Video Broadcasting-Terrestrial is one of the mainstream terrestrial transmission standard which uses terrestrial as transmission media for MPEG-2 digital television signal. Digital television terrestrial transmission face a complex situations during the transmission influenced by multipath, strong noise and various imperfect transmission condition.

The transmitter system is composed of source coding module,channel coding module and modulation module. The overall structure of system is shown in figure 1.
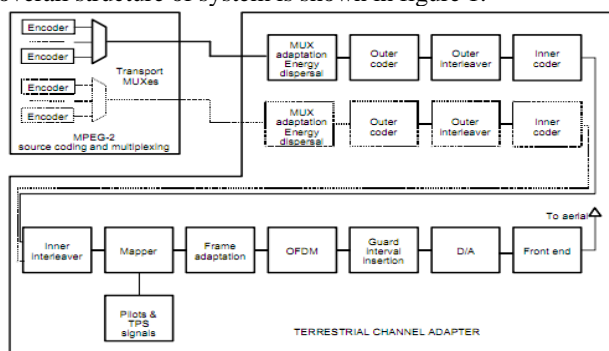

Figure 1. Functional block diagram of the system[1]

Simply said,the time-domain baseband DVB-T symbol generated by the multi-program transport stream(MPTS) will go through the following process,and then OFDM modulation has realized:

- MPTS received from source coding module and energy dispersal.

- Outer codeing and interleaving module.Each 188-byte data added 16-byte redundance data to form 204-byte transmission stream and then interleaving.

- Inter encode and interleaving module which compose of convolution coding ,bit and symbol interleaving.In order to avoid burst intersymbol interference,reduce the error rate.

- Mapping in amplitude and phase by three modulation ways of QPSK,16QAM, 64QAM,and insert pilot and TPS. DVB-T frame has formed

- Convert into a 2K or 8K mode after IFFT convert.

The receiver's function module of DVB-T system is shown in figure 2:
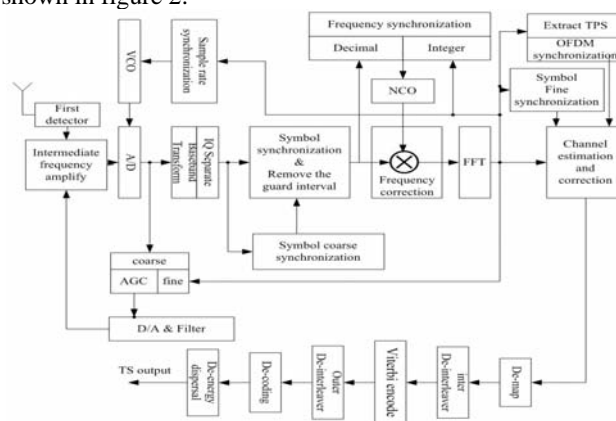

Figure 2. Function module of DVB-T receiver

The receiver system is divided into 3 parts[2]: time and carrier synchronization module, channel estimation and verification module and channel decoding module. Firstly,analog signal of medium frequency is converted to baseband signal. Secondly time and carrier resume module under the control of time and carrier synchronization. Signal compensated is putted into FFT converter.And then pilot and TPS signal is extracted for time and carrier fine synchronization, channel estimation and verification. Finally, the data after verification is putted into outer receiver and a operation contrary the operation in transmitter is executed in channel decode.

This paper researches and realizes the key module of DVB-T baseband system, such as coding and frame formation module in transmitter, synchronization module in receiver, based on detailed analysis the DVB-T standard. We also present the improvement plan and time verification

of this design on FPGA, and then give the simulation waveform and the test results at the end of this paper.

II. REALIZE THE KEY TECHNOLOGY IN DVB-T MODULATOR

Based on the analysis of the DVB-T structure, this section gives the specific implementation of the key module in transmitter.

A. RS coding

The input of the DVB-T modulator is 188-byte fixed length MPEG-2 stream. The first byte of each packet is synchronous byte,whose value constantly equal 47H or B8H.

The outer code error correction module of DVB-T uses RS (204,188, t = 8) truncated code to encode. For each 188-byte transport stream, we add 16-byte of redundant error correction code to generate a error protection package. This code can correct 8-byte burst errors[1].

The RS encoder which designed by this paper, in fact, is a polynomial divider, and defines the code words generation polynomial and domain polynomial.

This paper uses linear feedback shift register to realize a polynomial divide,utilize the information code to get the modulus of generate polynomial g (x) , then can obtain the check bytes.

Figure 3 shows the simulation waveform figure of RS encoder in Models in SE.188-byte data ,such as 47, 5d, 4e,... output directly ,when as 16-byte 00 check data at the end of data frame is replaced by the results which calculated by the RS encoder. Then we can get the 204 -byte data.
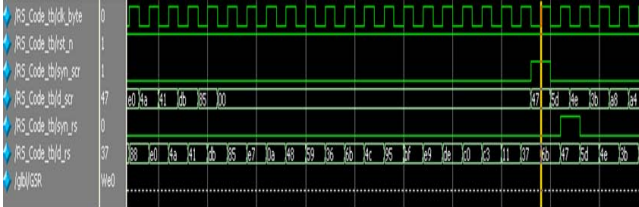

Figure 3. RS（204，188，t=8）encode waveform

B. Frame formation

Figure 4 shows the top-level module of DVB-T frame formation.

I,Q effective sub-carrier data which after mapping is entered into the mapping data FIFO;

Transmission parameter signaling(TPS) signal describes the main parameters of the DVB-T system and output from BCH encode module is entered into the TPS FIFO.

The Prbs_data_out,Prbs_en_out,and Type_out signals which output from sub-carrier type selection module are modulated by DBPSK.Then three new signals:Prbs data signal(Prbs_data1),Prbs data enable signal (Prbs_en_out),and sub-carrier type selection signal(Type_out1) can be formed.

The data from mapping FIFO ,TPS FIFO and Sub-carrier type selection module can be composed of OFDM data which have 45 continuous pilots ,17 TPS and discrete pilot cycle of 12.

After spectrum moving, this OFDM data can be translate into I,Q data and its effective signal, which is processed into IFFT module, then get the OFDM symbol finally.

DVB-T system using separate frame transmission way, every frame contains 68 OFDM symbol, every 4 frame form a super frame[1].

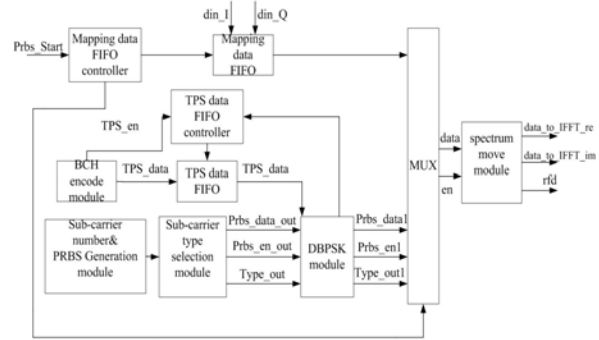
Figure 4. top-level module of DVB-T frame formatting

Figure 5 is the frame simulation figure by timing simulate in Modelsim SE.As shown in this figure ,we can see after this module ,each OFDM symbol is inserted zero. RFD is the effective signal of data , rdy_d1 is the control signal which for starting the IFFT module , when rdy_d1 equals to 1, the IFFT operation began.
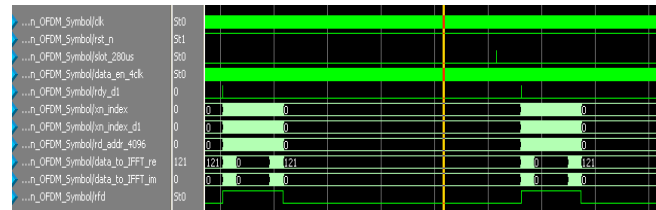

Figure 5. data output waveforms after the formation of the frame

III. IMPROVEMENT AND REALIZE OF SYNCHRONIZATION MODULE IN DVB-T RECEIVER

The synchronization system which based on multi-carrier system like OFDM ,mainly includes timing synchronization and carrier synchronization[3].

Fristly, using the timing and decimal frequency offset joint estimation to confirm the edge of the symbol ，and compensate decimal frequency offset .Then, using the pilot to complete integer frequency offset estimation.

This paper uses module multiplex and improveing traditional algorithm to reduce the computational complexity, and have a good performance in estimation.

A. Timeing synchronization

Now commonly algorithm for robust estimation is MLE algorithm which advanced by Jan-Jaap Beek and Magnus Sandell.This algorithm can estimate timing and decimal frequency offset jointly[4] .

The MLE algorithm uses the strong correlation between the symbol-head and symbol-tail ,the cycle prefix(Ng points) in DVB-T sequence ,and the information about symbol offset and frequency offset to estimate unknown parameter .

Set $f(\vec{r} \mid n_{err},\ \Delta f)$ as $2N+N_g$ points joint conditional probability density function under the condition of given OFDM symbol arrived moment n_{err} and frequency offset Δf .Its logarithm likelihood function can be expressed as:

$$\Lambda(n_{err}, \Delta f) = \lg f(\vec{r} \mid n_{err}, \Delta f) \quad (1)$$
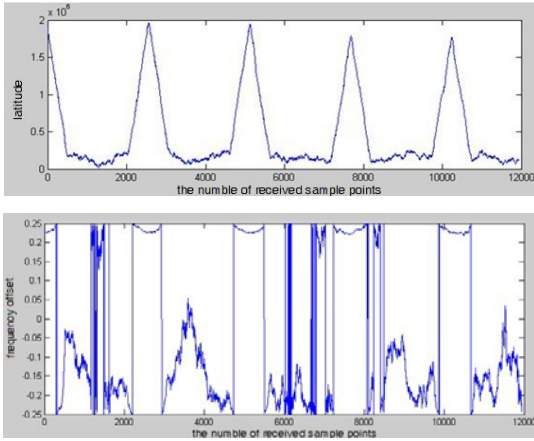

Figure 6.   ML algorithm simulation waveform in WGN channel

Figure 6 shows the likelihood function curve which is used for symbol robust synchronization of DVB-T system (2K mode) ,this systerm uses SNR=16dB,GI= N/4,normalization frequency offset is 4.224 .In the start of the symbol has the maximum of likelihood function ,which can be used for timeing robust synchronization to camfrie the start point of the FFT demodulation. At the same time, we can estimate carrier frequency offset, but only got the decimal part of the carrier frequency off set, as $\mid \Delta f \mid < 0.5$.

But when the signal transmit in the multipath channel, part of the cycle prefix will be polluted by the symbol before, so if we use the whole cycle prefix to calculate the correlation result, the effect of estimation is not very good. This paper on the basis of MLE algorithm, removes the data which has been polluted ,and uses the cycle prefix rest to calculate the correlation result and estimate finally. Thus, it can not only improve the effect, but also reduce the estimated computational cost.

This paper according to the different channel characteristic in advance, set up a channel power window wide PW (i.e. channel power mostly concentrated in this window),then make $L' = N_g - PW$,L' is the length of the data which is used for correlation calculation.

DVB-T standard provides two kinds of multipath channel model . Most of the multipath channel power concentrated in

the power window of width to 30 points around, so we can set PW=30. Then the maximum correlation estimation algorithm as ：

$$\hat{n}_{err} = \arg \max_{n_{err}} \left\{ \left| \gamma\left(n_{err} \right) \right| \right\} = \arg \max_{n_{err}} \left| \sum_{n=n_{err}}^{n_{err}+L'-1} r_n^* r_{n+N} \right| \quad (2)$$

Get the frequency offset at the same time as:

$$\Delta \hat{f} = \frac{1}{2\pi} \angle \gamma\left(\hat{n}_{err} \right) \quad (3)$$

After using symbols robust synchronous, the offset of remaining symbol can be expressed as $n_R = n_I + n_F$. Normally, symbol fine synchronous is used to adjust the integral part n_I , while the decimal deviation n_F would be compensated at the sampling clock synchronization part.

After symbol robust synchronization, because the residue frequency offset is low, so we assume approximately that the phase deflection caused by symbol synchronization error is in proportion to sub-carriers serial number and the synchronization error.

So the phase difference value between the K1 sub-carrier to the K2 sub-carrier in the same symbol as[5]:

$$\Delta\varphi_{k_1,k_2} = \varphi_{k_2} - \varphi_{k_1} = \frac{2\pi n_R(k_2 - k_1)}{N} = \frac{2\pi n_R \Delta k}{N} = \arg\left(Y_{l,k_2} c_{l,k_2} Y_{l,k_1}^* c_{l,k_1}^* \right) (4)$$

In the equation, $C_{l,k}$ denotes the transmitted frequency-domain signal, $Y_{l,k}$ denotes the outgoing signals from receiver after FFT operation. If K1,K2 is the number of the scattered pilot sub-carriers, then the above formula indicates the phase difference of scattered pilot in one symbol. Because the location of the pilot is known, then the symbol fine synchronous can be implemented by using the above formula[6].

At the beginning, we accumulate correlating pilot's correlation value, then calculate its phase:

$$\Delta \varphi = \arg \left[\sum_{n=1}^{N_{SP}-1} \left(Y_{l,k_{n+1}} c_{l,k_{n+1}} Y_{l,k_n}^* c_{l,k_n}^* \right) \right] \quad (5)$$

Then the symbol offset is calculated as:

$$\hat{n}_R = \frac{N\Delta\varphi}{2\pi\Delta k} = \frac{N}{2\pi\Delta k} \arg \left[\sum_{n=1}^{N_{SP}-1} (Y_{l,k_{n+1}} c_{l,k_{n+1}} Y_{l,k_n}^* c_{l,k_n}^*) \right] \quad (6)$$

N_{sp} denotes the number of scatter pilots. $\Delta k = 12$.

The timing diagram of symbol robust synchronization module simulated under Modelsim SE is shown in Figure.7. It can be seen from the figure that the abs_val_square is the modulus of sliding add result and the waveform is coincident with the result of MATLAB simulation. By analysing the signal waveform of MaxVal and MaxPos, it is can be observed that searching maximum is uninterrupted in the first OFDM symbol duration. This is the capturing phase of symbols robust synchronous, the tracking stage is taken at following. The stable value of MaxPos is 2525, it indicates that the maximum value of sliding add result appears on the NO.2525 sub-carrier. On the other hand, we are informed that the number of the first sub-carrier received at the receiver terminal is 35. These results are coincident with the accumulated offset of test data.
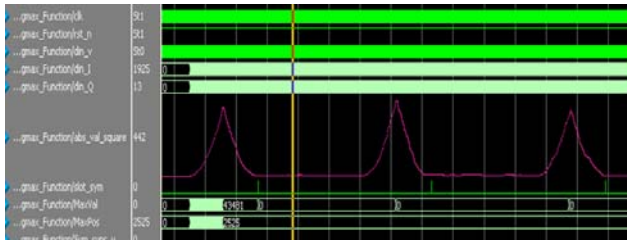

Figure 7. simulation waveforms of symbol robust timing synchronization module

As shown in Figure.8, when a OFDM symbol is over , the artan operation proceeds based on the sum of accumulated data. We estimate the integer offset of the symbol. The integer offset of the symbol of the test data is 35, so it is indicates that the symbol fine synchronization modular realize its function.
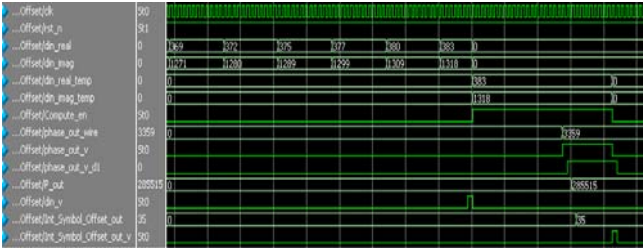

Figure 8. simulation waveforms of symbol timing fine synchronization

B. Carrier synchronization

The estimation and rectification of decimal frequency offset are completed in timing synchronization stage. At the same time, the estimation and rectification of integral frequency offset is proceeding in frequency domain.Integer frequency offset is defined as $C(m_{tr})$,which can be expressed as a formula as following:

$$C\left(m_{tr}\right) = \left| \sum_{k=0}^{N_{CP}-1} Y^{*}_{l-1,(p_k+m_{tr})_N} Y_{l,(p_{k+m_{tr}})_N} \right| \qquad (7)$$

N_{cp} and p_k indicate the number of continuous and the corresponding sub-carrier location. m_{tr} denotes cycle slip momentum. We are given that if the integer frequency offset equals to m_{tr} ,then $C(m_{tr})$ is sum of correlation accumulate of each pilot .Therefore,

$$\Delta \hat{f} = \arg \max_{m_{tr}} \left[C\left(m_{tr}\right) \right] \qquad (8)$$

The computational complexity of this kind of the estimation of integer frequency offset algorithm based on continuous pilot is high. In the DVB-T standard, there are 45 continuous pilots in 2K mode. If the detection range is ± 50 and all continuous pilots are occupied, the number of complex multiplication operation is as high as 4646 times. It is unbearable in practical application

According to DVB-T standard , the phase of transmitted continuous pilot is fixed, the quantity of pilotcorrelation result approximately equals to the multiple of single pilot frequency. It is worth noting that the size of multiple is the same with the number of continuous pilot. However, the data of non-pilot position do not have fixed phase, so the correlation result of phase is disordered which would cancel each other in the summation operator. Consequentially, correlation result of phase is minimum and the correlation result in pilot is more noticeable. Thus, the performance would not be promoted if only partial continuous pilot is employed.
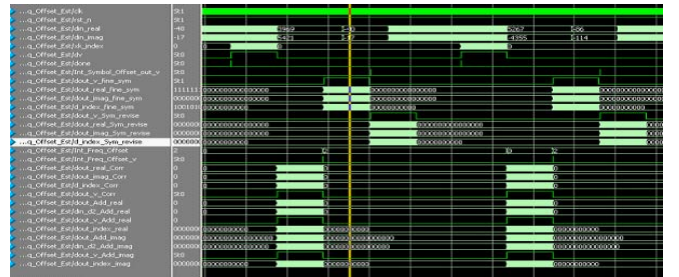

Figure 9. timing diagram of integer carrier frequency synchronization

Based on Frequency-Domain Maximum likelihood algorithm, this paper analyses the distribution of continuous pilot using 15 continuous pilots are, their number are: ：0、48、141、255、282、432、531、759、1261、1285、1393、1453、1483、1666、2047。

Timing simulation of integral frequency synchronization module in Modelsim SE is shown in figure9. Int_Freq_offset indicates the estimated integral frequency offset, Int_Freq_offset_v means effective signal. As can be seen from the figure, integral frequency offset is 2, which is coincident with the accumulated frequency error of test data.

IV. SYSTEM VERIFICATION AND CONCLUSION

A. System verification results

Debugging platform framework of this paper is shown in figure 10. In this test platform, we uses Virtex-5 SX50T FPGA chip by Xilinx company to simulate and verificate the algorithm and function of whole system .
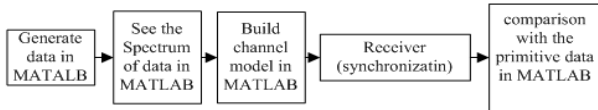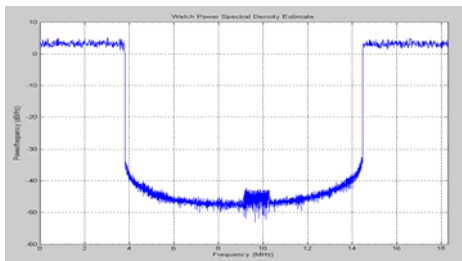

Figure 10. Debugging platform framework

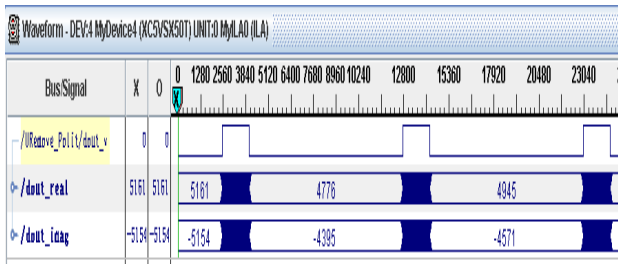Figure 11. The modulated signal spectrum diagrams

Figure 12. output waveform of Demodulator module running on the chip

Figure 11 is the the spectrum chart.After loading the design into this chip,we can capture the baseband modulator data and intercept it by the ChipScope which provided by Xilinx .Then import this data into MATLAB, as shown in figure 11 ,the spectrum chart shows that the actual modulation signal bandwidth is 7.61 MHz, conform to the DVB-T standard.

Also by the ChipScope Pro tools, we can capture the wave which output from DVB-T OFDM demodulator ,and show it in figure 12 .Figure 13 is the constellation chart of .DVB-T system output signal .

As it shown in figure 13 ,the synchronous module of DVB-T demodulator can basicly estimate and compensate the existential timing error and the carrier frequency offset.
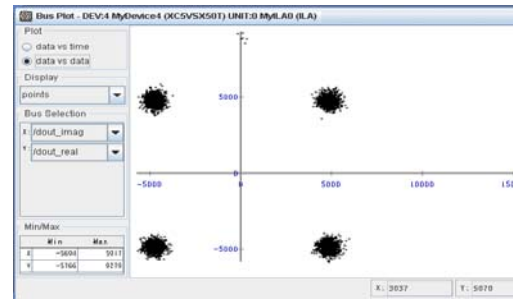

Figure 13. demodulator module output data constellation

B. Conclusion

This paper, based on the DVB-T standard,analysis the terrestrial digital broadcast system , reseaches on the coding modulation module in transmitter and the synchronization module in receiver. Contemporaryly,we give the key function module realization and the results in the physical layer based on FPGA.

Along with the promoting of the national digital television project and "three nets fusion" developments, in the present,digital television transmission play a important position in the new generation of television broadcasts market , digital TV receiver will also show a huge market demand.

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