A 2.4 GHz 1V Low Power LNA in Subthreshold Region

HangjiLiu[1, 2, 3],ZhiqunLi[1, 2],MengZhang[1]
[1]Institute of RF- & OE-ICs, Southeast University, Nanjing, 210096, China
[2]Key Laboratory of Jiangsu Province Sensor Network Technology, Wuxi, 214135, China
[3]College of Software Engineering, Southeast University, Suzhou 215123, China
Corresponding author: zhiqunli@seu.edu.cn

***Abstract*—**Thispaper presents the analysis and design of a 1V lowpower differential low noise amplifier (LNA) in 0.18 μm RF CMOS technology for 2.4 GHz WSN applications.The circuit benefits from subthreshold region and g_m-boosting techniques. These techniques provide a high gain andreducenoise figure (NF) and power consumption. The performance trade-off of thecircuit is discussed. Post simulation results have been shown and it exhibitsa 16.8dBgainwitha4.9dBNFwhiledissipating 0.9mW power from 1 V DC supply.

***Keywords*—**low noise amplifier (LNA); 1V; low power; subthreshold

I. INTRODUCTION

WIRELESS sensor network (WSN) standards like IEEE 802.15.4 require drastically low power consumption for remote applications with long battery lifetime.In order to achieve long battery life, the power consumption of the WSN receiver must be reduced and maintain an appropriate receiver sensitivity[1-4].

By applying subthreshold region and g_m-boosting techniques the supply voltage, current and NFcan be reduced.The aim of this paper is to design a 1V low power LNA.

Recently, CGLNA has become more attractive than CSLNA for its wideband input impedance matching. But compare with inductively degenerated common source (CS) LNA topology, thistopology has lower gain, so we choose CG cascade stage as the main topology of the circuit.

Besides, this topology has higher noise figure (NF) under 10 GHz [5], and the NF always has directly impact on the sensitivity of the RF receivers. But, in WSN applications, the nodes are always positioned not long distance, so the receivers do not have to achieve very high sensitivity. The robustness of the circuit, the DC supply voltage, the chip area, and the power consumption are key factors.

This paper is organized as follow: Section II discusses the circuit topology and gives the proposed LNA circuit. The relevant designed considerations of the proposed LNA are described in Section III. Section IV presents the post simulation results of the LNA. Finally, the paper concludes in Section V.

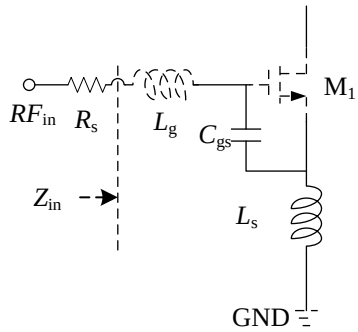

Fig. 1.Schematic of the basic CSLNA

II. TOPOLOGY DESIGN CONSIDERATION

The critical benchmarks for characterizing the performance of an LNA are NF, gain, power consumption, reverse isolation, stability, linearity, ease of input matching and matching accuracy usually relative to 50 Ω [6].The currently popular CSLNA topology is shown in Fig. 1, the input impedance at resonance to 50Ω [7]. Its input impedance can be expressed as

$$Z_{\text{in,CSLNA}} \approx sL_{\text{g}} + \omega_{\text{T}} L_{\text{s}} + sL_{\text{s}} + 1/sC_{\text{gs}} \qquad (1)$$

where$\omega_{\text{T}} = g_{\text{m}}/C_{\text{gs}}$is the unity current gain frequency of the M_1.It is hard to do the impedance matching at the inputs due to the interference of the circuit parasitic capacitance, the on-chip inductor modeling deviation, and so on. But an effective series resonance created at the RF operating frequency leads to a noiseless resistive input match, which accounts for the superior noise performance of the CSLNA configuration [6].

As stated in the Section I, it is easier for the CGLNA to doimpedance matching than the CSLNA,which without the influence of parasitic reactance. The input impedance of the CGLNA can be given by[8]

$$Z_{\text{in,CGLNA}} \approx \frac{R_{\text{D}}}{(g_{\text{m}} + g_{\text{mb}})r_{\text{o}}} + \frac{1}{g_{\text{m}} + g_{\text{mb}}} \qquad (2)$$

where$g_{\text{m}}$is the transconductance of the CG stage transistors, and R_{D} is the equivalent load connected to the drain of the MOS transistor. The antenna impedance is 50Ω. By adjusting the g_{m} and the R_{D}, it can obtain fully or partially resistive impedance that is less affected by parasitic reactance.The proposed LNA is shown in Fig.2.

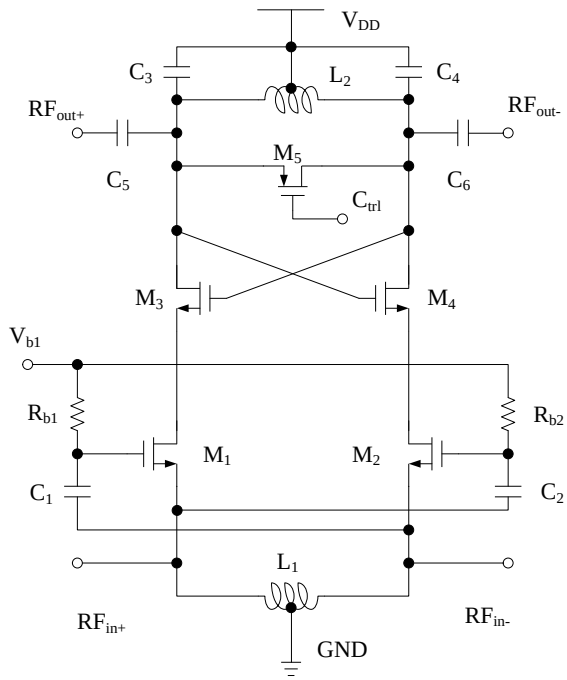

Fig. 2. Schematic of the proposed LNA

III. CIRCUIT DESIGN

A. Subthresholdregion

In reality, for V_{GS}approachesV_T (threshold voltage), a "weak" inversion layer still exists and some current flows from D (drain) to S (source). Even for $V_{GS}<V_T$, $I_D$is finite, but it exhibits an exponential dependence on V_{GS}. Called "subthreshold conduction," this effect can be formulated for V_{DS}greater than roughly 200mV as[8-9]

$$I_D = \frac{W}{L} I_{D0} \exp \frac{qV_{GS}}{nkT} \quad (3)$$

where$n$>1 is nonideality factor. The key factor here is that as V_{GS}falls below V_T, the drain current drops at a finite rate. With typical value of n, at room temperature V_{GS}must decrease by approximately 80mV for $I_D$to decrease by one decade, as shown in Fig.3[8].

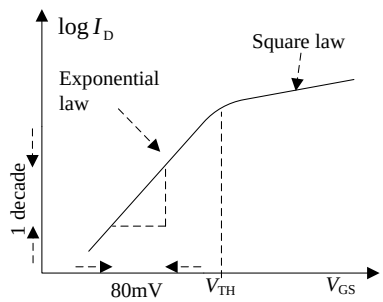

Fig. 3. Plot of drain current of V_{GS}

The exponential relationship between $I_D$and V_{GS} inthe subthresholdregion suggests the use of MOS transistors in this regime so as to achieve low drain current. As I_D decreases the power dissipation is lower.

B. Linearity

In most applications, the LNA does not limit the linearity of the receiver. Owing to the cumulative gain through the RX chain, thelatter stages, e.g., the baseband amplifiers or filters tend to limit the overall IIP_3or IP_{1dB}. We therefore design and optimizeLNAs with little concern for their linearity[10].

But subthreshold region and g_m-boosting techniqueshave been applied to reduce the current and noise at the same time, which can also increase the g_m related distortion and introduce extra distortion. Anestimation oftheg$_m$-boosted LNA IIP_3using IIP_3 andIIP_2 ofboth CGLNA and g_m-boosting CGLNA can be given by [11].

$$\frac{1}{IIP_3} = \frac{4}{IIP_{3-CG}{}^2} + \frac{1}{2IIP_{3-BOOST}{}^2} + \frac{3}{2}\frac{1}{IIP_{2-CG} \cdot IIP_{2-BOOST}} \quad (4)$$

The up-scaling of g_m-boosting CGLNA includes a noise-linearity trade-off since a high boosting gain is necessary for lowNF but leads to a degraded linearity performance. Fig.4 depicts the schematic simulated IIP_3.

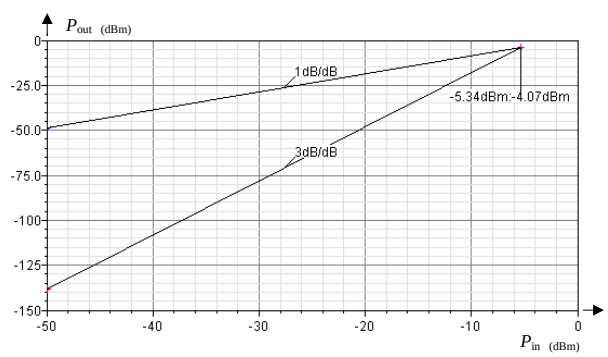

Fig. 4.IIP_{3dB}at low gain mode

C. Stability analysis

Given the positive feedback in the circuit, the stability must be investigated.The

small-signal impendence looking into the drain of M_1 is r_1 or M_2 is r_2. As M_1 and M_2 are identical, so $r_1=r_2=r$. The equivalent circuit of the positive feedback stage is shown in Fig. 5. The signals in M_3 and M_4 are a pair of differential signals, so the connections of r_1 and r_2 are equivalent virtual ground. The equivalent impendence Z_X from the drain of M_3 and M_4 can be written as

$$V_X = V_{gs4} + g_{m4}V_{gs4}r_2 + \left(-g_{m3}V_{gs3}r_1\right) - V_{gs3}$$
$$I_X = g_{m3}V_{gs3} = -g_{m4}V_{gs4}$$
$$Z_X = \frac{V_X}{I_X} = \left(1+g_m r\right)\frac{V_{gs4}-V_{gs3}}{g_{m3}V_{gs3}} = \left(1+g_m r\right)\left(-\frac{2}{g_m}\right) = -2\left(\frac{1}{g_m}+r\right)$$

(5)

whereg_{m3} is the transconductance of M_3, g_{m4} is the transconductance of M_4 . As M_3 and M_4 are identical, so $g_{m3} = g_{m4} = g_m$. But the positive feedback loop may lead the LNA to instability. As Z_L is the equivalent impendence of the LC parallel resonant network, we should keep Z_X <- Z_L to avoid oscillation. The result can be derived as follow.

$$\left.\frac{Z_X \cdot Z_L}{Z_X + Z_L}\right|_{Z_X<0, Z_L>0} > 0 \Rightarrow Z_X + Z_L < 0 \Rightarrow Z_X < -Z_L \qquad (6)$$

During the simulation, we should monitor the stability factor k-factor [10], whichindicates unconditional stability whenk_f> 1.Fig.6 shows the schematic simulated k_f.

$$k \approx \frac{1+\left|S_{11}\right|^2 - \left|S_{22}\right|^2 + \left|S_{11}S_{22} - S_{12}S_{21}\right|^2}{2\left|S_{12}S_{21}\right|} \qquad (7)$$

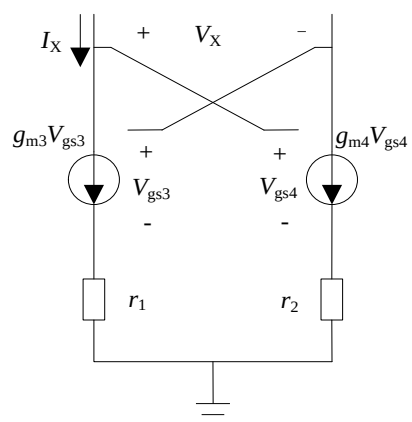

Fig. 5. Equivalent circuit of the positive feedback stage

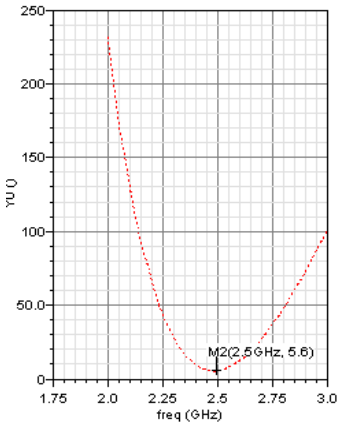

Fig. 6.k_f at high gain mode

IV. POST SIMULATION RESULTS

The layout of the LNA is shown in Fig.7. The total chip area is 950 μm×560 μm. The post simulated results of the LNA are shown as follow: S-parameterpost simulatedresults of the LNA are shown in Fig.8 and Fig.9 respectively. Noise figure and NFminare shown in Fig.10 and Fig.11. IP_{1dB}at high gain mode is shown in Fig.12 and at low gain mode is shown in Fig.13. Table 1 gives a summary of the post simulation results.

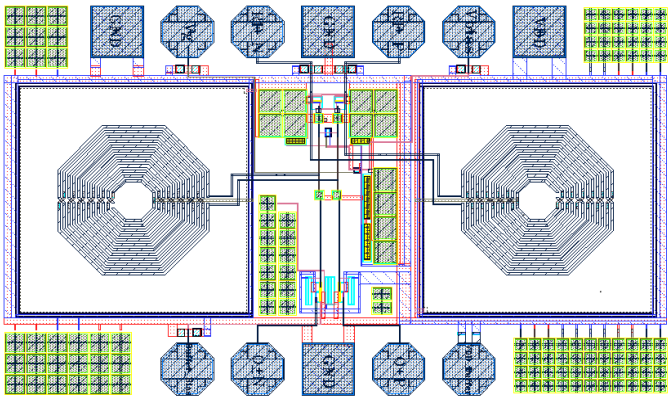

Fig. 7.Layout of the LNA.

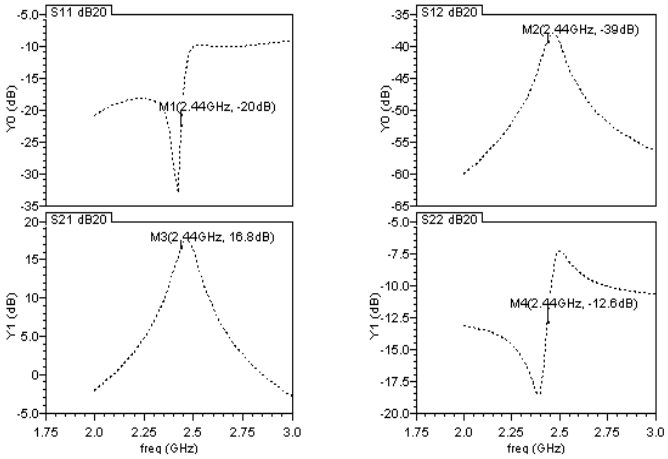

Fig. 8.S-parameter of the LNA at the high gain mode.

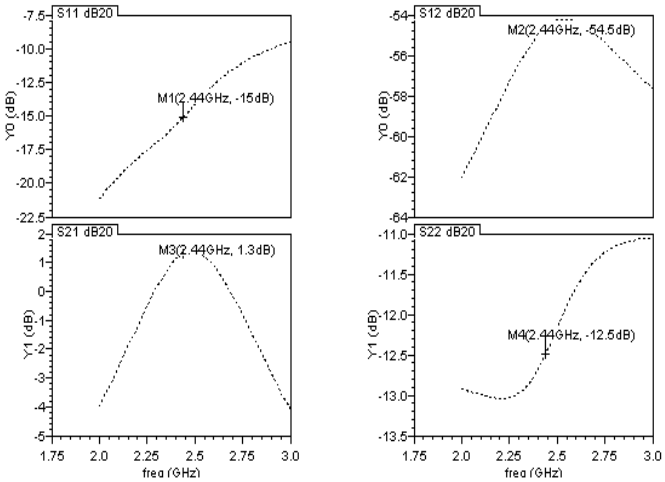

Fig. 9.S-parameter of the LNA at the low gain mode.

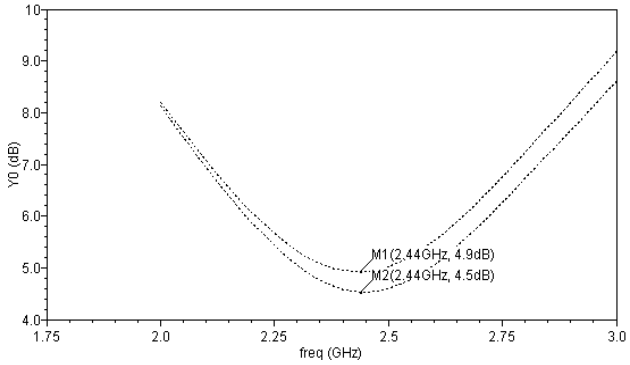

Fig. 10.NF and NFmin at high gain mode.

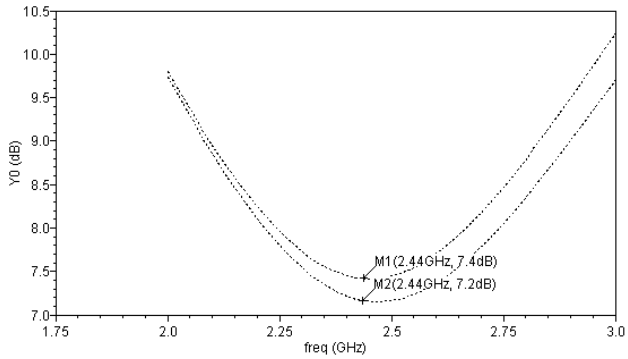

Fig. 11.NF and NFmin at low gain mode.

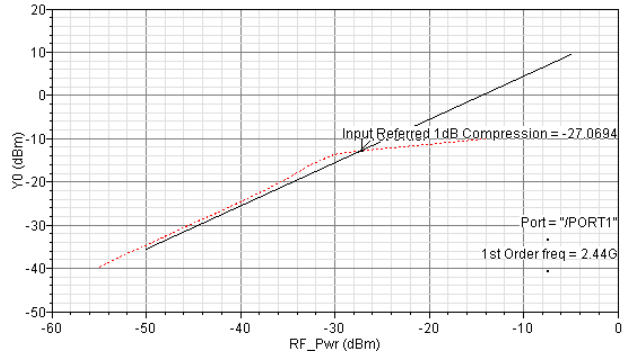

Fig. 12.IP1dB at high gain mode.

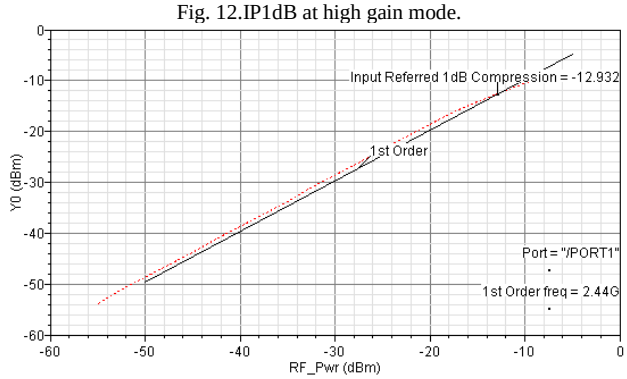

Fig. 13.IP1dB at low gain mode.

Table 1. Simulation Results of LNA

Parameter	Value
Supply voltage	1V
DC current	0.9 mA
Power consumption	0.9mW
S_{11}	<-10dB
S_{21} at 2.44 GHz	1.3-16.8dB
S_{22}	<-10dB
NF at high gain mode	4.9 dB
IP_{1dB} at low gain mode	-12.9dBm

V. CONCLUSION

In this paper, a1Vlow power low noise amplifier for wirelesssensor networks applications is presented. The LNA design makes use of subthreshold region and g_m-boosting techniques, in order to reducethe LNA's supply voltage and current. Trade-off between NF and linearity has been discussed. The LNA shows good stability as well as good robustness versus technologicalvariations. It achieves a power consumption of 0.9mW.

ACKNOWLEDGMENT

The authors would like to acknowledge the "National High Technology Research and Development Program of China" and "Special Fund of Jiangsu Province for the Transformation of Scientific and Technological Achievements" for the financial support.

REFERENCES

[1] T. Taris, A. Mabrouki, H. Kraimia, Y. Deval, and J.-B. Begueret, "Reconfigurable ultra low power LNA for 2.4 GHz wireless sensor networks," inProc. IEEE ICECS, Dec. 2010, pp. 74–77.

[2] Kluge W, Poegel F, Roller H, et al. A fully integrated 2.4-GHz IEEE 802.15.4-compliant transceiver for ZigBee applications. IEEE J Solid-State Circuits, 2006, 41(12): 2767.

[3] Camus M, Butaye B, Garcia L, et al. A 5.4 mW/0.07 mm2. 2.4 GHz front-end receiver in 90 nm CMOS for IEEE 802.15.4. WPAN standard. IEEE J Solid-State Circuits, 2008, 43(6): 1372.

[4] Zhang Hao, Li Zhiqun, Zhang Meng, et al. A 2.4 GHz low-IF RF frontend for wireless sensor networks. Microwave and Millimeter. Wave Technology (ICMMT), 2010: 225.

[5] Nguyen T K, Kim C H, Ihm G J, et al. CMOS low-noise amplifier design optimization techniques. IEEE Trans Microw Theory Tech, 2004, 52(5): 433.

[6] W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. Pineda de Gyvez, D. J. Allstot, and E. Sanchez-Sinencio. A capacitor cross-coupled common-gate low-noise amplifier. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 52, NO. 12, DECEMBER 2005.

[7] D. K. Shaeffer and T. H. Lee,"A 1.5-V, 1.5-GHz CMOS low-noise amplifier,"IEEE J. Solid-State Circuits, vol. 32, no. 5, pp. 745–759, May 1977.

[8] Razavi B. Design of analog CMOS integrated circuits. Xi'an: Xi'an Jiaotong University Press,2003.

[9] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 4th ed. New York: Wiley, 2001, ch. 1.

[10] Razavi B. RF Microelectronics 2nd. Bei Jing: PUBLISHING HOUSE OF ELECTRONICS INDUSSTRY,2012.

[11] I. R. Chamas and S. Raman, "Analysis, design, and X-band implementation of a self-biased active feedback g_m -boosted common-gate CMOS LNA,"IEEE Trans. Microw. Theory Tech., vol. 57, no. 3, pp.542–551, Mar. 2009.