Design of Class-D Power Amplifier for WSN Applications*

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Abstract: Wireless sensor networks (WSN) is a wireless network composed of a large quantity of stationary or mobile wireless sensors nodes. This paper presents a power amplifier (PA) design for Wireless Sensor Network (WSN) in the frequency band of 2.4GHz~2.4835 GHzbased on 0.18μm RF CMOS process. The structure of fully differential current-mode Class D PA was used in this circuit, and in order to save power dissipation, the power control technique was adopted. The off-chip inductors and capacitances are used to achieve output matching and there is also an off-chip balun at the output of PA. Post-simulation results show that the PA can get output power ranging from -3.83dBm to 5.09dBm with power added efficiency (PAE) ranging from 12.7% to 35.5%.

Key words:WSN; Current-Mode Class-D PA; power control; PAE

1. Introduction

As the development of the micro-electronics and wireless communication technology, CMOS RF transceiver chip with high integrity and low cost is being widely used in electronicequipment for industry and daily life, it has a huge potential market. Wireless Sensor Network(WSN) is a wireless network composed of sensor nodes with a wide application prospect inenvironmental monitoring, smart home furnishings and industrial production control and soon. Currently, it is a forefront hotspot of international concern. Therefore, it is of greatsignificance to research and design transceiver chip for WSN system.

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Since a wireless sensor network consists of many distributed sensor nodes which are typically deployed in remote or inaccessiblelocations, each node are expected to operate for years without replacing or recharging of the battery. Sensor nodes require a small, inexpensive, and highly integrated transceiver with low power consumption and high efficiency [1~3].The power amplifier (PA) is typically one of the mostpower hungry building blocks of an RF transceiver. It is thekey part of the RF front-end of a transmitter.

In this paper,we demonstrate a 2.4-GHz class-D PA based on 0.18μm RF CMOStechnology.Section 2 describes the design approach for the PA whichcovers the topology used and its advantages.Simulation resultsand layout of the proposed amplifier are given in section 3.Finally, the conclusion is summarized in section 4.

2.CircuitDesign

2.1 Selection of the Structure of PA

Switching-mode power amplifiers can potentially providehigh collector efficiency up to 100%. However, due to parasitic reactance, transition time,and turn-on resistance of the transistors, amplifier efficiencydegrades with increasing frequency. For instance, the class-Damplifier is very popular at lowaudio frequencies. However, it is hard to maintain this high efficiencyat RF frequencies because the output shunt capacitanceof the transistors causes significant loss[4].

The fundamental circuit and ideal voltage/currentwaveforms of a voltage mode class-D(VMCD) amplifier (sometimes referred to only as “class-D”)areshown in Fig 1(a) and Fig 1(b), respectively[4, 5].By driving two transistorsout-of-phase, the voltage across the transistors is a squarewaveform alternating between $V_{CC}$and zero.Ideally, sincethere is no overlap between voltage and current waveforms,efficiency of 100% can be achieved. However, if the transistorshave output shunt capacitance, this capacitance must be chargedor discharged to V_{CC}or ground. The resultant energy loss percycle $E_C$can be expressed as

$$E_C = \frac{1}{2} C_{DS} V_{DS}^2$$

where$C_{DS}$is the drain–source capacitance and $V_{DS}$is thedrain–source voltage when the transistor is turned on.Thisoutput capacitance lossbecomes the dominant loss

mechanism athigh frequencies starting at hundreds of megahertz.This is oneof the reasons that class-D is not a popular gigahertz amplifier[4, 5].

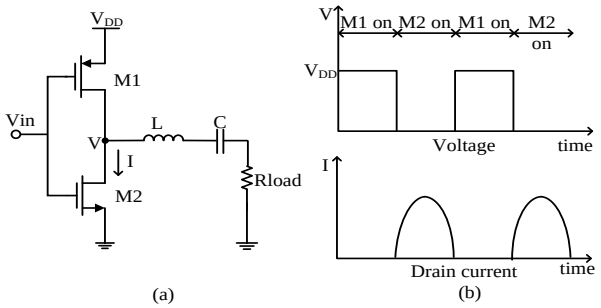

Fig. 1 VMCDcircuits and waveforms

(a)VMCDcircuit (b) Current and voltage waveform.

Fig. 2(a) shows thecurrent-mode class-D (CMCD) amplifier circuits and Fig. 2(b) showsthe ideal voltage/currentwaveforms. For the CMCD, we use currentsources instead of voltage sources, and the two switchingtransistors control the current instead of the voltage.There is aparallel-connected filter, with resonant frequency set to the carrierfrequency. Due to the filter resonance, there is no voltageacross the transistors at each switching time and so-called zero voltage switching(ZVS) is achieved. Even if the transistors have some output capacitance,the output capacitance can become part of the output parallelfilter; voltage waveforms are still as shown in Fig. 2(b).This ZVS feature is a key advantage of the CMCD architecture[5].

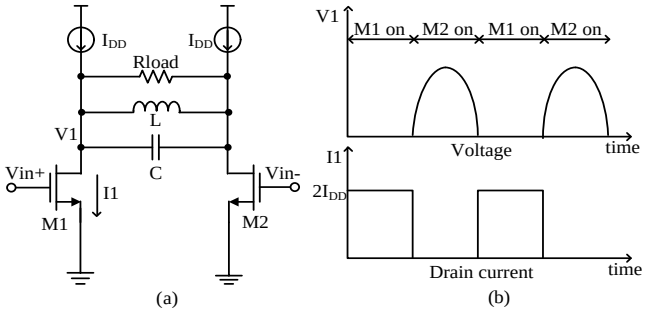

Fig. 2CMCDcircuits and waveforms

(a) CMCDcircuit (b) Current and voltage waveform.

2.2 Overall Circuit Structure

Power amplifier is an important part in radio frequencytransmitter of WSN system, which is located at the end of the transmitter system, used for amplifying the RF signal and transmitting it to the antenna. The signal delivered to the power amplifier is small, so driving stage is needed to amplify signals.

There are three unitamplifiers with different size in parallel to realize the control of output power. So the driving stage will be divided into two parts. The first part is the common driver stage and the second partisthree parallel driving stages with different size, driving three output amplifiers respectively.

The load network is used for impedance matching and filtering out high-order harmonics. In addition, the differential signal is converted into single ended signal by the load network. Theblock diagram of PA is shown in Fig. 3.

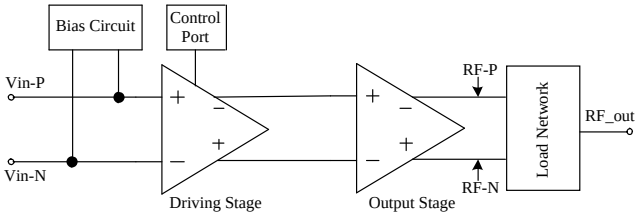

Fig. 3 Block diagram of proposed PA

2.3 Design of Driving Stage and Output Stage

For switch-mode power amplifier, the aim of thedriver stage is to generate a square wave in order to efficiently switch the output transistor. The more driving stages, driving ability is stronger, but at the same time, adding each additional stage will increase power consumption and degrade efficiency.

In conventional PA of high output power, efficiency is largely dominated by the output stage. But in a low transmit-power application such as WSN, the driving power and DC power consumption in the previous stage are no more negligible and severely degrade the overall efficiency. Therefore, in order to achieve high efficiency in a low transmit-power application, not only the output power stage, but also the driving stage needs to be co-optimized for low power operation. This design uses inverters to drive the input signal. Under the condition of meet the driving waveform requirements,minimize the number of driver

stageto reduce the consumption of the driver.

The output stage uses the CMCD circuit shown in Fig.2 (a). L、C and $L_{chock}$are implemented off the chip. The supply voltage of driving stage and output stage is different, so that you can control the output powerby controlling the supply voltage of the output stage. Thecircuit of driving stage and output stage is shown in Fig.4.

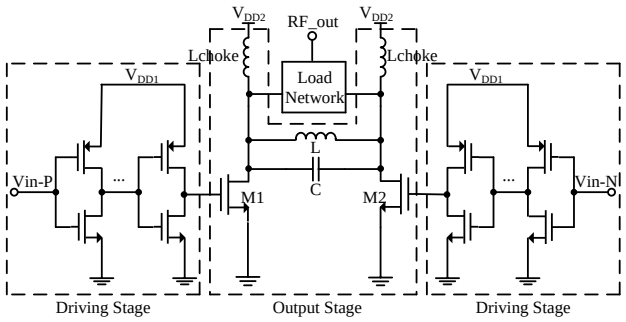

Fig.4 Driving stage and output stage of one unit amplifier

2.4 Design of Output Power Control

One important issue in the design is to implement the outputpower control which is often required in practical applications. The distancebetween one wireless sensor node and another communicatingnode is unfixed. Therefore, for longer battery life, we shouldtransmit signals of larger power when the distance is long andsignals of smaller power when the distance is short[6].

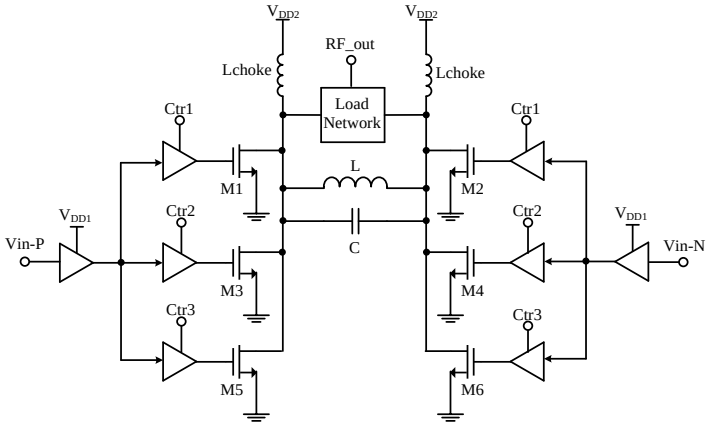

Fig.5 Implemented parallel-power amplifier.

Since the input signal provides only timing information in a class-D amplifier. The output power control can be realized through parallel amplification. The proposed architecture employs three unit amplifiers with same structure, the outputs of which are combined in a load network. The output power is changed by turn on/offeach individual unit amplifier.As a result, theoutput power can approximately make monotone changeswhen the control words (Ctr1, Ctr2, Ctr3) change from 001 to111 as shown in Fig. 5.

To widen the range of output power, another method implemented by this design to control the power is by alteringsupply voltage. There are two supply voltage values (V_{DD2}=1.8V or 1.3V) of the output stage.

2.5 Design of the Load Network

Fig. 6 shows the structure of the off-chip load network.Load network consists of two parts.The LCbalunconsists of C1、C2、L1 and L2, which converts the differential signal into a single-ended signal. L3、L4 and C4 compose a T-shape low-pass filter, which role is to filter out high-order harmonics andfulfill impedance matching. C3 and C5 are blocking capacitors.

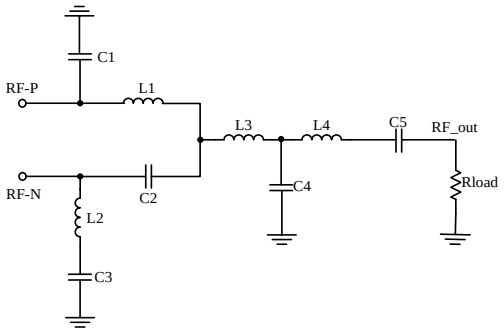

Fig. 6 The load network of PA

3. Layout and Simulation Results

The circuit is designed in a standard 6-metal layer, 0.18μm RF CMOS technology. Fig. 7 shows the layout of the power amplifier. The circuit occupies an area of 415×420μm ^{2}.Top is input and bottom is output. Control signals and observation points of bias voltage are located in the left and right parts.Fig.8(a)shows$P_{out}$and PAE of the class-D PA versus control words witha 1.8

V supply voltage at 2.44 GHz. A PAE of 35.5% is achieved with a -12dBm input power while delivering an output power of 5.09dBm, as shown in Fig. 8(a).As the supply voltage V_{DD2}become 1.3V, the output power and PAE versus control words as shown in Fig.8 (b). A PAE of 22.38% is achieved while delivering an output power of -0.64dBm, which can be used in a WSN system where a 0dBm output power is typically needed.

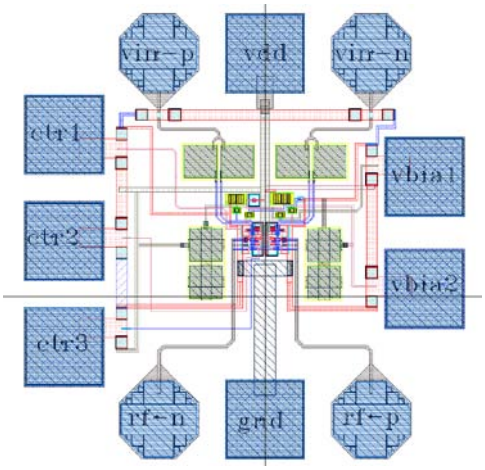

Fig. 7 Layout of the proposed Class-D PA

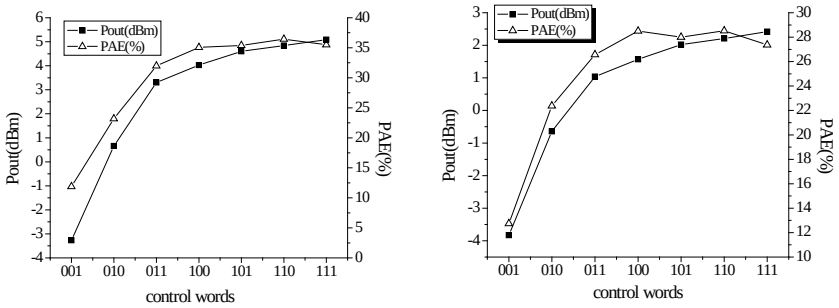

Fig. 8 Simulation results ofP_{out} and PAE versuscontrol words with

(a) 1.8 V supply voltage(b)1.3 V supply voltage

Table 1 shows thesimulation results of output power control. It is noteworthy thatall the data showed in the table are achieved when the inputpower is -12dBm.As you can see in the table 1, the output power in small step change, and cover the scope of 0dBm-5dBm.

Table 1 Simulation results of output power control

Control Words	V_{DD2}=1.8V		V_{DD2}=1.3V	
	P_{out}(dBm)	PAE(%)	P_{out}(dBm)	PAE(%)
111	5.09	35.50	2.42	27.37
110	4.84	36.44	2.21	28.52
101	4.60	35.40	2.02	28.00
100	4.03	35.07	1.57	28.50
011	3.30	31.98	1.04	26.57
010	-	-	-0.64	22.38
001	-	-	-3.83	12.74

4Conclusion

A class-D PA for WSN applications is presented, and a power controlmethod is proposed to achieve a maximum output power of 5.03dBm with a 35.5% PAE and a minimum of -3.83dBm with a 12.74% PAE. All the inductors used in the designs are off-chip. The proposed class-D PA shows the feasibility of using class-D PAs for low power applications.

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