

Design of Low Power Low Phase Noise 5-GHz Frequency Synthesizer for WSN Applications*

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Abstract: A fully integrated 5-GHz PLL frequency synthesizer for WSN applications has been designed and implemented on TSMC 0.18 μm RF CMOS process. In order to realize low power consumption, VCO adopted 6-bit switch resistors array which could provide varied biasing current by auto current calibration (ACC) circuit. Phase switching technique is also used in the frequency divider to reduce power consumption. In order to realize low phase noise, VCO is designed to have small gain and uses 4-bit switch capacitor array to provide wide tuning range. In order to reduce the locking time of PLL system, fast AFC is proposed. PFD is realized by the typical structure with TSPC dynamic D flip-flop. CP structure applying the replica technology is proposed. With a 1.8V supply voltage, the post-simulated minimum power consumption of the synthesizer is 6.4mW. Finally, the chip size of the frequency synthesizer is $1.11 \times 1.54\text{mm}^2$ with testing buffer and pads.

Key words: WSN; frequency synthesizer; ACC; low power; low phase noise; phase switching; fast AFC.

1. Introduction

Wireless sensor Network (WSN) is a wireless network composed of sensor nodes. With typical features of low cost, low power consumption and small size, WSN is now widely used in environmental science, traffic control, disaster prediction, and

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3. Circuit Design

3.1 VCO with ACC

The schematic of the LC-VCO is shown in Fig. 2. The VCO adopts complementary differential negative resistance structure. The cross-coupled pairs consist of NMOS transistors M1 and M2, and the PMOS transistors M3 and M4. They generate the negative resistance to cancel the loss of the LC tank. The inductor L is a differential symmetry circular inductor, with a higher quality factor of 10.2 at 5 GHz. A 4-bit switched capacitor array is adopted here to explore the tuning range. Reduce the size of variable capacitors to keep a low tuning gain K_{vco} which is around 100MHz/V.

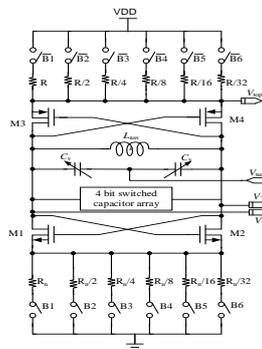


Fig. 2. Schematic of LC-VCO

The circuit of resistor biasing is simpler in structure and more flexible in power consumption control compared with the bandgap reference current biasing [2]. The bias current for VCO should be large enough to drive SCL divide-by-2. ACC circuit could select the proper working current to make SCL divider function well. As shown in Fig.1, a reference voltage V_{ref} is set to be compared with signal V_{top} which reflects the amplitude of the VCO output. In every clock period, the bias current of the VCO will be enlarged till $V_{top} \geq V_{ref}$. Thus, a proper VCO output swing could be set according to the sensitivity of the following divide-by-two stage and power consumption of the VCO could be minimized.

3.2 Frequency Divider

As shown in Fig. 1, the frequency divider basically consists of a 32/33 dual-modulus prescaler and a programmable pulse-swallow counter. The total

divide ratio could be set from 2400 to 2480, covering all required frequencies and the operating current of the whole programmable divider is 2.6mA.

Fig. 3 shows the block diagram of the 32/33 dual-modulus prescaler. Unlike traditional prescalers using synchronous counters at the first stage, the phase switching technique^[3] is used in this design to reduce power consumption as only the first divide-by-2 stage works at the highest frequency and each following stage works at a lower frequency. As shown in Fig. 3, a four bits circle counter is used to realize the phase switching function. After the reset signal, the initial state of the four flip-flops A, B, C, D is “1000” and one of the phase signals is selected. At the end of each prescaler counting cycle, the circle counter changes its state to select a 90° phase delayed signal, which is exactly one period of the input signal. Thus increased one counting is realized.

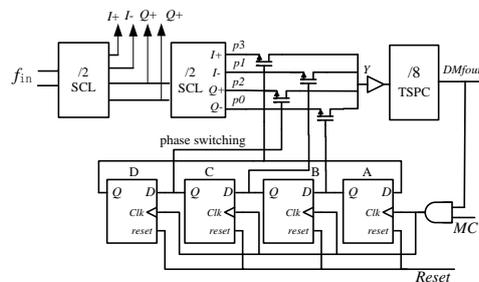


Fig. 3. Block diagram of 32/33 dual-mode prescaler

The first divide-by-2 circuit is realized by source-coupled logic (SCL) master-slave DFF^[4] with negative feedback to generate four quadrature outputs. By designing proper divider’s oscillation frequency and the amplitude of the input of the clock, SCL could function well. This circuit integrates three functions: 1) buffer of VCO; 2) to generate quadrature outputs for mixers; 3) part of the prescaler. Traditional design may use another separate divide-by-2 which is out of PLL to generate quadrature outputs; in this design, the divide-by-2 is integrated inside of PLL to reduce power consumption. Also its good input sensitivity makes it possible for VCO to save a significant amount of bias current.

3.3 Fast AFC

The schematic of fast AFC is shown in Fig. 4. AFC circuit is designed by counter-based methods. By using the high-frequency signal which is the output of dual modules prescaler as the clock input of the counter and the low-frequency

signal which is the reference signal of PLL frequency synthesizer as the enable signal, comparing the count value of the two counters and controlling the switch with binary search algorithm, the fast AFC is realized.

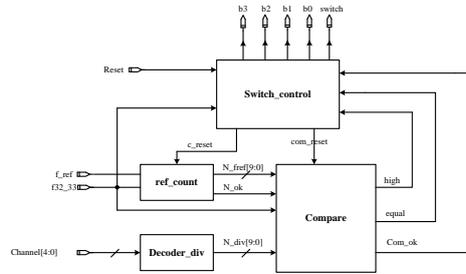


Fig.4. Schematic of fast AFC

The working process of AFC: 1) Set the channel and reset the circuit; 2) Count the value at the rising edge of clock input when the enable signal has a high level. Stop counting value when the enable signal has a low level. 3) Compare the count value of the counters and output the control switch code by an optimized algorithm. Then reset the counters and repeat the second process. 4) Output equal signal and AFC is locked.

3.4 PFD and CP

Two important modules in PLL synthesizer, PFD and CP are discussed in this part. A typical PFD structure with TSPC (true single phase clocking) dynamic D flip-flop has been presented in this paper, which has low power cost, high speed and simple structure. Meanwhile, the optimization of PFD reset delay overcomes the dead-zone and expands the detecting region. The schematic of PFD is shown in Fig. 5.

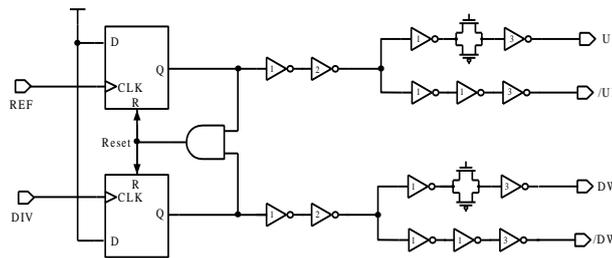


Fig.5. Schematic of PFD

Besides, a novel CP structure applying the replica technology is proposed. In

this design, the rail-to-rail operational amplifier guarantees the high current matching precision and enlarges the output voltage region as well. Moreover, controlling the current partly is employed to enhance the CP operational speed and current matching precision. The schematic of CP is shown is Fig. 6.

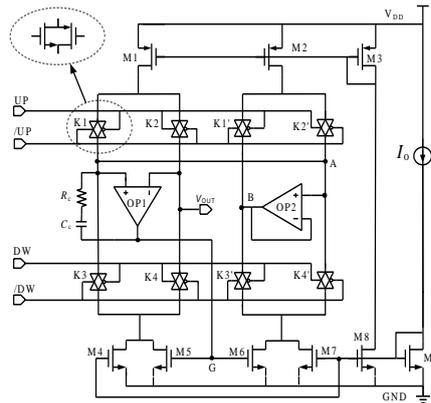


Fig.6. Schematic of CP

4. Layout and Post Simulation Results

Layout of the proposed frequency synthesizer, designed with TSMC 0.18 μ m RF CMOS technology in Cadence Virtuoso environment is shown in Fig.7. The area of the frequency synthesizer including I/O pads and ESD protection circuits is 1.11mm \times 1.54mm.

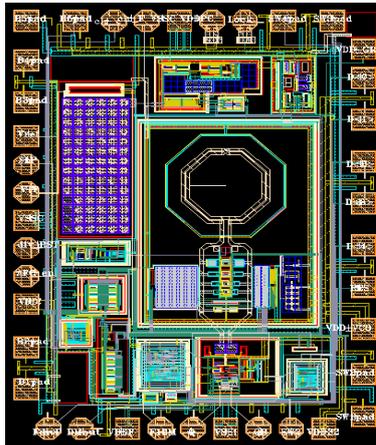


Fig.7. Layout of frequency synthesizer

With 1.8V voltage supply, post simulation of each part in the PLL system is done under the temperature of 27 degrees with Specter RF tool in Cadence. Fig.8.

shows post simulation of VCO tuning range which is from 4.5GHz to 5.5GHz. The phase noise of VCO is $-117\text{dBc/Hz}@1\text{MHz}$ at frequency of 5GHz and the operating current of the VCO is from 0.34mA to 3.3mA. Fig.9. shows post simulation of the prescaler output and the whole programmable divider output. Fig.10. shows post simulation of current mismatch of the proposed CP. The percentage error of current mismatch for the output range from 0.3V to 1.7 V is less than $\pm 0.005\%$. Post simulated results of AFC shows the time of frequency calibration is about 16 μs . The transient simulation of the output of the frequency synthesizer is shown in Fig.11. The minimum current consumption of the whole system is only 3.6mA.

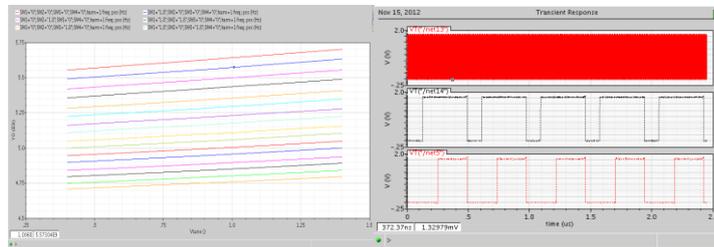


Fig.8. VCO tuning range **Fig.9.** Prescaler output and divider output

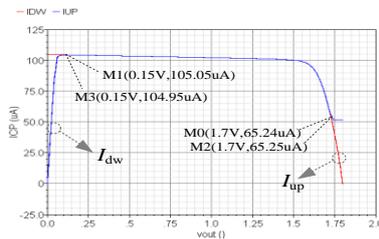


Fig.10. Current mismatch of CP

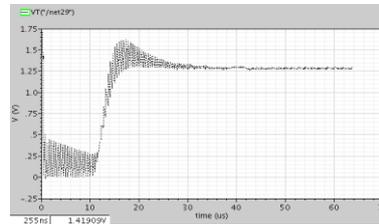


Fig.11. Transient output of frequency synthesizer

Table 1 summary the measurement results along with recent 5GHz synthesizers for comparison.

Table 1 Comparison of Other Published 5 GHz Synthesizers

Specification	[5]	[6]	[7]	This work
Process (m)	0.18	0.18	0.18	0.18
VDD (V)	1.0	1.8	1.8	1.8
Ref. Freq. (MHz)	20	5	2	2
Phase noise(dBc/Hz)	-96.3	-117	-118	-114
Power (mW)	29.9	35.5	19.8	6.4

5. Conclusion

A low power 5-GHz PLL frequency synthesizer for WSN applications has been implemented in 0.18 μ m CMOS technology. Automatic current calibration and phase switching techniques are used to reduce power consumption. The oscillation frequency of VCO is twice of the channel frequency, and IQ signals are generated by a divide-by-two frequency divider which is also part of the frequency divider. Simulation results show that the designed frequency synthesizer consumes a power of 6.4mW under 1.8V voltage supply.

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