# A Wideband Variable Gain Amplifier Design for 60GHz Millimeter-wave Receiver\*

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**Abstract:**This paper presents a wideband variable gain amplifier (VGA) applied to 60GHz millimeter-wave receiver with an operating frequency from DC to 1.08GHz and variable gain range from 0dB to 60dB. The entire VGA consists of an 8dB fixed gain stage, a 0~48dB coarse gain control stage, a 0~12dB fine gain control stage and an output buffer stage. Both the coarse gain control stage and the fine gain control stage adopt open loop amplifier with local feedback. The feedback capacitors are added to compensate the bandwidth of the circuit. The VGA circuit is designed in TSMC 65nm CMOS process. The post simulation results show that: the operating current of the entire VGAwith testing buffer is 20mA. The 3dB bandwidth is larger than 1.4GHz. The OP<sub>1dB</sub> at 0dB gain is 0 dBm. The whole chip area is 1.5×0.6mm<sup>2</sup>.

Key words: Variable gain amplifier • Wideband • Feedback.

#### 1. Introduction

With the development of multimedia applications, wireless communications require increasing transmission rate and signal bandwidth, demanding the study of 60GHz wireless communications. Since 2000, many countries opened near 60GHz continuous spectrum resources for high-speed wireless communications research and applications. Continuous 5~7GHz of unlicensed spectrum resources greatly stimulated the research and open process of 60GHz wireless communications<sup>[1-2]</sup>.

RFsignals received from the antenna have large amplitude variation. In order to make these different signal amplitudes get the correct demodulation, RF

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receiver chips usually use a variable gain amplifier (VGA) to achieve gain controlling, the control signals of VGA are from the baseband digital signal processor. The VGA is required to adjust the amplitude of the received signal depending on the signal level so as to keep almost constant signal level at the ADC input [3].

This paper presents a wideband VGA with an operating frequency from DC to 1.08GHz, variable gain range from 0dB to 60dB, 2dB gain step, 50 ohms outputresistance. The total current consumption is 20 mA.

#### 2. VGA Structure

Fig.1shows the block diagram of the whole VGA. The VGA includes an 8dB fixed gain stage, a  $0\sim48$ dB coarse gain control stage, a  $0\sim12$  dB fine gain control stage, and an output buffer stage. The  $0\sim48$ dB coarse gain control stage consists of 4 amplifiers, each providing 0dB/12dB gain. The fine gain control stage achieves a gain range of  $0\sim12$ dB with 2dB gain step. The output buffer provides a  $50\Omega$  output resistance to drive the input impedance of high speed ADC. Each stage of the VGA system is AC coupled.

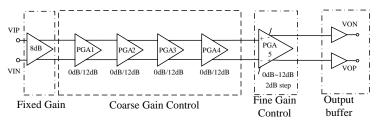


Fig.1 Block diagram of the proposed VGA

# 3. Circuit Design

#### 3.1 8dB Fixed Gain Stage

The schematic of the 8dB fixed gain stage is shown is Fig.2.

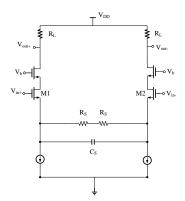


Fig.2Schematic of the 8dB fixed gain stage

The main purpose of the 8dB fixed gain stage is to compensate the gain loss of the output buffer. The topology of the 8dB fixed gain stage is a cascade amplifier with source degeneration. The feedback resistor  $R_{\rm S}$  can improve the linearity and the feedback capacitor can increase the bandwidth. But pay attention that a too large  $C_{\rm S}$  could make the circuit unstable.

## 3.2 Amplifier Design for Coarse Gain Control Stage

Four same amplifiers are cascaded to form the coarse gain control stage. The topology of the amplifiers is shown as Fig.3. The amplifiers use open loop structure with local feedback<sup>[4]</sup>. Compared to the closed loop structure with operational amplifier, Open-loop amplifiers are suitable for low power and broadband applications <sup>[5]</sup>. The input stage of the circuit is a transconductance amplifier which converts the input voltage into small signal current. The small signal current is copied by the current mirror and converted to voltage by the output stage. For this circuit different gain can be achieved by changing  $R_S(R_{S1})$  in parallel with  $R_{S2}$  or  $R_L$ .

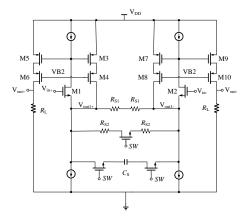


Fig.3 Schematic of amplifiers in coarse gain control stage

Compared to the closed loop structure using operational amplifier, the open loop amplifier has a lower loop gain at low frequency so that the linearity is worse and the gain is less accurate. But the open loop amplifier has following advantages: 1) the output of the previous stage circuit is connected directly to the gate of the input transistor of next stage, so that the previous stage has a small load capacitance. 2) The open loop amplifier has a relatively simple topology which can achieve a larger bandwidth with smaller power consumption. 3) The circuit has less active components and is likely to achieve better noise performance.

The following is the analysis of the circuit<sup>[6]</sup>. The input stage (M1, M2) can be seen as a source follower. The voltage gain of the input stage can be expressed as:

$$A_{V1} = \frac{V_{\text{out1+}} - V_{\text{out1-}}}{V_{\text{in+}} - V_{\text{in-}}} = \frac{Tg_{\text{m}}R_{\text{S}}}{1 + Tg_{\text{m}}R_{\text{S}}}$$
(1)

Where  $g_m$  is the transconductance of the input transistor, T is the additional loop gain of the local feedback. If  $g_m$  and T are big enough, the voltage gain of the source follower is close to 1.

The small signal current generates an output voltage over  $R_L$ , so the gain of the whole circuit is:

$$A_{\rm V2} = \frac{\rm V_{out^{+}} - \rm V_{out^{-}}}{\rm V_{in^{+}} - \rm V_{in^{-}}} = \frac{R_{\rm L}}{R_{\rm S}} \frac{Tg_{\rm m}R_{\rm S}}{1 + Tg_{\rm m}R_{\rm S}} \approx \frac{R_{\rm L}}{R_{\rm S}}$$
(2)

The circuit gain is closer to the ratio of resistors due to the local feedback, which increases the gain accuracy and linearity.

When the switch signal SW is set to low level, the feedback resistor is large and the circuit gain is 0dB. When the switch signal is set to high level, the feedback resistor is small and the circuit gain is 12dB. At the same time the feedback capacitor  $C_S$  is also connected in the circuit to improve the bandwidth.

## 3.3 Amplifier Design for FineGain Control Stage

The schematic of the amplifier in coarse gain control stage is shown is Fig.4. This circuit is similar to the topology in Fig.3, with more feedback resistors and switches. And more capacitors are added to keep the gain flat at each gain step. This stage achieves a gain range from 0dB to 12dB with 2dB step size.

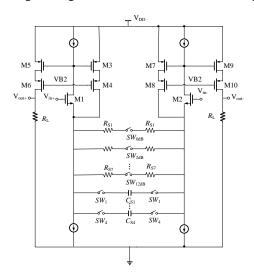


Fig.4 Schematic of the amplifier in coarse gain control stage

## 3.3 Output Buffer

Two source followers are used to achieve 50 ohms output resistance.

# 4. LAYOUT AND SIMULATION RESULTS

The layout of the proposed VGAdesigned with TSMC 65nmCMOS technology in Cadence Virtuoso environment is shown in Fig. 5. The area of the total VGA including pads is  $1.5\times0.6$ mm<sup>2</sup>.

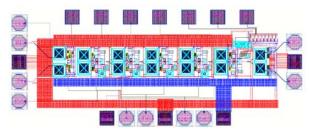


Fig.5Layout of variable gain amplifier

Using Cadence Spectre simulation tools, the post simulation is run under TT corner, temperature 27°C. The post simulation result shows that the working current of VGA is 20mA. The amplitude frequency characteristic curves at 7 different gain steps are shown as Fig.6. The bandwidth of VGA is up to 1.4GHz.

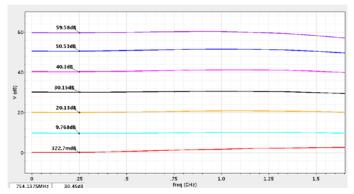


Fig.6 Post simulation results of amplitude frequency characteristic curve of VGA

Fig.7 shows the overall VGA gain at different digital control words for 250MHz signal.

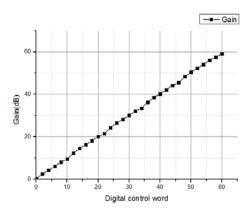


Fig.7 Post simulation results of gain at different control word of VGA

Post simulation of noise figure at 60dB gain is shown as Fig.8. The NF is large at frequencies below 10MHz due to flicker noise. The NF is below 16.6dB at frequencies from 10MHz to 1.08GHz.

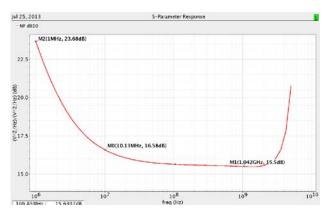


Fig.8 Post simulation of noise figure at 60dB gain

The post-simulation result of output 1dB compression point at 0dB gain is shown as Fig.9. The output 1dB compression point at 0dB gain is 0dBm.

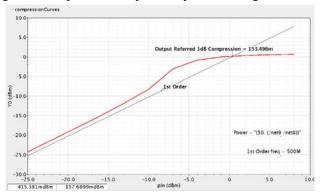


Fig.9Post simulation result of output 1dB compression point at 0dB gain

Table 1is the summaryof the post simulation results of the proposed VGA.

Table 1Summary of the VGA post-simulation results

Technology	65nm CMOS
Supply Voltage	1.2V
Gain Range	0-60dB
Gain step	1.4-2.86dB
$OP_{1dB}$	0dBm@0dB gain
NF	16.6dB@60dB gain
Current dissipation	20mA

#### 5. Summary

A wideband variable gain amplifier for 60GHz millimeter-wave receiver has been implemented in 65nm CMOS technology. The whole VGA circuit consumes 20mA current under 1.2V supply voltage. Simulation results show that the bandwidth can be up to 1.4GHz and the variable gain range is from 0dB to 60dB with 2dB step. The noise figure is below 18.8dB from 10MHz to 1.08GHz at 60dB gain. The output 1dB compression point is 0dBm at 0dB gain.

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