Design of 2-3.5GHz Transmitter Front-End

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Abstract. This paper provides a design of 2-3.5GHz transmitter front-end based on 0.18μm RF CMOS process. The front-end circuits consist of IF single-differential converter (SDC), LO SDC, up-conversion mixer and an output buffer for testing. Under 3.3V power supply, the post-simulation results indicate that the current consumption is 38.3mA, IP1dB is 0dBm, the voltage gain at 2-3.5GHz is 4.7-3.1dB, and NF is lower than 14.5dB.The front-end design has been applied in the 2-3.5GHz transmitter and meets the requirements of system application.

Key words: Cascode Balun· cross-coupling technology· Gilbert mixer

1. Introduction

The phased array radar has been widely used in military with the changes in international situation and development of science and technology. The critical technology of this radar is the T/R modules. Thousands of these T/R modules are assembled in large scale active phased array radar, which account for 60% cost of the whole radar system [1]. In consequence, the performance of the T/R modules has significant influence of the active phased array radar system.

In addition, the radar system is directly related to the structure of the T/R modules. For a large radar system with thousands of T/R modules, the weight of the arrays will be reduced significantly if the weight of T/R modules could be lowered a little effectively. And the volume of the T/R modules has strong restriction on the array layout.

The designed front-end is used in the T/R module of a phased array radar, the key performance indicators of which are linearity, voltage gain, NF (noise figure), input/output VSWR (voltage standing wave ratio) in the design process.

2. Circuit Design

In the transmitter front-end, the 400MHz single-ended IF (intermediate frequency) signal is up-mixed to 2-3.5GHz single-ended RF (radio frequency) signal, when the frequency of the input LO (local oscillator) signal is ranging from 2GHz to 3.5GHz with the frequency of the output RF signal, and the power of the input LO signal is 0dBm. The designed circuits transfer the single-ended IF and LO signals to the differential before up-mixing the IF signal to the RF band. Figure 1 shows the block diagram of 2-3.5GHz transmitter front-end, whose core modules are IF SDC, LO SDC circuit and the up-conversion mixer. And the output buffer is used for impedance matching as testing needs.

The proposed front-end for 2-3.5GHz transmitter is fabricated by a 0.18μm RF CMOS process and the power supply voltage is 3.3V.

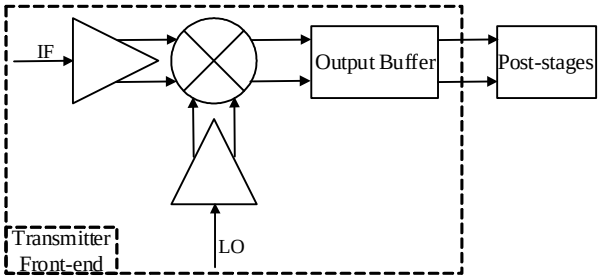


Fig. 1 Block diagram of 2-3.5GHz transmitter front-end

2.1 IF SDC & LO SDC

The IF and LO input ports need to build 50Ω impedance matching as required. There are various methods to achieve 50Ω impedance matching, such as the resistance network, the reactance network and the common-used amplifiers. The resistance network has wide broadband use, which brings inevitable noise and loss

however. The reactance network has small noise and loss, but it is usually applied in narrow-band situation [2]. In consideration of both noise and bandwidth, the amplifier structure is chose. Figure 2 shows the cascode balun structure for IF SDC and LO SDC circuit, which implements 50Ω impedance matching and output differential signal.

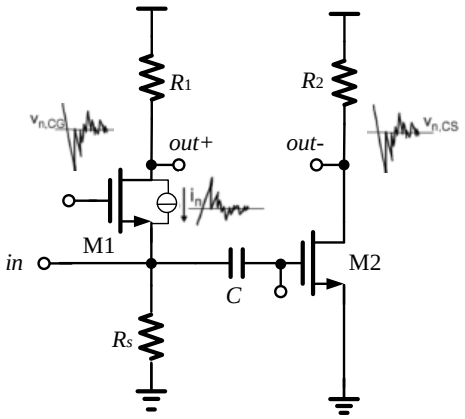


Fig. 2 Cascode balun structure for IF SDC circuit

The common-gate input transistor M1 generates two equal voltages in the two branches, which means the noise generated by M1 is canceled in the output end [3].

On the premise of satisfying system performance, the IF SDC and LO SDC ought to be of high gain and low noise as the first stage circuit in the transmitter, which helps reduce the system noise. Figure 3 shows the schematic of IF SDC circuit. Common gate transistors M3 and M4 are cascaded in the cascade balun with capacitance cross coupling technology to implement feed-forward cross coupling. The channel noise generated by M2 is reduced without increasing transconductance of M2.

Figure 4 shows the LO SDC circuit with the cascode balun structure. The source inductor *L*s is used to replace *R*s in Figure3, which is meant to reduce noise but occupies larger layout area.

In Figure 4, body cross coupling technology is used as the bodies of the transistors M1 and connect to the source of each other. In this way, the input transconductance of LO SDC circuit is improved without extra consumed current.

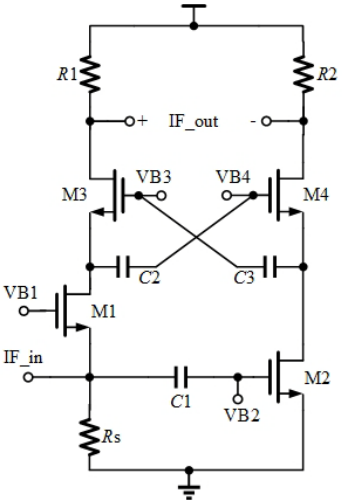


Fig. 3 Schematics of IF SDC

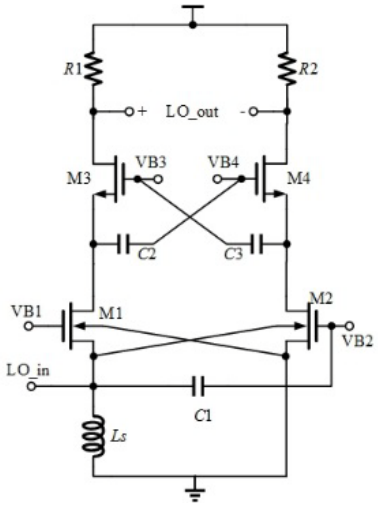


Fig. 4 Schematics of LO SDC

With the improvement of input transconductance, voltage gain of LO SDC circuit is increased and noise is reduced.

2.2 Up-conversion Mixer

Mixer is mainly divided into two categories, active mixer and passive mixer. In active mixers, Gilbert mixer is widely used for its high input impedance, good LO suppression and easy integration [4]. Figure 5 shows a Gilbert double-balanced mixer used as the up-conversion mixer circuit.

Frequency conversion is realized in the Gilbert double-balanced mixer shown in Figure 5. The switch level (M1-M4), driven by LO signal, modulates the current generated by the transconductance level (M5, M6). In the load level, load resistors (*R*1, **R**2) transfer the RF current signal to voltage signal. The bias current of the mixer circuit is supplied by the transistors (M7, M8).

To improve the linearity performance, the negative feedback resistor R0 is connected in the sources of the transconductance level, shown in Figure 5. From the perspective of single-end circuit, the linearity performance of the up-conversion mixer circuit is improved, while the conversion gain is reduced.

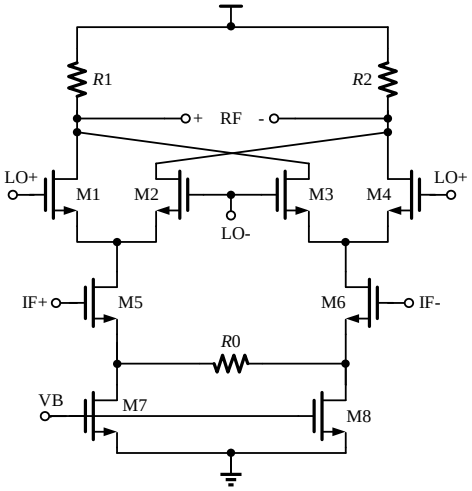


Fig. 5 Gilbert double-balanced mixer

2.3 Output Buffer

In the designed transmitter front-end, the output impedance of up-conversion mixer is in a high quantity. To be measured on the 50Ω impedance equipment, an output buffer is designed in the output end of up-conversion mixer to build 50Ω impedance matching. The output buffer has simple structure and it is not applied in the 2-3.5GHz transmitter system chip. The schematic is shown in Figure 6.

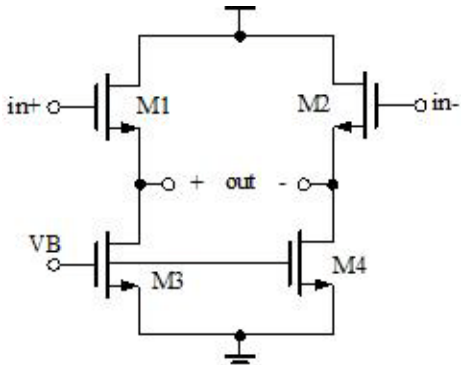


Fig. 6 Schematic of output buffer

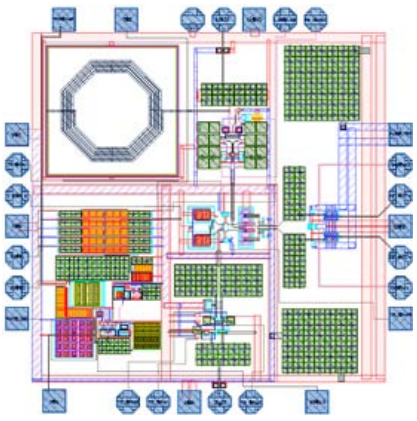


Fig. 7 Layout of transmitter front-end

3. Layout Design and Simulation Results

3.1 Layout Design

The layout of the transmitter front-end is designed from the view of S-band transmitter system chip. And the current density, matching performance and parasitic parameter are important factors that need considered. Figure 7 shows the layout of S-band transmitter front-end. It is designed in 0.18μm RF CMOS process.

3.2 Simulation Results

In Cadence software platform, the performances of the transmitter front-end are simulated including working current, linearity, voltage conversion gain, NF and port matching.

1. Working current

The transmitter front-end (except output buffer) consumes 38.3mA current and the output buffer consumes 32.0mA current.

2. Voltage conversion gain

Figure 8 shows the voltage conversion gain of the transmitter front-end (except output buffer). The IF frequency is fixed at 400MHz. The LO frequency ranges with the output RF frequency from 2GHz to 3.5GHz and its power is 0dBm. As described in Figure 8, the voltage conversion gain in the output band of 2-3.5GHz is 4.7-3.1dB.

3. NF

Figure 9 shows the NF of the transmitter front-end, which is lower than 14.5dB when RF frequency is 2-3.5GHz.

4. Linearity

Figure 10 shows the input referred 1dB compression curves of the front-end when the RF frequency is 2.4GHz and 3.2GHz, respectively. The IP1dB is described as 0dBm.

5. Port matching

Figure 11 shows VSWR of IF, LO and RF ports, and they are all less than 1.8.

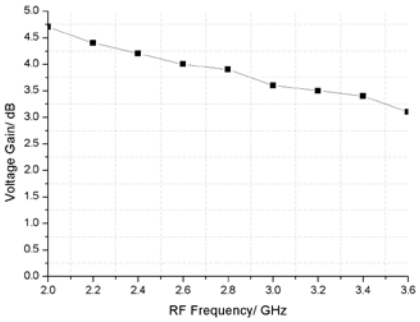


Fig. 8 Voltage conversion gain

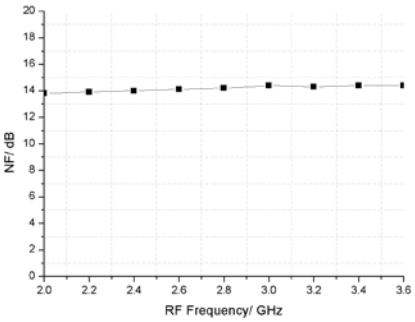
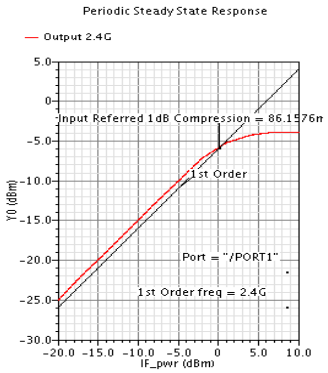
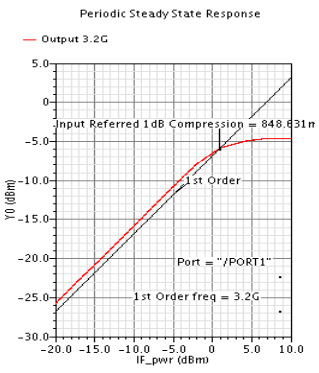


Fig. 9 NF



(a) RF@2.4GHz.



(b) RF@3.2GHz.

Fig. 10 IP1dB

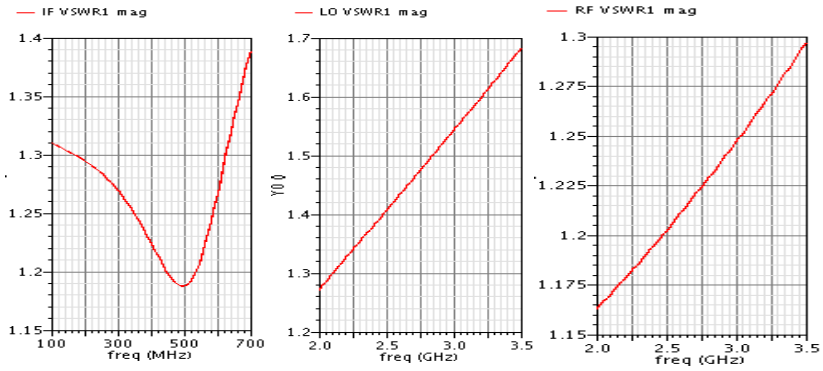


Fig.11 VSWR of IF, LO and RF ports

Based on the post-simulated results, the performances of the 2-3.5GHz transmitter front-end is shown in Table 1.

Table 1 Performances of 2-3.5GHz transmitter front-end

Performance Index	Simulated Value
Working Current（except output buffer）/ mA	38.3
IP1dB/ dBm	0
Voltage Conversion Gain/ dB	4.7-3.1
NF/ dB	<14.5
VSWR	<1.8

4. Conclusions

The 2-3.5GHz transmitter front-end is designed in 0. 18μm RF CMOS process and used successfully in the 2-3.5GHz transmitter system chip. The designed front-end satisfies the performance requirement of the transmitter system including up-conversion mixing, amplifying, etc. The shortcoming of the front-end is high power consumption, which could be reduced further more.

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