Design of Reconfigurable Low-passFilter for 60GHz Wireless Communication*

Keyuan Liao^{1,2}, ZhiqunLi ^{1,2+}, Qin Li¹, Zhigong Wang¹

¹Institute of RF- & OE-ICs, Southeast University, Nanjing, 210096;

²School of Integrated Circuits, Southeast University, Nanjing, 210096;

⁺Corresponding author: zhiqunli@seu.edu.cn

Abstract: A third-order Chebyshevlow-pass filter, using Gm-C structure, based on Nauta's OTA, is presented. The filter is designed for 60GHz wireless communication using 65nm CMOS process and 1.2V power supply. The cutoff frequency of the filter is required to be tuned from 1GHz to 5GHz.UsingNauta'stransconductance characteristics, the filter can be operated at ultra-high frequency band and has a high linearity and wideband frequency. From the results of the post-simulation, the cutoff frequency of the filter can be tuned from 631MHz to 5.027GHz. The gain in the pass band is nearly 2dB in high impedance. The adjacent channel rejection is about 26dB. The ripple in pass band is about 1.1dB.

Key words: 60GHz Wireless communication; Nauta's OTA; Gm-C filter

1 Introduction

The availability of the 57-66GHz band for short-range,highdata rate wireless communication has fueled a lot ofresearch to make CMOS integration possible. Several standards have been developed such as the IEEE 802.15.3c and the Ecma387 standard. When using one of the four 2.16GHz channels in the 57-66GHz band, the data rate can reach 3Gbit/s^[1]. Also, the Ecma-387 standard provides the possibility to combine more than one channel, which means that the data rate can be much higher than a single channel.

^{*}Project supported by the National High Technology Research and Development Program (No. 2011AA010202)

In this paper, the design of a reconfigurableGm-C low pass filter (LPF) for 60GHz wireless communication in a standard 65nm CMOS process is presented. The cutoff frequency is required to be tuned from 1GHz to 5GHz. The highest cutoff frequency (5GHz) means that we have combined 3 channels in that system. First, we give the topology of the filter and the method of reconfiguration. Second, we discuss the OTA design, which is really good for very high frequency filter design. Finally, the layout design and the post-simulation results of the filter are discussed.

2 Filter Topology Design and Reconfiguration Method

2.1 Filter Topology Design

Since ladder filters havegood sensitivity and dynamic range properties ^[2], the filter is usually derived from a passive LC ladder filter. In this paper, we give the normalized passive prototype filter in Fig.1. All the components are changeable so that the cutoff frequency of the filter can be tunable. It is a 3rd order Chebyshev filter, providing a good adjacent channel rejection and low power consumption.

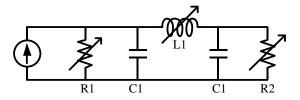


Fig. 1 Passive prototype filter

The active implementation is shown in Fig.2. The filter is designed with identical unit OTAs in different sizes. All the OTAs have different function. The g_{mC} module is a conversion of voltage to current. The g_{mR} module is an active resistor. The g_{mL} module and C_L forms an active inductor.

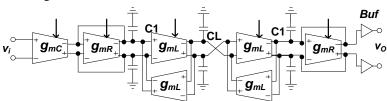


Fig. 2 Active implementation of LPF

There are several types of OTAs can form the filter as we mentioned. In this work, as the required highest cutoff frequency is 5GHz, we choose Nauta'sOTA^[3], as shown in Fig.3.

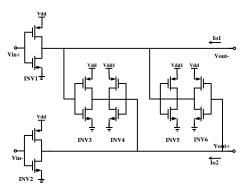


Fig. 3 Nauta's OTA

Nauta's OTA consists of 6 inverters. This circuit has advantages for high frequency design. There are no internal nodes to give rise to parasitic poles, the relatively high output conductance can be compensated by choosing transistor sizes appropriately, and large input and output voltage swings are possible for a given supply voltage.

2.2 Reconfiguration Method

As we have shown in Fig.1, through changing the value of resistor and inductor, the cutoff frequency can be tunable. We don't choose changing the capacitor, because in the circuit design of the LPF, the parasitic capacitor has a great impact on the cutoff frequency, especially in 5GHz.

In Nauta's OTA, we can calculate that the transconductance of it depended on the supply voltage $V_{\rm dd}$ (we will mention it later). The changeable transconductance means the changeable active resistor and the active inductor, which provides a means of reconfiguration.

To achieve a high cutoff frequency, the filter operates mainly on parasitic capacitances. Therefore, in the passive prototype filter, C_1 is determined by parasitic capacitances. In order to guarantee a good performance, the dc gain of all the OTAs need to be above 40dB and the cutoff frequency should be at least twice of the filter cutoff frequency.

In order to achieve anin-band gain higher than 0dB, the transconductance of

all the OTAs should meet the requirements as follows:

$$g_{mC} = 3g_{mR} g_{mL} = 2g_{mR}$$

3Nauta's OTA

3.1 V-I conversion

The transconductor is based on the well-known CMOS inverter, as shown in Fig.4. This CMOS inverter has no internal nodes and good linearity in *V-I* conversion if the β factors of the n-channel and p-channel transistors are perfectly matched^[3].

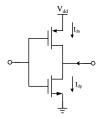


Fig. 4 A basic inverter

Assuming the p- and n-channel MOSFETS have ideal square law transfer functions in saturation, the transfer functions can be written as:

$$I_{dn} = \frac{\beta_n}{2} \left(V_{gsn} - V_{th} \right)^2, \quad \beta_n = \frac{\mu_n C_{ox} W_n}{L_n}$$
 (1)

$$I_{dp} = \frac{\beta_p}{2} \left(V_{gsp} - V_{th} \right)^2, \quad \beta_p = \frac{\mu_p C_{ox} W_p}{L_n}$$
 (2)

Then the output current of the single inverter can be written as:

$$I_{out} = I_{dn} - I_{dp} = \alpha (V_{in} - V_{tn})^2 + bV_{in} + c$$
 (3)

With

$$a = \frac{1}{2}(\beta_n - \beta_p)$$

$$b = \beta_p (V_{dd} - V_{tn} + V_{tp})$$

$$c = \frac{1}{2}\beta_p [V_{tn}^2 - (V_{dd} + V_{tp})^2]$$

When we have the differential inputs, assuming that

$$V_{in1} = V_c + \frac{1}{2}V_{id}V_{in2} = V_c - \frac{1}{2}V_{id}$$

then we can calculate the differential output current $I_{\rm od}$ ($V_{\rm c}$ is the common mode voltage).

$$I_{o1} = a(V_c - V_{tn} + \frac{1}{2}V_{id})^2 + b\left(V_c + \frac{1}{2}V_{id}\right) + c$$

$$I_{o2} = a(V_c - V_{tn} - \frac{1}{2}V_{id})^2 + b\left(V_c - \frac{1}{2}V_{id}\right) + c$$

$$I_{od} = I_{o1} - I_{o2} = V_{id}\left[\beta_p\left(V_{dd} - V_c + V_{tp}\right) + \beta_n\left(V_c - V_{tn}\right)\right] = V_{id}g_{md}$$

Then we can get the transconductance of the inverter:

$$g_{md} = \beta_p (V_{dd} - V_c + V_{tp}) + \beta_n (V_c - V_{tn})$$
(4)

Equation (4) is valid as long as the transistor operates in strong inversion and saturation. The differential transconductor is linear, even with nonlinear inverters. Also, the value of the transconductance can be changed with $V_{\rm dd}$.

3.2 Common mode control and DC-Gain Enhancement

The common-mode level of the output voltages V_{o1} and V_{o2} is controlled by the four inverters Inv3-Inv6 of Fig.1. In the nodes " V_{out+} " and " V_{out-} ", we can see the common resistor and differential resistor as shown in table 1.

 ${\bf Table~1}$ Common and Differential Resistance seen on nodes $V_{\rm out-}$ and $V_{\rm out+}$

Output Node	Common Resistance	Differential Resistance
$V_{ m out}$	$\frac{1}{g_{m5} + g_{m6}}$	$\frac{1}{g_{m5}-g_{m6}}$
$V_{ m out+}$	$\frac{1}{g_{m4} + g_{m3}}$	$\frac{1}{g_{\mathrm{m4}}-g_{\mathrm{m3}}}$

Therefore, if we choose g_{m3} equals to g_{m4} and g_{m5} equals to g_{m6} , the dc-gain will be infinite theoretically. But the maximal dc gain of an integrator will be degraded by mismatch. In fact, when g_{m3} closes to g_{m4} , the dc gain will be high enough for us to use.

In another side, the network of Inv3-Inv6 forms a low-ohmic load for

common mode signal. When we choose the proper size of each invertor, the common mode input voltage can be equal to the common mode output voltage. That is really benefit for the connection of the LPF system.

When the cutoff frequency of LPF is lower than 1GHz, we usually choose the value of g_{m3} equals to g_{m4} and equals to g_{m1} , thus guarantees the common mode stability and enough dc gain. However, as the cutoff frequency of the LPF is up to 5GHz now, we must minimize parasitic capacitance. Therefore, the four inverters, Inv3~Inv6, should have the minimum size of length. Also, CM stability requires the size of the inverters to meet the requirement as follows [4]:

$$g_{m3} + g_{m4} \ge 0.66 g_{m1}$$

4 Layout Design and Post-simulation Results

4.1 Layout design

The LPF layout is shown in Figure 5. To achieve a better performance, some critical parameters in layout should be accounted for: the interconnect resistance, the parasitic capacitance and the current density.

The interconnect resistance and parasitic capacitance will affect the performance the LPF, so we should minimize them. When the cutoff frequency is above 5GHz, the power consumption will be as large as 40mW, which means that the width of metal should be large enough. The total area of the layout is nearly 0.3mm^2 .

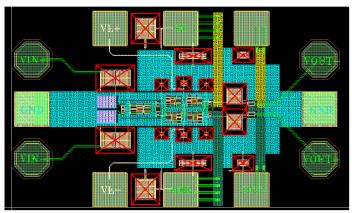


Fig. 5 Layout of LPF

4.2 Post-simulation results

This LPF is processed in 65nm CMOS technology with a 1.2V power supply.

At first, we give the post-simulation results of integrator, as shown in Fig. 6. The dc gain is 43dB and the unity-gain frequency is 15.5GHz, the phase margin is 66.6 degree. The transconductance of this integrator is given in Fig. 7. It is nearly 15.75mS and do not vary too much with frequency.

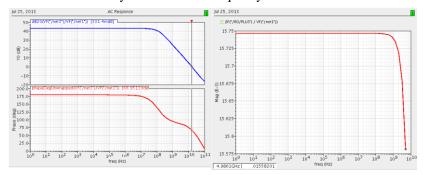


Fig. 6 AC response of Nauta's OTA

Fig. 7 Transconductor of Nauta's OTA

Then, we give the post-simulation results of LPF, as shown in Fig. 8. Fig. 8(a) shows that the cutoff frequency of LPF can be 631MHz. At that time, the in-band gain is nearly 2dB, the adjacent channel rejection is about 23.5dB, the ripple in band is about 1.1dB. The total current is about 2.1mA.Fig.8(b) shows that the cutoff frequency of LPF can be 5GHz. At that time, the pass-band gain is nearly 2dB, in-band ripple is about 1.1dB, theadjacent channel rejection is about 27dB. The total current is about 27mA. Table 2 shows the comparison of the target and the post-simulation results.

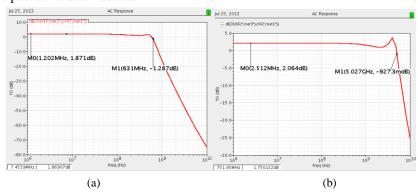


Fig. 8 AC response at 631MHz and 5GHz

 Table 2

 A comparison of the target and post-simulation results is given in table 2.

Parameters	Target	Post-simulation
Process	65nm CMOS	65nm CMOS
BW	1~5GHz	0.631~5.027GHz
Vdd	1.2V	1.2V
In-band gain	>0dB	2dB
In-band ripple	<1.5dB	1.1dB
Adjacent rejection	>20dB	26dB
T . 1.C	<30mA	27mA(@5GHz)
Total Current		2.3mA(@1GHz)

5 Conclusion

In this paper, we have presented a design of a 3rd order Chebyshev filter, based on Nauta's OTA. When the cutoff frequency is 5GHz, it means that 3 channels have been combined together and the data rate can reach the level of nearly 10Gbit/s. The post simulation results show that the LPF can meet all the requirements in the system.

References

- P. Wambacq, V. Giannini, K. Scheir et al, A Fifthorder 880MHz/1.76GHz Active Lowpass Filter for 60GHz Communications in 40nm Digital CMOS[J], Proc. ESSCIRC, pp. 350-353, September 2010.
- [2] Rolf Schaumann et al. Design of analog filters (second edition)[M]. Oxford University
- [3] B. Nauta, A CMOS Transconductance-C Filter Technique for Very High Frequencies, IEEE J. Solid-State Circuits, February 1992, vol. 27, no. 2, pp. 142-153
- [4] FawziHoufaf, Mathieu Egot1, Andreas Kaiseret al. A 65nm CMOS 1-to-10GHz Tunable Continuous Time Low-Pass Filter for High Data Rate Communication[C]. IEEE ISSCC February 22, 2012. pp. 362-364
- [5] S. D'Amico, M. Conta, and A. Baschirotto, A 4.1 mW 79 dB-DR 4th-order source-follower-based continuous-time filter for WLAN receivers[J], IEEE ISSCC Dig. Tech. Papers, Feb. 2006, pp. 1378–1387.