Design of a 24 GHz Programmable Frequency Divider in 65-nm CMOS Process[*]

Huagui Bao[1, 2], ZhiqunLi[1, 2, +], Qin Li[1], Zhigong Wang[1]
[1]Institute of RF- & OE-ICs, Southeast University, Nanjing, 210096;
[2]School of Integrated Circuits, Southeast University, Nanjing, 210096;
[+]Corresponding author: zhiqunli@seu.edu.cn

Abstract: A 24 GHz programmable frequency divider in 65-nm CMOS process is presented in this paper. The divide ratio can be varied from 208 to 270 in a step size of 2.The divider consists of a divide-by-2, an 8/9 dual-modulus prescaler, a programmable pulse-swallow counter and a buffer. The post simulation results demonstrate that the divider can operate with the input frequency ranging from 16 GHz to 32 GHz while it draws 7.3 mA from a 1.2 V power supply.
Key words: frequency divider; programmable frequency divider; divide-by-2, prescaler; pulse-swallow counter;

1. Introduction

Frequency dividers are widely used in many communication systems such as frequency synthesizer, time-recovery circuits and clock generation circuits. In a phase-locked loop (PLL), a frequency divider is to divide down the local oscillation frequency generated by the voltage-controlled oscillator (VCO) to make a comparison with the reference frequency. The programmability provided by the frequency divider leads to different locking frequencies of the PLL.

In this paper, a programmable divider for a 24 GHz PLL is presented. Fig. 1 shows the architecture of the PLL, and the proposed programmable divider is presented in the dashed box. As the input frequency of the proposed programmable divider is approximately 24~26 GHz, the proposed programmable divider is started by a divide-by-2 instead of traditionally a DMP to provide a large frequency division bandwidth and to reduce the burden of the DMP.

This paper is organized as follows. Section 2 discusses the circuit design of the proposed programmable divider. Layout design and post simulation results are presented in Section 3 and Section 4 comes to the conclusions.
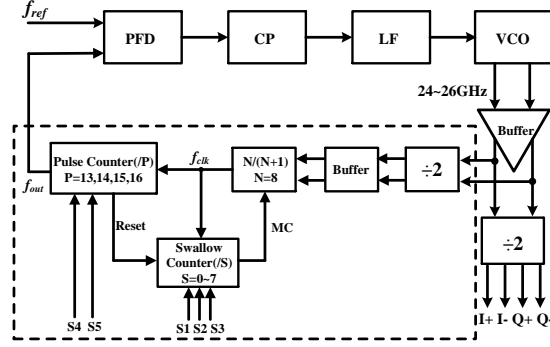

Fig. 1 Block diagram of the PLL and the proposed programmable divider

2. Circuit design

As shown in Fig. 1, for the 8/9 DMP, it divides by 8 when modulus controller (MC) is set to be '0' and 9 when MC is '1'. Then, the counter value of the pulse counter and swallow counter are set to be P and S, respectively. Before swallow counter counts to 0, MC is high so that the DMP divides by $(N+1)$ which is 9 in this paper. When swallow counter counts to 0, MC changes to be low so that the DMP begin to divide by N which is 8 in this paper. Hence, the modulus of the DMP and the pulse-swallow counter is

$$M^* = (N+1)S + N(P-S) = NP + S \tag{1}$$

As mentioned in Fig. 1, P is set from 13 to 16, S from 0 to 7 while N is set to be 8. Consequently, the modulus M^* can vary from 104 to 135 continuously. Taking the divide-by-2 into consideration, the overall divide ratio of the proposed programmable divider is

$$M = 2M^* \tag{2}$$

Which means the divide ratio of the proposed programmable divider varies from 208 to 270 in a step of 2.

2.1 Divide-by-2

Fig. 2 illustrates the structure of the proposed divide-by-2 frequency divider. The divider consists of two same latches in cascade, namely master latch and slave

latch. The output of the slave latch is inverted and fed back to the data input of the master latch as shown in Fig. 2 (a). This kind of feedback enables the divide-by-2 to oscillate at a certain frequency f_{osc} without any input signal. The self-oscillation frequency f_{osc} generally decides the operating frequency of a divider. The higher the self-oscillation frequency is, the higher the speed of operation will be. Also the input clock amplitude required in the vicinity of f_{osc} is very small, it is usually best to design $2f_{osc}$ to be slightly higher than the input frequency f_{in} of the divider to allow robust divider operation [1]. The latch uses a pseudo-differential structure which is different from the conventional frequency divider in which the tail current source is removed.
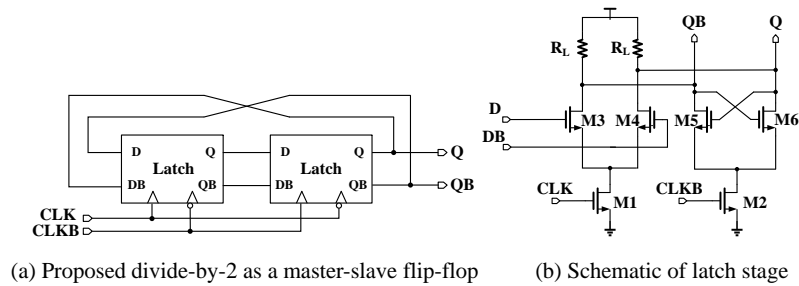

(a) Proposed divide-by-2 as a master-slave flip-flop   (b) Schematic of latch stage

Fig. 2 Structure of the divide-by-2

2.2 8/9 dual-modulus prescaler

Fig. 3 shows the block diagram of the proposed 8/9 DMP. It basically consists of a 4/5 synchronous dual-modulus circuit and a divide-by-2 asynchronous circuit. The 4/5 synchronous dual-modulus circuit consists of three differential D-flip-flops (DFF), as shown in Fig. 4 (a), and 2 NOR gates for modulus selection. The first two flip-flops form a divide-by-4 circuit while the third flip-flop adds an extra clock period delay for divide-by-5 [2], [3]. The propagation delay through these flip-flops and NOR gates decide the maximum operating frequency of the prescaler. So it is recommended to merge the flip-flops and the NOR gates together to reduce the delay [4]. Fig. 4 (b) shows the schematic of the D flip-flop with NOR. D_1 and D_2 are the input of the NOR logic while VB is a DC bias.

The divide-by-2 asynchronous divider adopts the topology of true single phase clock (TSPC). Fig. 5 shows the schematic of the proposed TSPC DFF. The reasons for using TSPC DFF instead of CML are that the input frequency of the divide-by-2 asynchronous divider is not that high. So it is suitable to use TSPC.

Compared with CML, TSPC has many advantages such as low power consumption, single-ended input and smaller chip area. When the negative output of the TSPC DFF feeds back to the input of the DFF, it works as a divide-by-2.
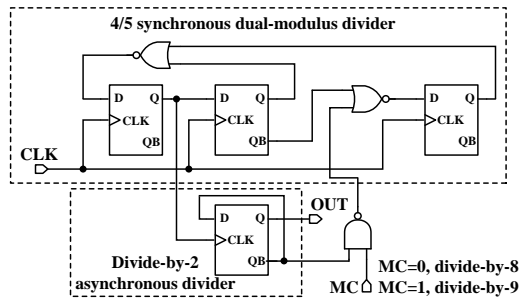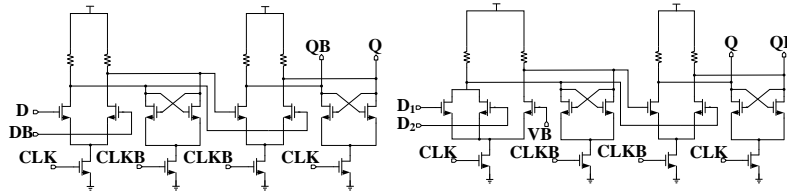
Fig. 3 Block diagram of 8/9 dual-modulus prescaler

(a) Schematic of D flip-flop without NOR (b) Schematic of D flip-flop with NOR

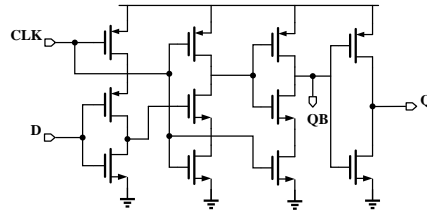**Fig. 4** Schematic of the DFFs used in 4/5 dual-modulus divider

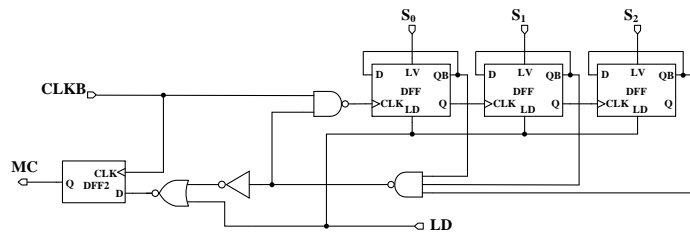**Fig. 5** Schematic of the proposed TSPC DFF

2.3 The pulse-swallow counter

The block diagram of the pulse counter and swallow counter are shown in Fig. 6. Both of the pulse counter and swallow counter consist of several DFFs and logic gates. In the pulse counter, $P_0 \sim P_3$ are the control bits of the counter, LD is a load signal or reset signal for both the pulse counter and the swallow counter. The LD signal enables the pulse counter and swallow counter to load the new counting

control bits which means the new counting value. The MC signal in the swallow counter is a modulus control signal for the 8/9 DMP.
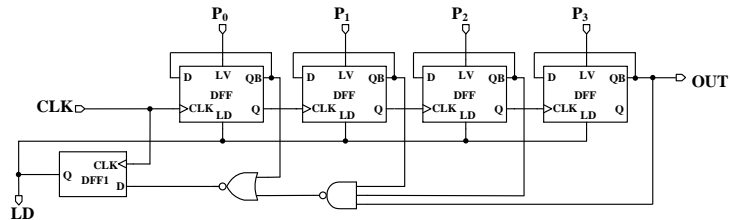
(a) Block diagram of the pulse counter

(b) Block diagram of the swallow counter

Fig. 6 Block diagram of the pulse counter and swallow counter

Fig. 7 illustrates the schematic of the TSPC DFF with reset signal and load-value signal in the pulse counter and swallow counter. LD is the input node of reset signal while LV is the input node of the load-value signal which is supposed to connect the control bits of the counter.
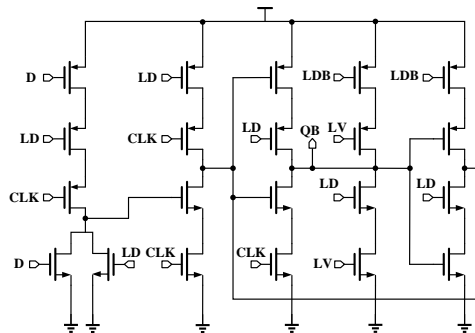

Fig. 7 Schematic of the TSPC DFF in pulse-swallow counter

3. Layout design and post simulation results

In this paper, the proposed programmable divider is fabricated in 65-nm CMOS

process. The layout of the proposed programmable divider is shown in Fig. 8. The area of the layout is $655\times650\mu m^2$. The inductors in the layout are adopted in the buffer which is to connect the divide-by-2 and the DMP. The buffer adopts a two stage CML differential amplifiers with resistive loads and inductive peaking for high-speed operation.
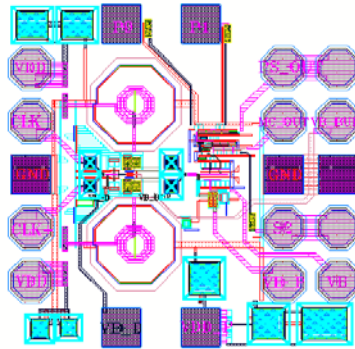

Fig. 8 Layout of the proposed programmable divider

The post simulation results show that the proposed programmable divider can operate properly with the input frequency ranging from 16 GHz to 32 GHz in normal condition. With the PVT variation, the divider can at least cover the frequency range from 20 GHz to 28 GHz which is large enough for the input frequency of 24~26 GHz for the application.

Fig. 9, Fig. 10 and Fig. 11 show the transient waves of the post simulation results of divide-by-2, 8/9 DMP and the pulse-swallow counter, respectively.

All the post simulation transient waves are simulated in the condition that the input frequency of the proposed divider is 32 GHz with the amplitude of 200 mV. The control bits are that $P_3P_2P_1P_0$=1100, $S_2S_1S_0$=100, which means the divide ratio $M=2M^*=2(NP+S)$ =216. And the load is 50 Ω. The current consumption is 7.3 mA from a 1.2 V power supply.

In Fig. 10, the transient waves are the input signal, output signal of the 8/9 DMP and the MC signal, respectively. When MC is high, the 8/9 DMP is in divide-by-9 mode while in divide-by-8 mode when MC is low. Four divide-by-9 periods can be counted in the output of the 8/9 DMP which corresponds to the control bits $S_2S_1S_0$=100.

As shown in Fig. 11, with the total divide ratio of 216 and the input

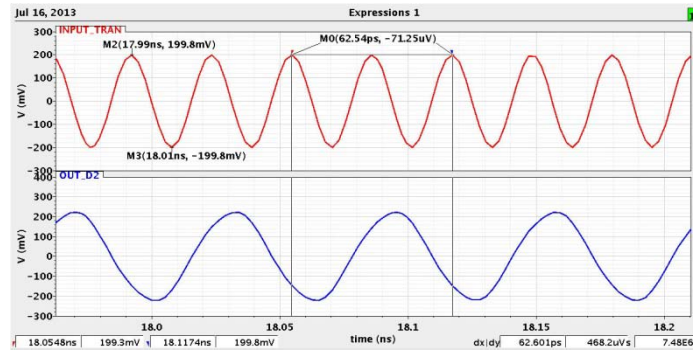frequency of 32 GHz, the output frequency is approximately 148.15 MHz.

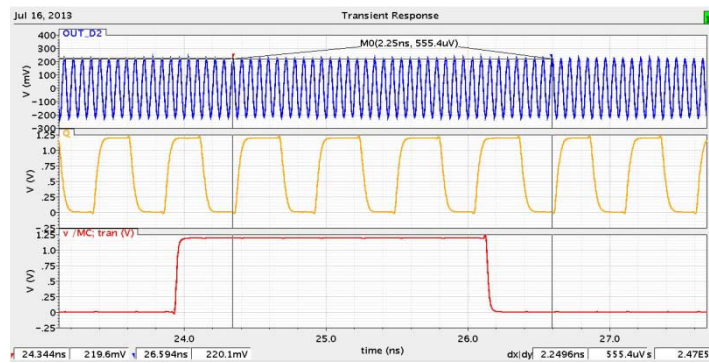**Fig. 9** Post simulation transient waves of the divide-by-2

Fig. 10 Post simulation transient waves of the 8/9 dual-modulus prescaler
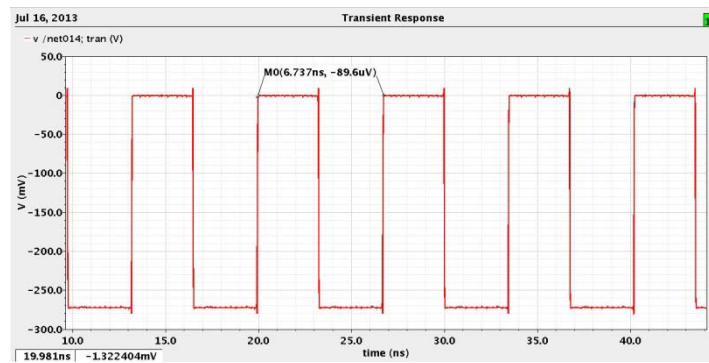

Fig. 11 Post simulation transient waves of the pulse-swallow counter

The performances of this work and some previously published programmable frequency divider are summarized in Table 1 for comparison.

Table 1 Performance comparison of high-speed CMOS programmable frequency divider

Ref.	Frequency range(GHz)	Divide ratio	Power(mW)	Process
[2]	6~21	256~263	9	0.13-μm CMOS
[5]	7~12	256~268 (step of 4)	19.95	0.18-μm CMOS
[6]	18.69~22.8	7/8	6.7	90-nm CMOS
This work	16~32	208~270 (step of 2)	8.76	65-nm CMOS

4. Conclusions

This paper presents a programmable divider designed in 65-nm CMOS process with divide ratio varied from 208 to 270 in a step of 2. The post simulation results show that the divider can work properly with the input frequency from 16 GHz to 32 GHz while the power consumption is 8.76 mW.

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