IV. THE RESULT OF OUR DESIGN

In our design, we use the CP2103 chip, the SPARTAN XC2S200 FPGA and other hard resource. The core of the softdog has been implemented using Veilog HDL. The Xilinx's ISE 9.2i tool for synthesis, place and route is used. The results after synthesis are shown in Table II

Our design for the data processing can be working at 255.875MHz. It supports a variety of baud rates.

V. CONCLUSION

In this work, we have presented a design of softdog based on FPGA. Our design uses the CP2103 which is a highly-integrated USB-to-UART Bridge Controller and the SPARTAN XC2S200 FPGA. The SPARTAN XC2S200 FPGA completes acquiring, processing and sending data. We take the AES as Encryption algorithm. Our design for the data processing can be working at 255.875MHz using 1520 slices. It supports a variety of baud rates.

Table 2. The Results after Synthesis

	Device Utilization Summary		
Logic Utilization	***Used***	***Available***	***Utilization***
Number of Slices	1520	1920	79%
Number of Slice Flip Flops	1048	3840	27%
Number of 4 input LUTs	2878	3840	74%
Number of bonded IOB	4	141	2%
Number of BRAMS	2	12	16%
Number of GCLKs	3	8	37%
Number of DCMs	1	4	25%

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