

# Integrated Switched Beamformer for 802.11ac Application

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**Abstract** - This paper present a fully integrated RF front-end beamformer for 802.11ac system. The principle of beam control is to use the array antenna arrangement circuit to control the phased array antenna; the antenna arrangement structure is to compensate for the distance difference caused by such a constructive interference or destructive wave interference. The circuit includes the low-noise amplifiers, passive phase shifters and high coupling transformer. The proposed study has eight different directions. The simulation result shows that the phased array can achieve a total gain of 17.65 dB and consumes 61.1mW under 0.9 voltage supply. Realized by the TSMC 1P6M 0.18um CMOS process, the area of the chip is 2.37mm\*1.84mm.

**Index Terms** - beamformer, LNA, phase shifter, 802.11ac

## 1. Introduction

With the rapid growth in communication system, Consumer electronics need to be compact, low cost and high efficiency, thus the passive element that cost large area is going to be integrated together. Several technique of integrated passive element such as Low-Temperature Co-fired Ceramics, System on Chip (SoC), System in Package (SiP) are now applied by industry. RFIC design is easy to implement by using SOC technique, it means that a chip contains a low noise amplifier, mixer, filter, power amplifier, voltage controlled oscillator and antenna, by doing so, this is more convenient for large-scaled production and cost savings, each part of the chip can reduce internal wiring, power consumption and parasitic.

The beamformer technique is a concerned issue in recent years. The beamformer system can improve the antenna gain and increase the quality of communications. Some researches implement the beamformer in the baseband with digital signal processing [1][2], it is must to meet some of the high speed Digital to Analog Converter (DAC), Analog-to-Digital Converter (ADC), digital signal processing (DSP) components and each signal path must maintain the same phase relationship. As the antenna number increase, the cost and the power consumption increase, the system becomes large and difficult to handle. It is practical to use direct RF front-end phase controlled array antenna for the application because it only needs to regulate the phase we need.

We proposed a switched beamformer in this study; it uses an array antenna circuit to regulate the phase we need and to make it in a particular direction to form constructive interference in space. The system can also improve the communication capacity suppress multipath fading caused by indoor mobile communications. Due to the base station working at different time, the main range is different such as during the day time, we can adjust the radio beam directions to science parks and other relatively crowded work area

however, after working hours, the base station's signal can be turned to a residential area in order to facilitate people to use. In addition, it also allow some of the base station to stop working, thus achieving carbon reduction and energy conservation.

## 2. Circuit Design

Fig. 1 shows the system architecture. Each building block are analyzed in the following section.

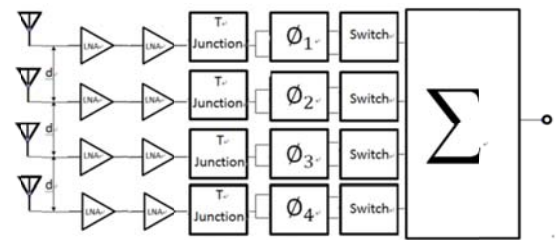


Fig.1 Beamformer Architecture

### A. Low-noise Amplifier

The proposed LNA is shown in Fig. 2; the input impedance can be expressed as below [3]

$$Z_{in} = \frac{sL_1}{1 + (gm_1 + C_{gs1})sL_1} \quad (1)$$

$gm_1, C_{gs1}$  represent the transconductance and gate to source capacitance of M1,  $L_1$  provides small impedance to ground and determined the input impedance. In the low frequency, the input impedance is close to zero, as the frequency increase and  $gm_1 \gg C_{gs1}$ , the impedance is approximately to  $\frac{1}{gm_1}$ .

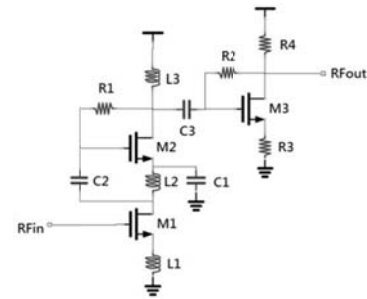


Fig. 2 802.11ac low noise amplifier

To achieve reasonable conversion gain and power consumption, the current reused technique is utilized. Fig. 3 shows the operating mechanism. The first stage is cascode architecture, as  $L_2$  and  $C_2$  separate M1 and M2, two common source amplifiers are formed, and the signal can be amplified

twice by using the same current. The output matching network are M3 with a resistive feedback resistor R2, the parasitic capacitances of M3 are also a part of the network. We can do the output matching by adjust the size of M3 appropriately. Although the resistive feedback decreases the overall gain and increase the noise figure, it is a practical method to broaden the bandwidth and save the chip area.

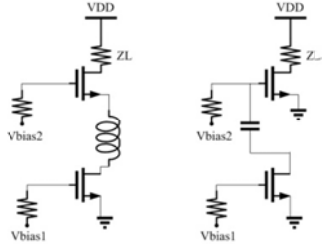


Fig. 3 Current reuse mechanism

Fig. 4 and Fig. 5 presents the simulation result of S-parameter of proposed LNA, the parameters are below -10 dB and cover the whole band. Fig. 6 shows the noise figure of the LNA.

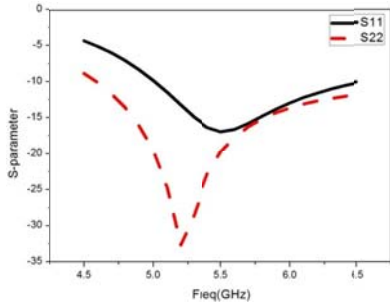


Fig. 4 S11 and S22

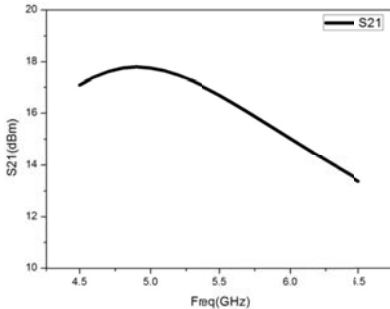


Fig. 5 S21

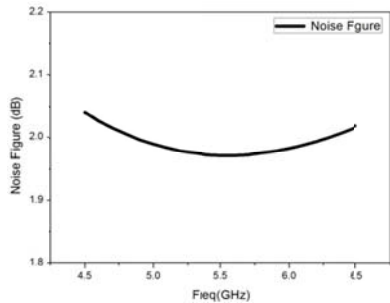


Fig. 6 noise figure

### B. Passive Phase shifter

One of the key elements of proposed study is the ninety degrees phase shifter. By controlling the phase shift of four antennas, a constructive interference or destructive wave interference can be achieved. The R1 and C1 makes a positive forty five degrees phase shift, and R2 and C2 makes a negative forty five degrees phase shift. Thus, we can have a ninety degrees difference output signal relative to the input one. Fig. 8 shows the phase simulation result of the proposed study. The angle deviation is about  $\pm 2$  degrees. The simulation result indicates a -8dB loss which is shown in Fig. 9.

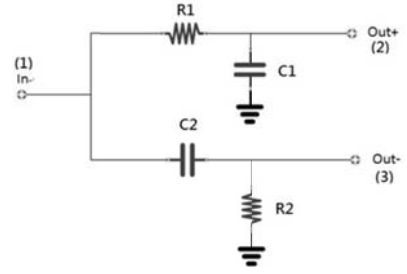


Fig. 7 Passive phase shift

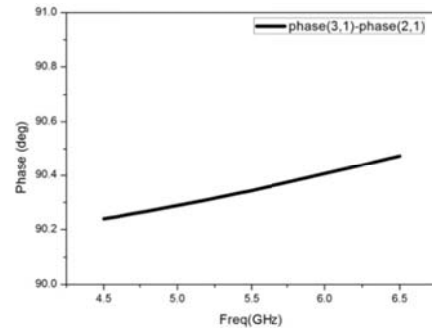


Fig. 8 Passive phase shift

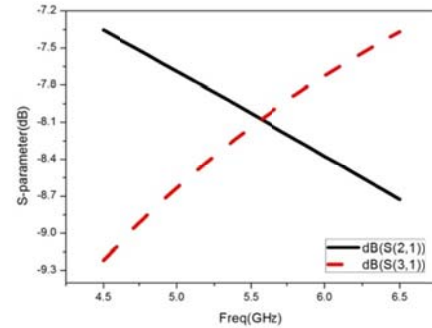


Fig. 9 Passive phase shift

### C. Switch

The Switch schematic is shown in Fig. 10. The output can be switched between ON / OFF mode by controlling the voltage of V and  $\bar{V}$ . The switch provides wide bandwidth without high insertion loss. R1 and R2 acts like RF chokes which can avoid the noise interference from DC supply. Table1 shows the truth table of the switch.

TABLE I Switch truth table

V	$\bar{V}$	Channel 1	Channel 2
5V	0V	ON	OFF
0V	5V	OFF	ON

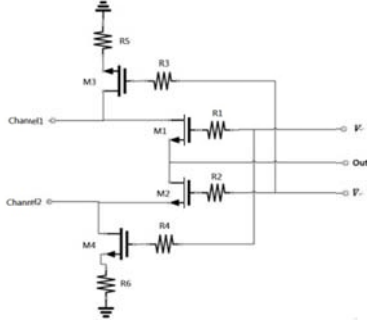


Fig. 10 Switch

#### D. Transformer

The last stage is the transformer that can combine the power from the former LNAs. The power combine method can be divided into two types: series combining transformer (SCT) and parallel combining transformer (PCT) [4]. The PCT method is more efficient and can save area compared to the SCT method, thus the proposed study adopts the PCT [5].

The desired inductance  $L_p$  can be calculate by (2)

$$f = \frac{R}{2\pi * L_p * \sqrt{1-K^2}} \quad (2)$$

R represents the former stage impedance, f is the frequency and K is the coupling coefficient. Fig. 11 shows the proposed transformer. We have already reported the transformer in [5]

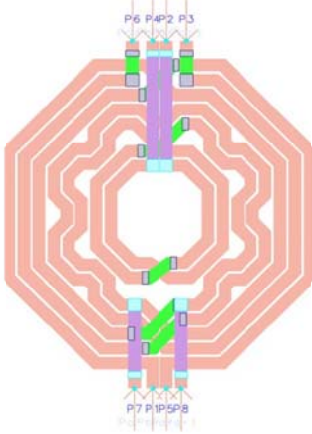


Fig. 11 transformer

### 3. Simulation Result of the System

The circuit design proposed in this study was developed using the TSMC 0.18  $\mu\text{m}$  1P6M CMOS technology process, and was simulated using Advanced Design System (ADS) software with Cadence employed for the layout. The simulation and layout included the parasitic effects of the

circuit, and electromagnetic (EM) simulation was also conducted. Fig. 12 shows that the four antennas are arranged in a square-type. The relationship can be obtained by calculating the trigonometric functions. Fig. 12 shows the simulated pattern in different case of phase shift. Fig. 13 shows the simulated pattern in different combinations of phase shift.

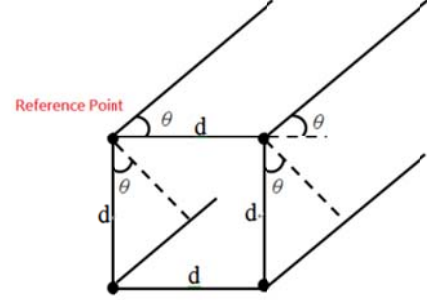


Fig. 12 Antenna positions

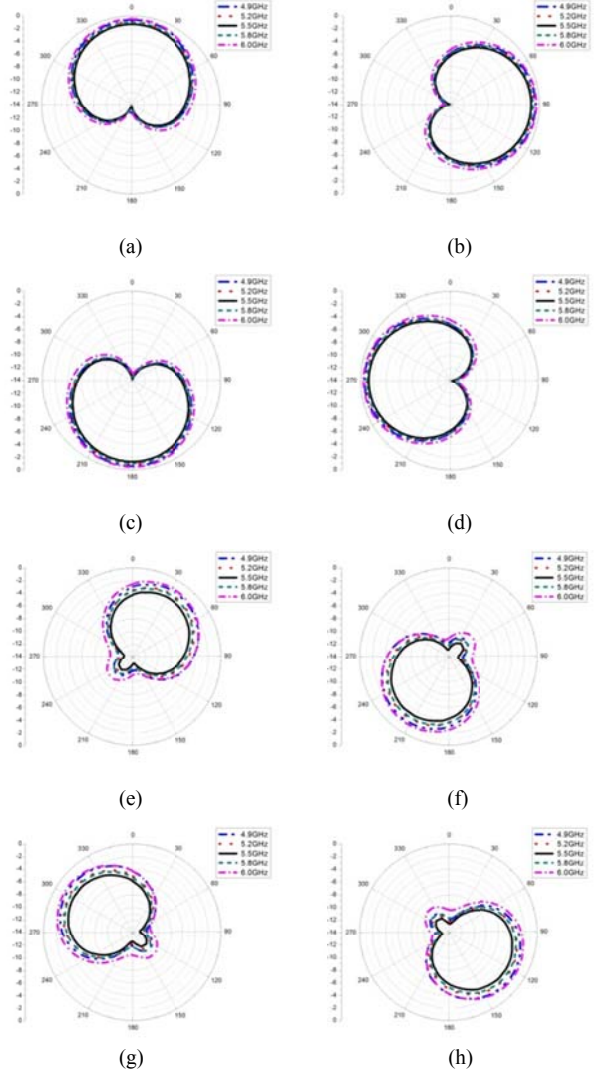


Fig. 13 pattern

- (a)  $\phi_1 = 90, \phi_2 = 0, \phi_3 = 0, \phi_4 = 90$
- (b)  $\phi_1 = 0, \phi_2 = 0, \phi_3 = 90, \phi_4 = 90$
- (c)  $\phi_1 = 0, \phi_2 = 90, \phi_3 = 90, \phi_4 = 0$
- (d)  $\phi_1 = 90, \phi_2 = 90, \phi_3 = 0, \phi_4 = 90$
- (e)  $\phi_1 = 90, \phi_2 = 0, \phi_3 = 90, \phi_4 = 90$
- (f)  $\phi_1 = 90, \phi_2 = 90, \phi_3 = 90, \phi_4 = 90$
- (g)  $\phi_1 = 90, \phi_2 = 90, \phi_3 = 0, \phi_4 = 90$
- (h)  $\phi_1 = 0, \phi_2 = 90, \phi_3 = 90, \phi_4 = 90$

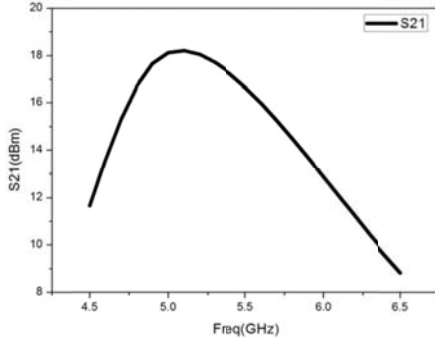


Fig. 14 S21

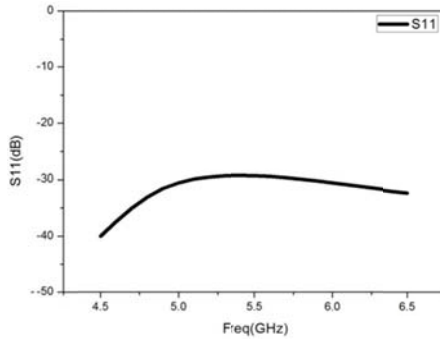


Fig. 15 S11

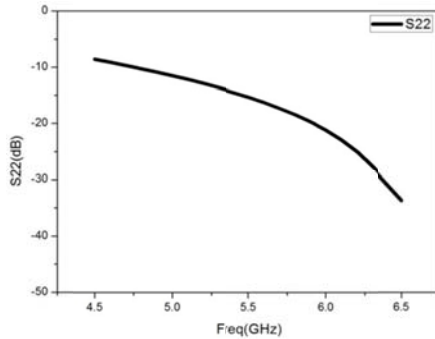


Fig. 16 S22

Fig. 14 shows the S21 of the beamformer system, the gain is above 14 dB in the 802.11ac band. Fig. 15 and Fig. 16 present the s11 and s22 are below -10 dB. Fig. 17 is the layout of the study; the die area is 2.37mm\*1.84mm.

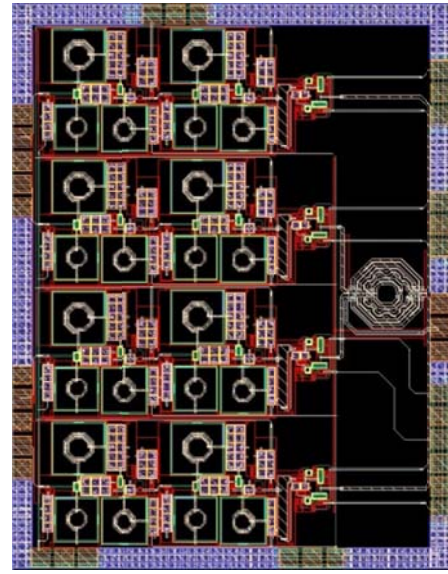


Fig. 17 Layout of proposed study

#### 4. Conclusions

A fully integrated 0.18  $\mu\text{m}$  CMOS beamformer system for 802.11 ac application was demonstrated. Low noise amplifiers, phase shifters, switches and transformer are integrated on chip. The proposed LNA adopts the current reuse topology makes the system low power consumption. Switch and phase shifter are adjusted appropriately in order to attain good performance. The simulation result shows that the system can achieve a total gain of 17.65 dB and consumes 61.1mW under 0.9 voltage supply. The area of the chip is 2.37mm\*1.84mm.

#### Acknowledgment

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#### References

- [1] Gierenz, V.S, Schwann, R. Noll, T.G "A low power digital beamformer for handset ultrasound systems," Solid-State Circuits Conference, 2001. ESSCIRC 2001. Proceedings of the 27th European, 2001, pp261-264
- [2] Dudas.L, Kovacs. P, Seller.R, "Digital Beamformer Antenna System," Radioelektronika, 2007. 17th International Conference, April 2007, pp1-5
- [3] Ke-Hou Chen; Jian-Hao Lu; Bo-Jiun Chen; Shen-Iuan Liu, "An Ultra-Wide-Band 0.4–10-GHz LNA in 0.18- $\mu\text{m}$  CMOS," Circuits and Systems II: Express Briefs, IEEE Transactions on , vol.54, no.3, pp.217,221, March 2007
- [4] Kyu Hwan An; Ockgoo Lee; Hyungwook Kim; Dong Ho Lee; Jeonghu Han; Ki Seok Yang; Younsuk Kim; Jae Joon Chang; Wangmyong Woo; Chang-Ho Lee; Haksun Kim; Laskar, J., "Power-Combining Transformer Techniques for Fully-Integrated CMOS Power Amplifiers," *Solid-State Circuits, IEEE Journal of*, vol.43, no.5, pp.1064,1075, May 2008
- [5] Jhu-Jyun Jhang, Yang Jeng-Rern "A high coupling factor transformer at 2.4 GHz in 0.18  $\mu\text{m}$  CMOS," IEEE Signal Processing, Communication and Computing (ICSPCC), 2013, pp1-4