Multi-DSP and FPGA-based Image Acquisition and Processing Platform

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Abstract - To meet the complexity of digital image processing algorithms and the development trend of the modular process, proposed multi-DSP and FPGA based digital image processing platform. Four TI's DSP of C6455 family as platform cores, and FPGA of Virtex-4 family as a system coordinated controller, achieve the four DSP interconnect, complete real-time, high-speed, parallel digital image processing system. Four DSP and FPGA connected to the EMIF interface, through which switch and transfer the data flow and the instruction stream, each costing DSP is equipped with DDR Ⅱ memory, to help DSP to complete the transfer of data and instruction memory, and out through one of the PCI expansion interface and Ethernet port. The image acquisition is controlled by the FPGA, and achieved by the ADC chip, which is the ADS5270 with four 8-channel, 12-bit precision, 40MSPS sampling rate, together constitute the analogue signal of 32-channel acquisition module. Ultimately complete image acquisition and signal processing platform.

Index Terms - EMIF, Parallel processing, A/D acquisition, Digital image processing.

1. Introduction

In people's lives and production process, the image is an effective way to obtain and exchange information, so the image signal acquisition and processing is necessary. With the image processing technology continues to evolve, the A / D acquisition made increasing demands, not only in the acquisition rate in the signal processing to be able to meet the requirements, but also in multi-channel acquisition should be increased. Due to the A/D chip level of development constraints, a single A/D acquisition chip can't meet the needs of high-speed and high accuracy, so use relatively low-speed multi-chip A/D chip sampling is to improve the system sampling rate is an effective way [1].

High sampling rates and complex requirements of digital image processing algorithms require signal processing platform to show more robust performance in hardware, not only the capacity to meet certain requirements, and processing platform architecture also can promote the parallel processing algorithm. The Harvard architecture DSP microprocessor compared with normal Von-Neumann architecture in this area has a great advantage, it is processing capability, rich peripheral interfaces, when a single processing core can't meet the processing requirements and architecture, DSP peripheral interface for interconnection and parallel multi-core processing provides strong support.

DSP provides the Rapid I/O, EMIF, PCI, HPI and other interfaces can achieve multi-DSP interconnect, but they also exist the relatively large differences, because different interfaces Flynn corresponding to different structures and different the Flynn structure corresponding to the different processing algorithms. For example: Rapid I/O and the EMIF is generally used to interconnect data exchange, the corresponding structure is generally Flynn multiple instruction multiple data stream (MIMD); PCI bus is generally used to interconnect, the corresponding structure is generally Flynn multiple instruction single data stream (MISD).

Applications under the platform and the execution of the code structure, MIMD architecture more obvious advantages, the Rapid I/O and the EMIF interface as the first choice. Rapid I/O interface structure is more complex, it's based on the general need to use a dedicated chip interconnect as the interface switch, while the EMIF interface simple, FPGA interconnect switching can be realized, so the platform built by the FPGA to control DSP EMIF interface to achieve a multi-DSP parallel signal processing.

2. The Structure of the Hardware Platform

Hardware platform architecture is shown in Figure 1, FPGA logic control 4 ADC chip, and sampling the data passing through the EMIF interface of DSP. FPGA complete the data distribution, according to each specific algorithm of software in the DSP, transfer incoming data according to certain rules of each DSP, achieved the optimal allocation of data. The EMIF interface Built-in DSP and FPGA seamlessly through simple logic within the FPGA configuration to complete high-speed data transmission. And, TMS320C6455

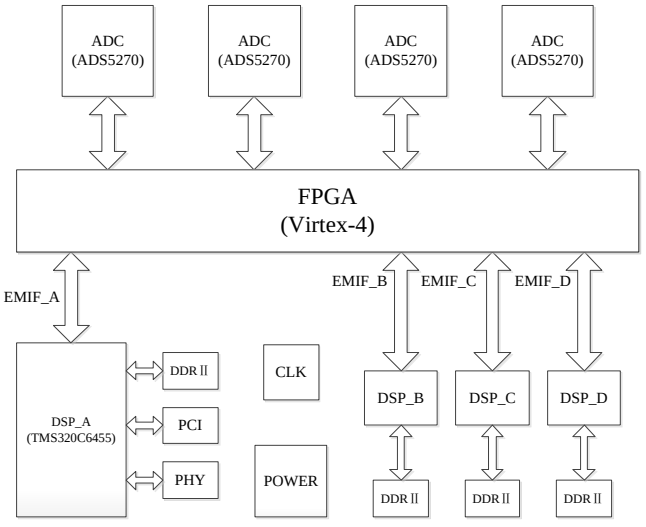

Figure 1: The structure of the hardware platform

series DSP built-in interface is very rich, the platform according to own needs and scale-out Ethernet interface PCI. All are equipped with dedicated DSP DDR Ⅱ memory, to be responsible for processing data and temporary storage of data has been processed for real-time, high-speed, parallel digital signal processing provides a strong support.

Platform built-in power supply module, the input voltage of +5 V and ± 12V, the voltage through the power conversion chip, to be +3.3 V, +2.5 V, +1.8 V, +1.2 V and other voltage. Each chip has a strict system power-on sequence, controlled by the TPS3808G01 chip, the order is: FPGA core, FPGA's I / O interfaces, DSP cores, ADS5270, other.

Unified management system clock, including the following sections:

1, ADS5270 part of the clock, including ADCLK and SCLK, ADCLK provide for the 40MHz crystal oscillator, SCLK up to 20MHz provided by the FPGA clock.

2, Part of the DSP clock, including 50MHz and 25MHz, provided by the crystal. After a clock buffer, while four DSP provides the clock signal.

3, EMIF interface and FPGA portion of its clock are 100MHz, provided by the crystal.

3. ADC control

ADS5270 is TI's ADC of 8 channel 12-bit precision, 40MSPS sampling rate, it has low power consumption and high integration features, the output interface uses a serial LVDS, reducing the number of interfaces and interface connection packet the size of the. ADS5270 all channels are controlled under the same clock signal ADCLK, the output format is LVDS with the signal 6 octave and 1 octave of the clock signal.

3.1 Initialization

The initial configuration of the ADS5270 is the SCLK and SDATA via the serial interface implementation, shown in Figure 2. SCLK is the serial input provided by the FPGA clock, chip select signal with the case, in eight clock cycles, in order to write the serial data signal 8-bit. The first one is the highest position, the top four for the register address, the last four for the data to be written. For example: When the 8-bit serial data is "00000011", said register address as "0000" that LVDS settings, and the write data is "0011" that the normal output of the ADC, the output circuit is 6.0mA.

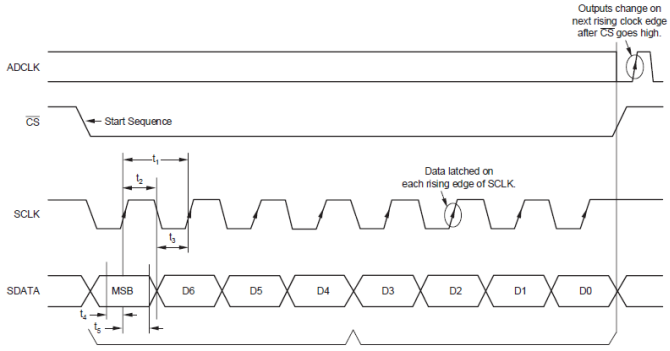

Figure 2: Serial interface timing

3.2 LVDS timing

ADS5270 can be configured for internal reference mode, in the internal reference mode, ADC can achieve a higher sampling accuracy. REFT as the reference voltage 1.95V, REFB to 0.95V, so the differential amplitude of the lowest is -1V, the output conversion results corresponding to 0LSB; differential amplitude of up to +1 V, the corresponding output conversion results 4095LSB (Full scale).

Specific timing of the LVDS output shown in Figure 3. Since the output data of each channel go through parallel-serial conversion and output by pipeline structure, thus resulting in delay of 6.5 clock cycles. The output is the LVDS serial data format, and clock output with 6-fold ADCLK.

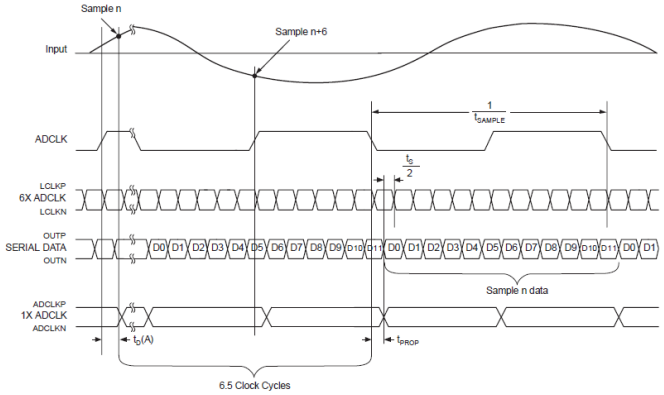

Figure 3: LVDS timing diagram

3.3 Power-up and reset

ADS5270 power-up and reset are achieved respectively through the signal of PD and #RESET. When the PD signal goes low last 1us, chip all the power-down, and stop working; when the PD signal up last 10us, all on-chip power, and start working. On-chip power continued to 10ms, if the #RESET continued low 100ns, the ADS5270 to restart, to be re-configured.

4. Debugging Interface

Mainly in signal processing platform using EMIF, PCI and Ethernet interfaces, these interfaces have been built in the TMS320C6455 series DSP chip.

4.1 PCI and Ethernet interfaces

PCI interface supports four types of PCI data exchange, namely: slave model to write, slave model to read, master mode to write and master mode to read. PCI interface includes three types of registers, namely: PCI configuration registers, PCI I/O registers and the PCI registers of mapped in the DSP memory space [2-4]. In this platform, PCI interface is responsible for the data transmission between the inside and external, data can be passed by the PCI interface platform can also be transmitted by the processing platform.

C6455 on-chip Ethernet MAC supports four Gigabit Ethernet media interfaces, respectively, MII, RMII, GMII, and RGMII. One MII and RMII support 10M and 100M operation,

RMII is to simplify the MII interface. The GMII and RGMII Gigabit Ethernet MII interface, RGMII that simplifies the GMII interface. As long as EMAC PHY chip is connected by the MDIO module is responsible for management, including PHY chip device status monitoring, configuration, and enumerations.

By configuring the internal registers can be completed EMAC/MDIO module, configuration, and many other operations. In addition, EMAC module has two internal buffers, were used to store or to receive Ethernet packets to be sent a description of information, such as the storage location or data packet length. Through on-chip peripheral bus, and register these buffer memory mapped to the DSP system, a fixed address space [5-6]. Therefore, by means of on-chip direct memory access DMA controller and the data packet description, EMAC/MDIO interrupt the CPU can work independently of work and then directly access the data storage area.

4.2 EMIF

The signal lines of EMIF interface shown in Figure 4, C6455 has a 64-bit wide external memory interface, EMIFA, addressable space of 4GB, with almost all types of memory, and interfaces directly to the FPGA, the data throughput of up to 4800Mbyte/s. DSP exchange the data between each internal module and external memory, must be controlled by the EMIF. EMIF input clock can either be generated internally, but also by external input [7-8]. External clock input pin through ECLKIN, register the software by setting the PLL frequency factor for frequency. EMIF can be reset by hardware reset or software reset the form, the hardware state machine is reset, FIFO and reset the internal registers; software reset only resets the internal state machine and FIFO and interrupt registers, and other internal registers cannot be reset.

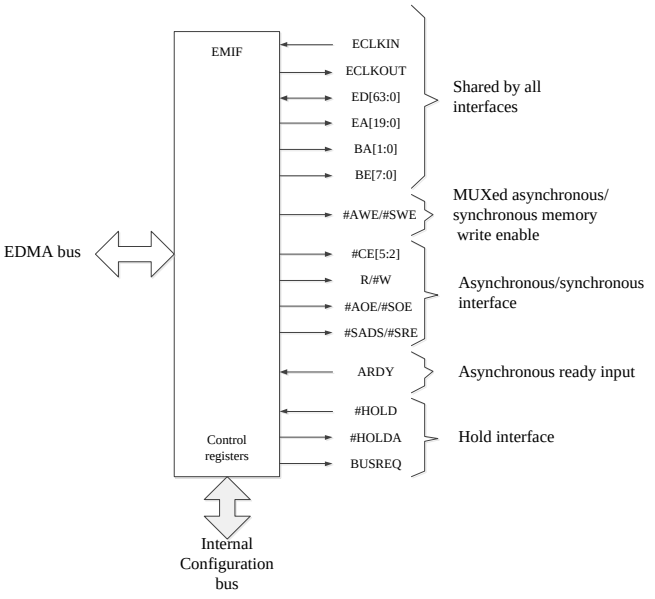

Figure 4: EMIF interface

4.3 Interconnection based on the EMIF interface

Multi-DSP-based data exchange must rely on interconnect chip interconnect to achieve, as long as all the DSP through its own interface directly connected with the interconnect chip can be achieved. Interconnection of systems in this way there is no mutual coupling, and the scale of the system is not completely limit the number of DSP chip interface can be extended infinitely. In this way the transmission efficiency, good controllability, large scale, is now the most widely used DSP interconnect technologies.

The design of the interconnection and routing module with the FPGA's internal logic implementation, with all EMIF interface, set within the FPGA FIFO for temporary data storage. By using sample lookup table design, according to each DSP within the FPGA mapped address, data of the move. Compared with using a dedicated interconnect chips, FPGA has more flexibility, according to the different needs of its internal logic and make the appropriate changes to meet the needs of different use.

5. Conclusions

The project designed a multi-DSP and FPGA-based digital image processing platform. 32-channel analogue input signal acquisition module, single channel to achieve 40MSPS sampling rate. In-depth study of DSP technology theory and multi-DSP interconnect technology, taking into account the signal processing system scalability and versatility, to determine to use four TMS320C6455 series DSP common high-speed parallel signal processing, the via data exchange by DSP EMIF interface, FPGA as an interconnection and control chip, to achieve without the aid of any computer system in case of complete digital image processing, storage and transmission and other related work. Processing speed, up to the 34400MIPS; signal parallel processing can be divided into a few pieces of data to be processed; rich interface to adapt to a variety of conditions and applications, digital image processing hardware platform design, production and commissioning has been completed.

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