# Novel BCD Circuits Design Using And-Or-Inverter Gate and Its Quantum-Dot Cellular Automata Implementation

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## Abstract

Quantum-dot cellular automata (QCA) provide a novel electronics paradigm for information processing and communication. A basic quantum-dot cell consists of several quantum dots with two excess electrons. A binary coded decimal (BCD) and a decimal coded binary (DCB) circuit based on QCA logic gates: the and-or-inverter (AOI) gates are proposed in the study. In addition, the circuits designed by traditional CMOS technology are also implemented for comparison. Compare with the traditional CMOS BCD device, QCA circuit is a low power and area-efficient architecture.

**Keywords**: Quantum-dot cellular automata (QCA), binary coded decimal (BCD), decimal coded binary (DCB), and-or-inverter (AOI) gates

## 1. Introduction

Quantum-dot cellular automata (QCA) have been recognized as one of the revolutionary to nano-scale computing devices [1]. The basic quantum-dot cell is charged with two excess electrons and performs computation on Coulomb interactions of electrons [2]-[5]. In this paper, we propose the design of a novel QCA logic gate: the and-or-inverter (AOI) gate [6]. The design of AOI gates is shown in Fig 1.

Utilizing the property of Majority Voter (MV) that with three inputs, we have Y=F=AB + BC + AC. Assume the output of MV1 is F1, and the output of MV2 is F. Then we get F1 =A’B+ BC’ + A’C. With the same reason, we can get F= (A’B+BC’+A’C’) D+ (A’B+BC’+A’C’) E+DE= DE+ (D+E) (A’B+ BC’+ A’C)

In the traditional computing science, there are only logic 0 and logic 1. High voltage is defined as logic 1 and low voltage is defined as logic 0. CMOS technology utilizes current to drive the device, while QCA is based on the encoding of binary information in the charge configuration within quantum dot cells. It can change its phase by the Columbic interaction between QCA cells [7].

In digital systems, the translating circuit of decimal numbers by encoding each digit in binary form is very important. In our study, a binary coded decimal (BCD) and decimal coded binary (DCB) circuit based on AOI gates are proposed for the first time.

## 2. BCD circuit design based on AOI gates

In this study, we present a novel and complex QCA gate: the AOI gate, which is a five-input gate consisting of seven cells. QCA-based binary coded decimal circuit decodes each binary pattern (0 and 1) to the decimal digit (0~9). The QCA-based binary coded decimal circuit based on AOI gates (AOI-BCD) is shown in Fig. 2(a). When the binary signals (0 and 1) are inputted into the AOI-BCD circuit, the input digits ($W_3$, $W_2$, $W_1$, $W_0$) are decoded to the decimal digits ($Y_9$, $Y_8$, $Y_7$, $Y_6$, $Y_5$, $Y_4$, $Y_3$, $Y_2$, $Y_1$, $Y_0$). The logic expressions for $Y_9, Y_8, Y_7, Y_6, Y_5, Y_4, Y_3, Y_2, Y_1, Y_0$ are

$$Y_9 = W_3\overline{W_2}\,\overline{W_1}W_0, \quad Y_8 = W_3\overline{W_2}\,\overline{W_1}\,\overline{W_0},$$

$$Y_7 = \overline{W_3}W_2W_1W_0, \quad Y_6 = \overline{W_3}W_2W_1\overline{W_0},$$

$$Y_5 = \overline{W_3}W_2\overline{W_1}W_0, \quad Y_4 = \overline{W_3}W_2\overline{W_1}\,\overline{W_0},$$

$$Y_3 = \overline{W_3}\,\overline{W_2}W_1W_0, \quad Y_2 = \overline{W_3}\,\overline{W_2}W_1\overline{W_0},$$

$$Y_1 = \overline{W_3}\,\overline{W_2}\,\overline{W_1}W_0, \quad Y_0 = \overline{W_3}\,\overline{W_2}\,\overline{W_1}\,\overline{W_0}$$

Following the above expression, the design flow chart for AOI-BCD is demonstrated in Fig. 3.

In the similar way, AOI-DCB circuit transforming each decimal digit to the binary pattern is implemented and simplified that is shown in Fig. 2(b). $W_3, W_2, W_1, W_0$ are expressed as

$$W_3 = Y_9 + Y_8$$
$$W_2 = Y_7 + Y_6 + Y_5 + Y_4$$
$$W_1 = Y_7 + Y_6 + Y_3 + Y_2$$
$$W_0 = Y_9 + Y_7 + Y_5 + Y_3 + Y_1$$

# 3. BCD circuit design based on CMOS technology

In addition, a BCD circuit designed by traditional CMOS technology (shown in Fig. 4) is implemented for comparison. Compares with traditional CMOS devices which need 19(Length) ×12(Width) ×12(Height)mm to implement BCD circuit. The AOI-BCD circuit needs simply areas of 355nm×1425 nm. .Lent C.S presents the power dissipation of QCA is roughly $10^{-10}$ Watts per input bit, that is much less than the conventional devices [1]. So we demonstrate that the AOI-BCD circuit is actually area-efficient and less power dissipation architecture.

# 4. Conclusion

In summary, an AOI-BCD and an AOI-DCB circuit are proposed. This QCA circuit design provides a new functional paradigm for information encoding and decoding. Compare with the traditional CMOS BCD device, AOI-gates circuit is a low power and area-efficient architecture. In addition, the QCA binary logic functions and the related new digital computational nanotechnology will provide high speed, and high density applications. It is believed that QCA will become a much more practical approach to create a faster and denser circuit.

# 5. References


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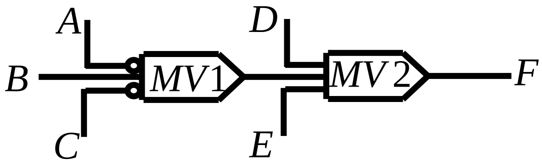


**Fig. 1.** The basic AOI gate. The logic function of the AOI gate is $F = DE + (D+E)(\overline{A}\,\overline{C} + \overline{A}B + B\overline{C})$

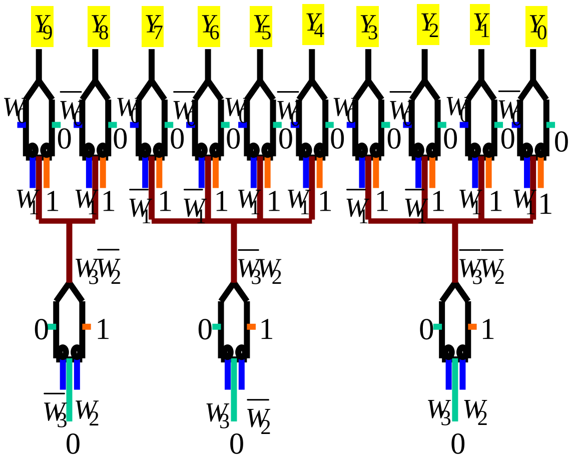

**Fig. 2(a).** The Q-BCD circuit designed using AOI gates.

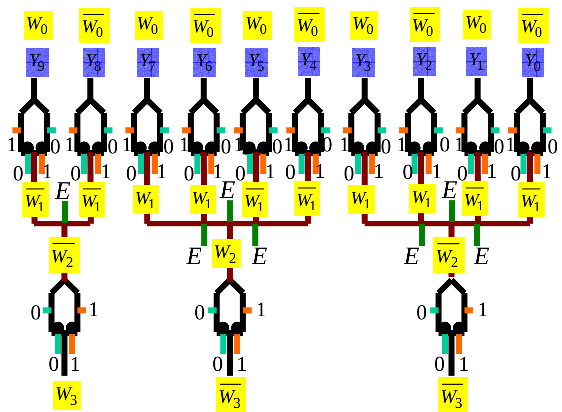

**Fig. 2(b).** The Q-DCB circuit designed using AOI gates.

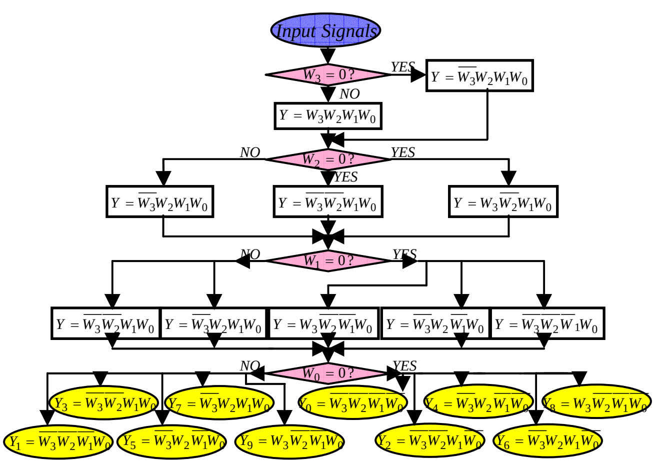


**Fig. 3.** The flow chart of AOI-BCD circuit design.

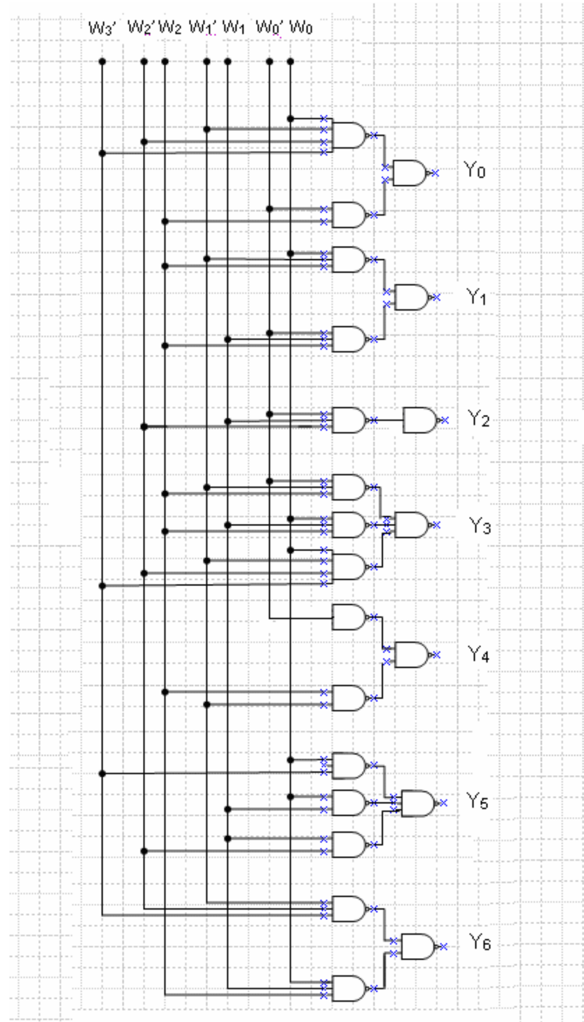


**Fig. 4.** The BCD circuit designed by traditional CMOS technology.