Numerical study for enhancement-mode AlN/GaN/AlN N-polar MISFET with self-aligned source/drain regions

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Abstract—In this work, for the first time, the electrical characteristic of the enhancement-mode (E-mode) N-polar GaN metal-insulator-semiconductor field effect transistor with self-aligned source/drain regions is investigated by SILVACO TCAD software. Macroscopic polarization effect of III-V nitrides are included and are used to realize the E-mode operation. Numerical study results show that E-mode N-polar GaN transistor can keep E-mode operation at the gate length of 0.62 μm, and the simulation result is in accordance with the experimental report result. As the gate length decreases, the short channel effect becomes severe and is able to change this E-mode device to depletion mode operation. The introduction of the vertical scaling technique is beneficial to suppress short channel effect to maintain the E-mode operation even if the gate length scales to below 100nm gate length. This detailed study in N-polar GaN-based transistors establishes technological base for further development of field effect devices based on N-polar III-nitrides.

Keywords-GaN; short channel effect; III-nitrides; MISFET; enhancement-mode

I. INTRODUCTION

The unique properties of Group III-nitride-based semiconductors have fueled their use in many different applications. These semiconductors are characterized by outstanding electronic and transport properties. Hall mobility in excess of 2000 $cm^2/V{\cdot}s$ and carrier densities in excess of 1.2×10^{13} cm^{-2} are reproducibly obtained in AlGaN/GaN heterostructures, which has allowed very intense research on conventional depletion-mode (D-mode) GaN-based heterostructure field-effect transistors (HFETs) have been made reliable enough for practical application [1-3]. Thus, the development of enhancement-mode (E-mode) GaN HFETs has become essential to expand the range of their applications. E-mode GaN HFETs enable a circuit to be simple, because the voltages applied to the gate and drain electrodes can be of a single polarity, and safety components can be omitted[4,5].

There are several methods to be presented to obtain E-mode GaN-based FETs. Typical methods to obtain E-mode GaN FETs are gate recess etch, thin gate barrier layers, and Fluorine-ion treatment[6-8]. The new concept of polarization engineering is introduced and applied in the realization of an E-mode device. The lattice mismatch between GaN and the ternary compound AlGaN or binary AlN in appropriately designed structures produces strain induced polarization fields[9,10]. A compound material stacks like sandwich can be utilized to offset polarization fields from the two interfaces in order to deplete two-dimensional electron gas underneath the gate to realize the E-mode operation[11]. It is not certain whether this kind of device can work in E-mode operation as the gate length enters nano-scale region as well.

Here, we report E-mode N-polar GaN FETs with self-aligned regrown source/drain regions. Using the SILVACO TCAD, the transfer characteristic and output characteristic for device with 0.62 μm gate length are investigated and compare with experimental data. In order to increase operating frequency, transfer characteristic with different gate length is investigated. A technique to suppress short channel effect is presented when the gate length deceases to the nanometer scale.

II. DEVICE STRUCTURE AND MODEL DESCRIPTION

The cross-sectional views and band diagrams of self-aligned device with source/drain regrowth are shown in Fig.1(a) and Fig.1(b). t_{GaN} is used to represent the thickness of the GaN channel. The fabrication process is presented in detail in [11].The two fields from polarization effect respectively between in the GaN/AlN/GaN layer are offset to deplete the two-dimensional electron gas underneath the gate, meanwhile 2DEG under both the sidewall access and source access regions is maintained because of the removal of the AlN layer from the access regions, as shown in Fig.1(b).

A two-dimensional device simulator SILVACO ATLAS, a powerful tool for the modeling of hetero-junction, is employed to model III-V semiconductors[12]. The GaN channel is 20 nm thick with a 2 nm AlN back barrier. An AlN capping layer with 2 nm thickness is used

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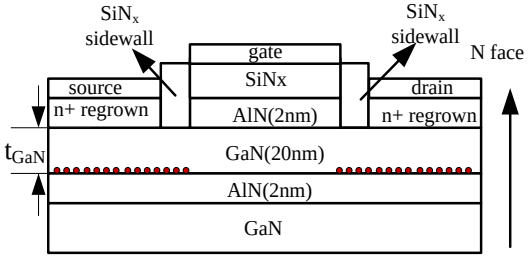
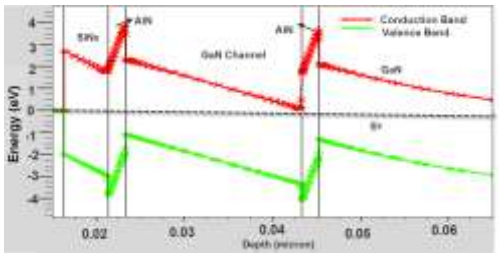
to deplete the 2DEG due to offset of polarization-induced fields between GaN/AlN barrier layer and GaN/capping layer AlN. A graded heavy n-doped InGaN (40 nm) with a density of 2×10^{19} cm^{-3} in the drain and source region reduces the access resistance. The GaN subtract concentration is set as 1.5×10^{18} cm^{-3}.The thickness of 5 nm nitride is taken as gate dielectric layer. We include the low field mobility model proposed by Albrecht[13], which is specified to describe the mobility dependence on the doping and lattice temperature in GaN. A high field mobility is employed to describe the electron drift velocity versus applied electric field for ternary or binary III-Nitride compound[14].



(a)



(b)

Figure 1. (a) Schematic of the device cross section, (b) Band diagram underneath the gate region

Macroscopic polarization P of III-V nitrides consists of two components, one is the spontaneous polarization P^{eq} in the equilibrium structure, the other is strain induced or piezoelectric polarization without presence of external fields. The total piezoelectric polarization δP is expressed as[15]

$$\delta P_i = \sum_j e_{ij}\varepsilon_j \tag{1}$$

ε is strain, e_{ij} is the piezoelectric tensor. If it is restricted to consider the polarization along c-axis, the spontaneous along z axis is $P^{eq} = P^{eq}\hat{Z}$ .This expression will be simplified as

$$\delta P = e_{33}\varepsilon_3 + e_{31}\varepsilon(\varepsilon_1 + \varepsilon_2) \tag{2}$$

$$\varepsilon_3 = \frac{c - c_0}{c_0}$$

$$\varepsilon_1 = \varepsilon_2 = \frac{a - a_0}{a_0}$$

where ε_3 is the strain along the axis, ε_1 and ε_2 is the in-plain strain. a_0 and c_0 are the equilibrium values of the lattice parameters. The relation between the lattice constants of the hexagonal GaN is given as

$$\frac{c - c_0}{c_0} = -2\frac{C_{13}}{C_{33}}\frac{a - a_0}{a_0} \tag{3}$$

where C_{13} and C_{33} are elastic constants. Combining (2) with (3), the amount of the piezoelectric polarization in the direction of the c-axis can be determined by [16]

$$\delta P = 2\frac{a - a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) \tag{4}$$

TABLE I gives all the parameters related to the polarization. Surface charge at the GaN/AlN barrier layer interface is assumed to 5.23×10^{13} cm^{-3}.The self-heating effect is not included in simulation.

TABLE **1**. Simulated parameters for GaN. Spontaneous polarization (in units of C/m^2),and piezoelectric constants (in units of C/m^2), lattice parameter (in units of Å) [15,16]

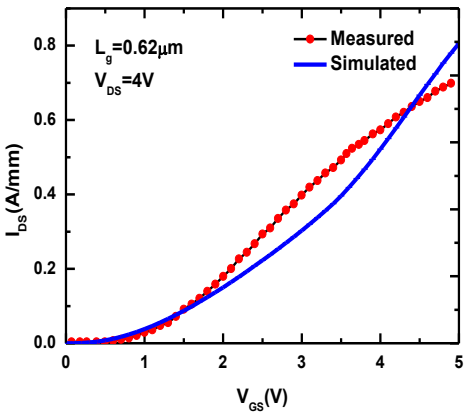
	P^{eq}	e_{31}	e_{33}	c_{13}	c_{33}	a_0
GaN	-0.029	-0.49	0.73	103	405	3.189

III. SIMULATION RESULT AND DISCUSSION

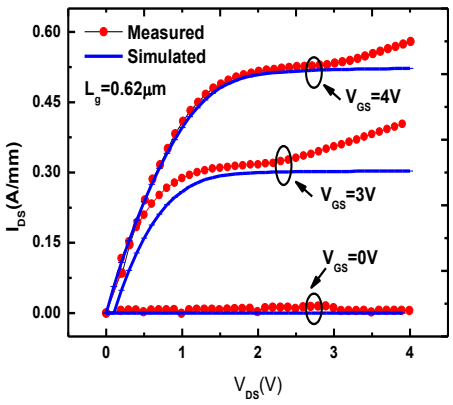
Transfer characteristic and output characteristic for AlN/GaN/AlN MISFET devices with 0.62 μm gate length have been carried and compared with the reported experiment result. The device exhibits the enhancement operation mode with a threshold voltage of about 0.7 volt, which is extracted when current exceeds certain value, as shown in Fig.2(a). It shows that the experimental data is higher than simulated data in the gate voltage range from 1.5 volts to 4.3, and is lower than simulated data over 4.3 volts. The reason is that, in the low field mobility expression[13], there are two terms proportional to lattice temperature and one term inversely proportional to lattice temperature. The increase in temperature due to self-heating effect plays major role in enhancement of mobility in the gate voltage range from 1.5 volts to 4.3. On the contrary, above 4.3 volts, the decrease in mobility caused by self-heating temperature outweighs the increase in mobility. The maximum drain current at V_{GS}= 4 volts is 0.6 A/mm for experiment result, which diverges from the simulated result as the drain-source voltage increases to a certain data, as shown in Fig.2(b). It is because of short channel effect result from drain induced barrier-lowering effect (DIBL). The simulation shows accordance with the experimental finding.

The gate length is a key parameter to improve trans-conductance and dynamic characteristics of the device. Fig.3 gives the transfer characteristics of the devices in the case of different gate lengths. Drain bias is set as 4 volts. The threshold voltage begins to shift negatively as the gate length decreases due to short channel effect. At

the gate length of 70 nm gate length, the device even cannot be pinched off at all. Higher operation frequency of the transistors requires the decrease of the gate length. When the gate length decreases to a certain length, the drain voltage plays more roles. The drain-induced electric field prevails over the gate-induced field at a critical point, gate voltage is incapable of depleting the carriers. As the consequence, the drain-induced electric field



(a)



(b)

Figure 2. (a).Comparison of I_{DS}_V_{GS} curves of device with 0.62μm gate length, (b).Comparison of I_{DS}_V_{DS} curves of device with different V_{GS} bias.

sweeps carriers directly towards the drain and current starts to flow. This short-channel effect results in a severe reduction in modulation efficiency. As a consequence, a negative shift of the threshold voltage, increase of subthreshold current can be discovered.

The aspect ratio L_g/t_{GaN} plays key role in predicting the short-channel effect, L_g is the gate length. It has a direct effect on the DC and RF characteristics. To suppress the short channel effect, a critical aspect ratio has to be held to suppress the short channel effect [17,18]. Hence, in order to hold the device aspect ratio high to avoid the short channel effect and improve high RF performance in nano-meter scale gate length, the vertical dimension of the device is necessary to be scaled. It is shown that the threshold voltage begins to become positive as GaN channel thickness declines, as shown in Fig.4. It means the gate voltage can control more charges in the channel region. Hence, the maximum trans-conductance increases from 250 S/mm to 370 S/mm with the decrease of GaN channel thickness.

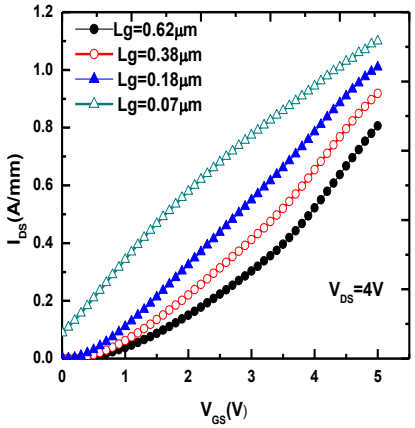


Figure 3. I_{DS}_V_{GS} curves of device with different gate lengths

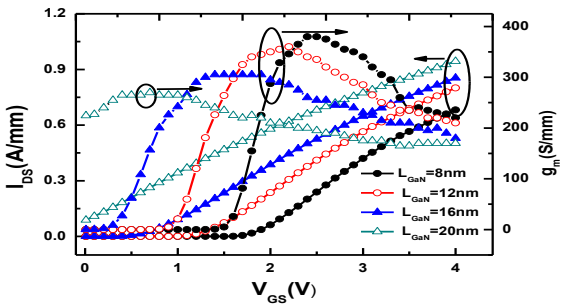


Figure 4. I_{DS}_V_{GS} curves of device with different GaN channel t_{GaN}

IV. CONCLUSION

A numerical study for E-mode N-polar GaN metal-insulator-semiconductor field effect transistor with self-aligned source/drain regions is performed with SILVACO TCAD. A positive threshold voltage of about 0.7 volt from the transfer characteristic is obtained at the gate length of 0.62 μm, a maximum 0.6 A/mm from output characteristic curve is achieved as well. The simulated result has a satisfied agreement with the reported experimental result. The fact that E-mode device suffers from severe short channel effect leads to its operation transforming from E-mode to D-mode at 70 nm gate length. Further vertical scaling technique is capable of keeping the E-mode operation even gate length scales into sub-100-nm dimensions. It becomes a promising technique for integrating with D-mode devices to realize novel circuit functionalities.

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