Radar tracking control system design for phase comparison ranging

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Abstract—This paper describes the structure and performance of phase comparison ranging radar, and mainly discusses its application in the continuous phase phase comparison ranging radar, introduces the basic working principle of phase comparison ranging radar, analyzes the hardware configuration and software design of radar tracking control system based on DPS, as well as detailed discusses the design and implementation of the software in section. The test results show that the whole system has better met the design requirements.

Keywords- FFT; continuous wave ; phase comparison ranging radar ; LPI

I. INTRODUCTION

Phase comparison ranging radar is produced by AD company in the United States; it's a high-performance 32-bit floating-point processor, i.e. a single chip integrated with a strong fire floating point capabilities microprocessor core , 1Mbit zero wait SRAM, various forms of external interfaces and separate I / O controller , hence constitute a complete system , Super Harvard Architecture (SHARC) Cache CPU and high-speed instruction that make the instructions of phase comparison ranging are all single-cycle instruction; 6 separate sets were used in the program memory (PM) and data storage area (DM), while the data can be stored and accessed; optimized DMA and interrupt transmission mechanism make data exchange independently and parallel with computing processor cores process; host interface and bus arbiter could make multi-chip processor become a multi- processor array without any additional resources . The processor is suitable for a variety of high-performance digital signal processing tasks and could composite a multi- processor array. The main features of the phase comparison ranging radar include:

A. kernel operating frequency in a frequency : 600MFLOPS (millions of floating point operations per second) floating point peak ; monolithic unit 1024 -point complex FFT can be completed only in 92 us.

B. 32-bit single-precision (or 40 -bit extended precision) IEEE floating-point DSP processor core ; There are three separate computer unit associated (respectively, the arithmetic / logic unit , multiplier and shifter) ; complete arithmetic instruction set ; 16 general purpose registers ; All arithmetic instructions are single cycle instructions ; support pending loop execution and conditional branching .

C. 2M/1M within dual-port integrated zero -latency SRAM memory, which is divided into program memory (PM) and data memory (DM). Dual-port design allows DSP processor core, DMA controller, and I/O processor quickly access the memory independently.

D. two identical arithmetic processing unit that support a single instruction multiple data (SIMD) architecture ; using a parallel bus structure, it can execute within a time period a multiplier ALU arithmetic operation , but also can conduct a dual-port SRAM reading or writing operation.

E. same sets address generating unit that effectively supports SIMD architecture, supports circular buffer addressing, broadcast addressing and bit reverse order addressing and a variety of addressing modes, which very suitable for T digital signal processing.

F. I/O processor independent from the processor core, which has a DMA control , memory map and external communication function; 14 DMA channels used in conjunction with a dual-port SRAM , and thus achieves parallel transmission of the internal memory and external memory , the external auxiliary equipment, host , serial ports , chain junction without affecting the operation process of DSP processor cores ; 8 serial ports and 2 chain junctions composed of point to point connection are easy to construct multi-processor systems.

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II. The Basic Principles of Phase Comparison Ranging Radar

Continuous wave phase comparison ranging radar completes the measurements of targets distance, speed and other parameters in the frequency domain. Assuming two continuous sine waves with transmitting frequencies f0, f1 with the different frequency of A f, where Af = fl-f0. In order to facilitate the discussion, all were taken as 1 signal amplitude. Due to the Doppler effect, the frequency of the echo signals has shifted. The signal receiver distinguished two echo signals by mixing， low pass filtering , orthogonal dual-channel processing , A / D conversion , and get two Doppler signal frequency discrete domains . Do FFF process for xO (n) and xl (n) respectively, and search the peak position. According to the peak position, we can get the radial velocity of targets and thus determine the phase of peak position. Using the phase difference between the two we can get the target distance corresponding to each other. The radar of this type in the electromagnetic interference environment has a better low vision and anti-jamming capability , especially in speed measurement , phase ranging radar is more superior ; there was no shelter from the pulse radar when ranging ; transmitting power of transmitter is low, so that the receiver can not effectively track,hence the strong anti-interference ability achieves a low probability of intercept; phase ranging radar has a narrow receiver bandwidth, with good self-test capability in the electromagnetic interference background; it reduces the microwave receiver loss, and can detect smaller targets , which makes tracking radar distance meet the technical and tactical requirements.

III. Hardware and Software Design of Tracking Control System

Tracking control system gives real-time target speed, distance , angle, signal to noise ratio and other information, and is able to control the radar servo system so as to enable tracking radar always live . Design of the system includes hardware design and software design .

A. Hardware Design

The main principle of the tracking control system hardware includes four parts: a data latch circuit , FIFO memory circuit , count control circuit , DSPS small system, in which DSP minimum system also includes three main components: ADSP21161, EEPR0M and SDRAM .

The front end of the data acquisition module conducts for mixing, filtering, A / D conversion, and a series of processing of the radar echo data, and outputs the temporal discrete Doppler shift signal. Data latch circuit will latch a discrete Doppler shift signal inputted by the front end, and input the required data into the FIFO memory circuit. FIFO memory circuit will store the required processing data and is under control of the count control circuit. When the count control circuit reaches the set count value, FIFO stops writing data while the count control circuit generates an interrupt signal to the DSP. When the measurement is started, the system receives a set of control parameters from inhaled computer, and count control circuit is initialized. Upon receiving an interrupt signal sent by the count control circuit, the system begins to read echo wave radar data preprocessed from the FIFO memory circuit , then conducts FFF and a series of digital signal processing; in the conclusion, it will generate the target speed , the phase difference and the signal to noise ratio and other parameters, which will be sent using host interface of the system to the embedded computer, so as to calculate the elevation and azimuth error, and send to the servo system, hence the track has always been alive with S target, and real-time displays on the terminal about target parameters . EEPROM is used to store a number of software code and data as procedures required. SDRAM is used to solve memory capacity shortage for the real-time signal processing system.

B. Software system design

All program code of tracking control system are stored in EKPROM; when the system is in power, it will through BMS pin signal to automatically select EEPROM for auto loader.

After the boot process is complete, the system first through the dual-port RAM to receive set control parameters from the embedded computer - , including operational points, such as FFT operations. Then initialize the count control circuit; when the data FIFO reaches operational requirements, count control circuit sends an interrupt signal to the system, the system began to read the target echo data that has been preprocessed from the FIFO memory. After completion of data acquisition, in order to reduce side lobes, before the FFT operation we need to conduct Window treatment on the raw data. Window function required and desired rotation factor required by FFT operation are placed in the EEPROM, after completion of the program we will use DMA to import them into SDRAM.

According to the different actual uses, in order to achieve the best effect, we can change the number of FFT points. If the 1024 point or FFT points are relatively small, all the processing can be done in the SRAM using FFT algorithm -2 decimation. If 16384 point and FFT points are relatively large, SRAM capacity is insufficient to handle all at once , when FYT first use frequency- domain samples , then the time -domain samples , and the final reordering to obtain normal sequence of FFT output bit.

System can directly access to the SDRAM , but in the case of relatively large FFF points, there often have large amounts of data need to be exchanged between SRAM and SDRAM; if use CPU to direct access to SDRAM, and with SDRAM in maximum operating frequency of 166MHz, we need about 13 instruction cycle transmission data . If use DMA for transmission of data, under the same conditions, a data transmission requires only one instruction cycle. Moreover, transmission of data using DMA can also takes advantage of parallel operation of the CPU and the DMA transfer so as to further improve the processing efficiency. In addition, the system supports chained DMA: it can automatically transfer multi-section data in the case of CPU operation without interruption. In this system, the transmission data uses the DMA mode quite often.

After FFT processing, radar echo wave data has been converted to the frequency domain. Systems based on the results of FFT will further estimate the power spectrum, and start tracking control based on power spectrum estimation.

When radar finds the target at first, it is impossible to enter the track condition immediately. At this stage the radar is in the target capture state. In this case, the above system using the estimated power spectrum to search peak from a initial velocity window sent by embedded computer, and calculate SNR; for a given SNR threshold to determine whether the current search is a valid peak speed point . If it is an effective velocity point , we use the energy center of gravity method for the spectrum correction, and by the corrected spectral peaks to calculate corresponding speed value, so as to obtain a more accurate real-time parameter ; if the point is invalid , then the radar has not found the target. Using this approach, after we have obtained several consecutive effective speed points, and after the target registration, we identify it as target acquisition success. In order to prevent glitches, do not search peaks in the vicinity of the zero-frequency. After a successful target acquisition, tracking control system shifts into the target tracking stage. First, according to several speed points, using the least squares algorithm to estimate the speed value for the next moment, in which the predicted rate of participation points and the order of least squares prediction may vary depending on the application. Then the system uses the estimated power spectrum data and the predicted speed value to search peak in the center range of the speed predictive value , uses the SNR threshold to determine the current peak is a valid point or not. If several consecutive invalid speed points appear, it indicates the tracking target has been lost, then system re-enters the target acquisition state; If a few consecutive effective speed points appear, then it means the current radar target tracking is in good condition. To reduce interference and improve processing efficiency, the speed search range can be gradually reduced; to give an accurate velocity value, discard some speed points long from the current measurement time, and only use last few effective points to predict speed value the next time.

In addition to fore mentioned speed parameters, the system also calculates the pitch peak phase , the orientation phase , SNR and other parameters based on the peaks it searched, and uses the host interface to send result parameters into embedded computer , for the completion of the target distance measurement and pitch error angle , calculate azimuth error angle calculation .

After system testing, the tracking control system is better able to perform real-time processing of radar signals. Distance, speed measurements have reached a relatively high accuracy, and can simultaneously track multiple targets, hence meets the design requirements of the system.

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