Design and Experimental Study of Three-level Inverters

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***Abstract*—Three- level inverters has small harmonic component, torque ripple, high utilization rate of DC side voltage which is widely applied in active power filter system, middle, high voltage high power drive, flexible AC power supply system and becomes the research hotspot. Based on the diode clamped Three- level inverters regarded as the research object, the mathematical models of the voltage space vector modulation algorithm simulation and result analysis, simulation results show that the optimal voltage space vector modulation algorithm based on look up table is feasible, the design of FPGA three-level inverters system based on hardware circuit, taking the use of HDL, we designed the part of software, according to the design method of top-down design of space voltage vector signal generator IP core, finally the program is downloaded to the experimental development board in order to verify the IP core, the verification results show that the algorithm has real-time, high reliability, meet the real-time requirements of the system.**

Keywords-three-level inverters; SVPWM; FPGA; signal generator

I. INTRODUCTION

In the 80's of the last century, Japanese scholars A.Nabae et al first proposed the neutral point clamped inverter (NPC-INV)[1-3], pointed out the development direction of high voltage, high power converter device. Prior to this, the main technical bottlenecks of such devices from the main switch devices and micro controller, because at that time the thyristors switch frequency limit as main switch device of power electronic devices are less than 10kHz, can not rely on the carrier frequency controller and effectively restrain the harmonic, but depends on the method of neutral point clamped the output voltage of the converter is composed of two levels rise three levels. Nowadays, various kinds of new power switching devices continue to emerge and the successful application with digital signal processor in the electric field, the NPC-INV circuit is not only shelved, but has been widely applied in high power frequency fields [4].

Presently there are many implementations of SVPWM modulation strategies [5]. This design adopts FPGA to realize the diode clamped three-levels SVPWM inverter system, this method makes the system more reliable and stable than the traditional method and the use of peripheral devices greatly reduced. It also has the advantage of high flexibility, high precision and fast response characteristics as the DSP [6].

II. THREE LEVEL SVPWM MODULATION STRATEGY MODEL SIMULATION

Diode clamped three-level inverters (DCT-INV) is one of the NPC-INV circuit topology which is developed the earliest and the most mature [7]. Topological structure as shown in "Fig. 1" of the DCT-INV.

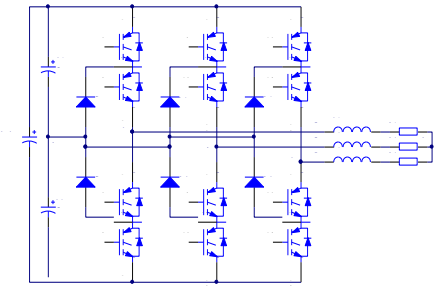

Figure 1. DC-INV main topology

Three level voltage space vector for:

$$V(K)=\frac{1}{3}U_d\left(S_a+S_b e^{j\frac{2}{3}\pi}+S_c e^{-j\frac{2}{3}\pi}\right) \quad (1)$$
$$=\frac{U_d}{6}\left[(2S_a-S_b-S_c)+j\sqrt{3}(S_b-S_c)\right]$$

From the formula we can calculate the amplitude of the 19 voltage vectors. As the amplitude of synthetic vectors of each are not identical, we can divide the vector into three categories: 2/3Ud, $\sqrt{3}/3U_d$ and 1/3Ud, the diode clamped three-level inverters 27 (plus 8 redundant short vectors) voltage vector distribution as shown in "Fig. 2".

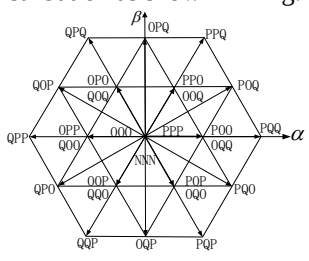

Figure 2. Voltage space vector diagram of distribution

As shown in "Fig. 2", the 6 outermost (PQQ) vector magnitude 2/3Ud is called the long vector; vector magnitude

$\sqrt{3}/3U_d$ is called middle vector; vector magnitude 1/3Ud as the short vector. Three in the switch state of origin is called the zero vector. The NPC inverter 27 space voltage vector according to the different vector classifications summary "TABLE. I".

TABLE I. THREE LEVEL SPACE VOLTAGE VECTOR CLASSTFICATION

Vector types		Voltage vector
long vector		PQQ PPQ QPQ QPP QQP PQP
middle vector		POQ OPQ QPO QOP OQP PQO
short vector	positive short vector	POO PPO OPO OPP OOP POP
	negative short vector	OQQ OOQ QOQ QOO QQO OQO
zero vector		PPP OOO QQQ

Carries on the division to the sector, according to the traditional algorithm of "Fig. 2" can be divided into 6 regions; each region according to the vector rules is divided into 4 regions, as shown in "Fig. 3" shows [8-10]. On 27 basic space vectors, in order to better use, the article on the basis of regions partition and puts forward a new classification method, a large sector is divided into 6 small sectors, with I, II, III, IV, V, VI regions, with 1, 2, 3, 4, 5, 6 internal I district 6 small regions, as shown in "Fig. 4" shows.

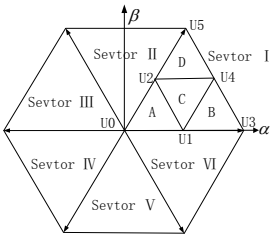

Figure 3. The traditional SVPWM algorithm

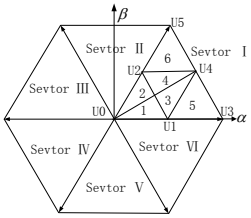

Figure 4. Improved SVPWM algorithm

The precise division sector brought convenience to the simulation and signal processing sector judgment. As shown in "Fig. 5", assume that synthetic reference voltage vector V_{ref} argument for the θ ($0 \le \theta \le 60$ °), according to the argument of θ system we can determine the V_{ref} falls in the I sector, and then according to the amplitude of the reference voltage vector judgment synthesis of specific V_{ref} in which a small sector, projection V_{ref} in the α and β axes are respectively V_α and V_β, for $V_\alpha = V_{ref}\cos\theta$, $V_\beta = V_{ref}\sin\theta$, we can know the synthesis of the reference voltage vector V_{ref} falls in the I sector of the fifth district, the synthesis of the reference voltage vector falls in the judgment principle other small area and the similar process.

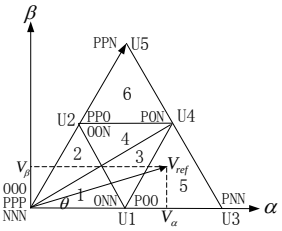

Figure 5. SVPWM area of judgment

We apply the MATLAB/SIMULINK simulation tool to simulate the lookup table optimization SVPWM. "Fig. 6", "Fig. 7" for SVPWM control voltage and current waveform diagram method, "Fig. 8" is the graph spectral FFT transform.

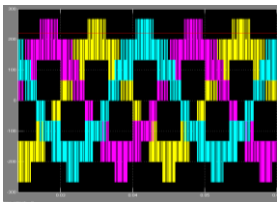

Figure 6. The inverter output voltage waveform of phase

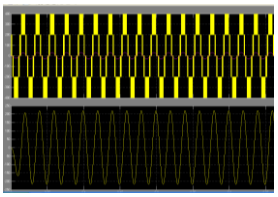

Figure 7. The filtered A phase line voltage, line current waveform

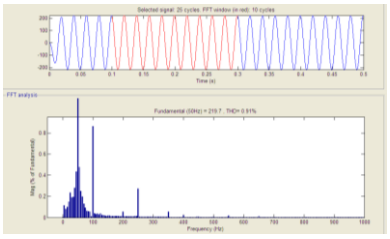

Figure 8. Voltage and FFT spectrum of SVPWM mode

From the simulation waveform we can see that DCT-INV without filter line voltage is five level ladder waves, sine wave we need to get through LC low-pass filter, what can be seen from "Fig. 8" is the harmonic content of output voltage is less than 1%, so improved SVPWM modulation algorithm based on look up table can be applied to the diode clamped three- level inverters.

III. DESIGN OF SVPWM SIGNAL GENERATOR

A. Design Of The Hardware Circuit System Of Three Level Inverters

The hardware system of the diode clamped three level inverters is mainly composed of two parts: the main circuit

and control circuit. Through the transformer acquisition input DC voltage signal. the output current signal, after A/D conversion to FPGA [11], processing algorithm within FPGA, then the FPGA output 12 channel PWM signal, control signal through the HCPL-361J drive chip to control the IGBT on-off, when IGBT fault occurs, the fault signal driver chip back to the processor, consisting of a single loop control system. The system hardware block diagrams shown in "Fig. 9".

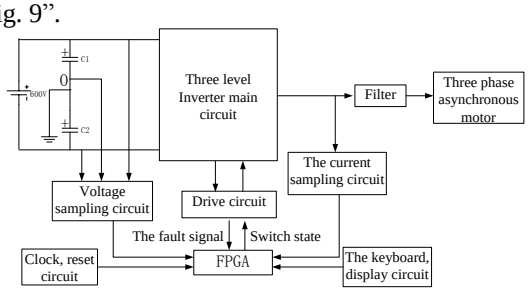

Figure 9. Control system hardware block diagram

B. *The Design Of SVPWM IP Core*

FPGA implementation of vector control algorithm of voltage space overall block diagram is shown in "Fig. 10". Including the SVPWM signal generator: sector judgment, reference vector rotation, vector calculation time, district judge, the switch sequence distribution, mapping and transformation as well as the PWM unit [12].

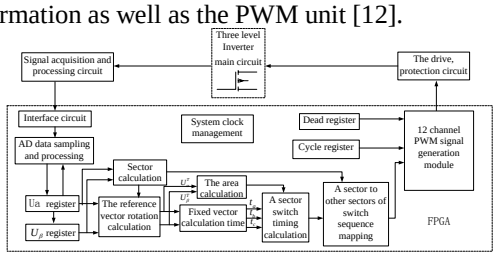

Figure 10. Schematic diagram of SVPWM signal generator

C. *AD7656 Sampled Data Control*

From the control system hardware circuit, we know that AD data acquisition and processing unit is the focus of the design, the sampling precision, processing speed directly influences the realization process of SVPWM control algorithm. FPGA received to AD7656 data achieve state machine programming. The six state of the state machine for ST0, Start, Judge, Waiting, Read, Stop. Finite state transfer of AD7656 as shown in "Fig. 11".

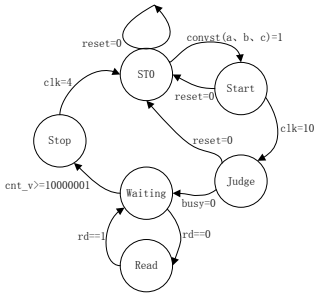

Figure 11. AD7656 finite state transition diagram

Reset is the system reset signal, ST0, Start, Judge three state in the transition process if reset=0, state machine that is returned to the idle state, waiting for the system to give the starting signal. AD7656 Verilog compiler, synthesis and simulation in the Quartus II, constraints and timing simulation in Modelsim, timing simulation waveform as shown in "Fig. 12".

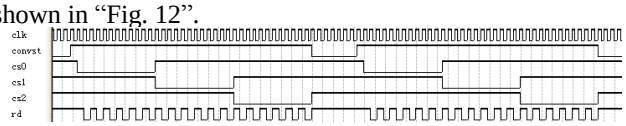

Figure 12. Verilog HDL AD7656 sequence diagram

D. *The Pulse Generating Module Design*

Pulse generating module consists of a triangular wave counters, comparators, and dead time generator. "Fig. 13" is a Modelsim three-phase 12 road simulation waveforms based on PWM.

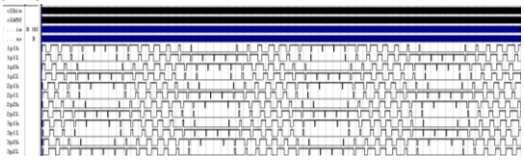

Figure 13. 12 PWM timing simulation waveform

At any time DCT-INV circuit in the switching state always has two main switch is turned on, the other two main switch complementary off state, in the actual pulse distribution in the control process, in order to prevent any one single bridge arm short, must carry on the pulse distribution strict to 12 main switch device, and follow the principle of control BBM, oscilloscope to measure the actual dead zone protection waveform as shown in "Fig. 14", which point potential unbalance or IGBT failure FPGA blockade of PWM measured protection signal as shown in "Fig. 15".

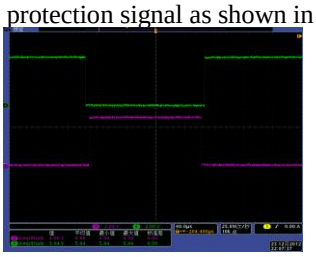

Figure 14. The measured waveform of dead zone protection

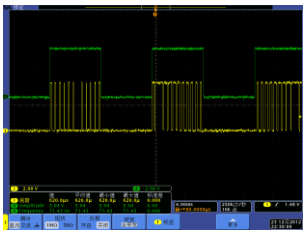

Figure 15. Measured PWM blocking protection signal

IV. EXPERIMENTAL RESULTS AND ANALYSIS

The design of the experiment is based on DCT inverter hardware EP2C35F484C8N experimental system, the main

circuit of the IGBT selected Infineon company BSM150GB-120DN2, clamp diode with fast recovery diode DD50N12 company Eupec SVPWM, the improved optimization algorithm is verified, the modulation of PWM than M=1.0, the output frequency of the inverter is 50Hz.

Using Verilog HDL hardware description language for the part of software design in Quartus II + Modelsim, according to the design method of top-down design of SVPWM signal generator of IP kernel, and the program is downloaded to the board to verify the IP kernel, “Fig. 16” is the measured IGBT PWM control trigger pulse, “Fig. 17” – “Fig. 19” for the inverter output some waveforms.

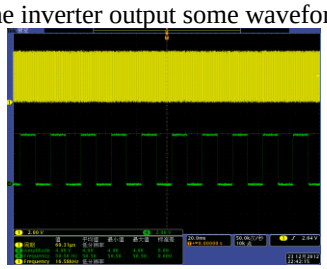

Figure 16. PWM control trigger IGBT pulse sequence

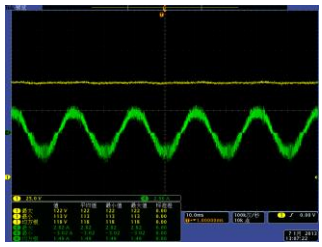

Figure 17. The DC side voltage, current

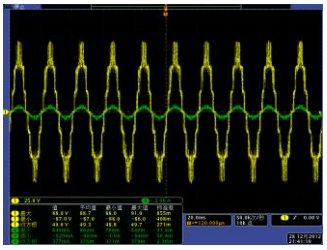

Figure 18. A inverter output phase voltage waveforms

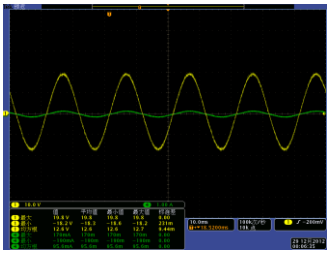

Figure 19. After LC A inverter output phase voltage waveforms

The measured output voltage waveform of the inverter and the SIMULINK simulation comparison, measured waveform well validate the simulation waveform of the mathematical model, the result shows that the algorithm has good real-time, high reliability, meet the requirements for the algorithm design of DCT-INV control system.

V. CONCLUSION

Design in-depth study on three-level inverters, the diode clamped three-level inverters is used in the hardware design, software realization part with hardware description language for programming and debugging. Based on the mathematical model of DCT-INV research, the construction of the hardware system, the software part of the simulation results show that, the system of SVPWM three-level inverters to realize the design of inverter output voltage waveform similar to the sine wave, low harmonic content, neutral point voltage balance improve obviously advantages, with advanced technology, digital control, reduce the modulation strategy the loss of the system, the real-time control get better realize the advantages, and has great application value and broad market prospect.

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