An 1GHz~6.25GHz Phase-Locked Loop for SERDES

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Abstract. An 1GHz~6.25GHz phase-locked loop (PLL) for SERDES is presented in this paper. For achieving optimized balance between acquisition speed and jitter performance at all frequency points, this PLL adopts an adaptive bandwidth method. A current-programmable charge pump is introduced to make loop bandwidth configurable. And a novel Current Controller module is used to output configurable codes automatically. This PLL is implemented in 65nm, 1P10M CMOS technology, occupying an area of 0.17mm^2. Results show its charge pump can draw 20uA to 420uA currents from 1.2V supply, proportional to changeable bandwidth 3MHz~58MHz. The measured jitter and locking time at 6.25GHz are 5.52ps and 9.5us, respectively.

Keywords: PLL, SERDES, adaptive bandwidth, acquisition speed, jitter performance.

1. Introduction

SERDES (SERializer-DESerializer) transceivers is widely used in data communications of ADC/DAC and FPGA [1-2]. Phase-locked loop (PLL) is commonly used as a frequency synthesizer to provide the clock for transmitting and receiving functions of SERDES. With data throughput increasing, more stringent lock and jitter requirements are imposed on PLL.

Previously, designer often optimized individual PLL structure and component to meet above clock requirements. However, it is not well concerned that jitter performance, speed and stability of PLL also heavily depend on loop bandwidth. Adaptive bandwidth technique is important in PLL design[3].

In this paper, detailed theoretical background of PLL and its loop bandwidth is given. And a PLL that supports a wide input range of 1GHz~5GHz, an output frequency range of 1GHz~6.25GHz is proposed. With adaptive bandwidth method, this PLL works well in high-speed and low-jitter area.

The structure is organized as follows: Section 2 briefly reviews PLL and presents importance of bandwidth selection. Section 3 proposes our PLL structure model, focus on our automatic bandwidth programming method. Experimental results are summarized in Section 4. Finally, Section 5 draws conclusions.

2. PLL Architecture

Fig. 1 depicts a typical type2 charge-pump PLL (CPPLL). It contains frequency/phase detector (PFD), charge pump (CP), low-pass filter (LPF), voltage-controlled oscillator(VCO) and dividers [4].

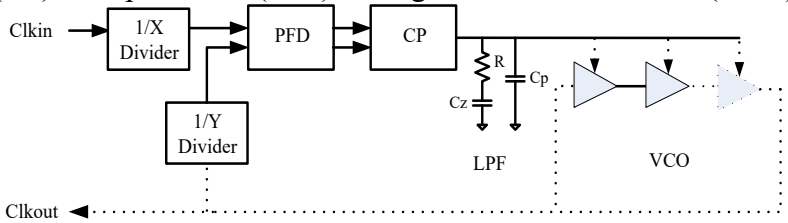


Fig. 1 Typical type2 charge-pump PLL

The Open loop transfer function of this CPPLL is given by

$$H_{open}(s)=\frac{I_{CP}K_{VCO}(1+sRC_P)}{2\pi Ns[s^2RC_PC_Z+s(C_P+C_Z)]} \quad (1)$$

Where I_{CP} is output current of CP, K_{VCO} is the gain of VCO, and N is the dividing factor of divider. R, C_P and C_Z consist of the second-order LPF. We can see Type2 PLL has three poles (two at origin) and one zero [5].

Assuming that the main noise sources of PLL are external reference input noise $\Phi_{n,in}$ and VCO internal noise $\Phi_{n,VCO}$. Then the output noise $\Phi_{n,out}$ caused by them can be expressed as:

$$\frac{\Phi_{n,out}}{\Phi_{n,in}} = N\frac{H_{open}(s)}{1+H_{open}(s)} \qquad \frac{\Phi_{n,out}}{\Phi_{n,VCO}} = \frac{1}{1+H_{open}(s)} \tag{2}$$

We all know that PLL loop bandwidth characterizes speed. But from (2), we can find that the PLL behaves as a low-pass filter to the reference input noise but a high-pass filter to the VCO noise. In other words, PLL phase noise (or jitter) performance also largely depends on the choice of loop bandwidth. There exists a trade-off between the loop bandwidth, jitter performance and the locking speed.

When $C_Z \geq 10\,C_P$, the loop bandwidth BW can be described as follows

$$BW = \frac{I_{CP}RK_{VCO}}{2\pi N} \tag{3}$$

From (3), we can conclude that the loop bandwidth of traditional PLL is fixed, because all circuit parameters won't change once determined. However, in wide-frequency-range applications, constant loop bandwidth is not suitable. When we set the loop bandwidth to an optimum value at one frequency point, it is not the best for other frequency points. For example, if we set the optimized loop bandwidth of 1GHz as all frequencies' bandwidth, this value is too small for 6.25GHz; PLL takes long time for locking and has little jitter reduction of the internal VCO noise. But if we set the optimized loop bandwidth of 6.25GHz as all frequencies' bandwidth, this value is too large for 1GHz, not only leaves much of the input reference noise unreduced, but is very likely to cause PLL unstable. Bandwidth-programmable technique is necessary in PLL design.

3. Proposed PLL

Our proposed wide-frequency-range PLL is a second-order PLL using a tri-state PFD, an 1/1.25 divider and a three-stage ring VCO. It achieves adaptive bandwidth by adaptively programming current of charge pump with a current Controller module. The following will focus on the design of CP and Current Controller.

3.1 Charge Pump

The structure of CP is shown in Fig. 2, M1 and M2 are current transistor; M3~M6 are switching transistor. The current flows from OUTB to loop filter.

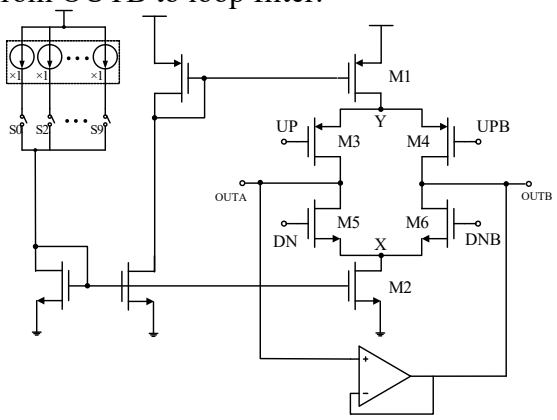


Fig. 2 Charge Pump architecture

There are two issues need to be addressed in the design of CP. First is the wide dynamic range of I_{CP} required to support a wide range of bandwidth. This paper adopts a normal design to solve this

problem: I_{CP} is copied from a series of configurable current sources (using switches S1~S8). But that leads to the second issue. CP's switching transistors should be sized for the maximum current. When CP operates at minimum current, excessive charge injection and feed-through will add reference spurs in output clock. To diminish influence, our CP adopts dual-switch structure to provide another current path when M4, M6 are turned off for reducing charge sharing effect. And a unity gain amplifier is used for reducing voltage overshot.

3.2 Current Controller

The architecture of Current Controller module is shown in Fig. 3; it is composed of 10 same cells. This module receives output of PFD, and automatically generates 10 digital codes to control CP.

The output of PFD controls I_{up} and I_{down}. The initial value of OUT[9:0] are all 1. When powering on, discharging current $I_{down} - I_{up}$ make OUT[0] gradually decrease, OUT[0] is determined by accumulation of time that $I_{down} - I_{up}$ exist. If OUT[0] is discharged lower than inverter threshold, X1 flip, OUT[1] repeat the same process with OUT[0], OUT[1] is determined by accumulation of time in which $I_{down} - I_{up}$ exist from the moment X1 flip; so as the other output nodes. And if OUT[1] is pulled down lower than inverter threshold, Y0 flip, OUT[0] will sharply turn to 0. To sum up, the accumulation of time in which $I_{down} - I_{up}$ exist, or rather phase/frequency difference between PLL input clock and output clock, can be turned into digital codes automatically.

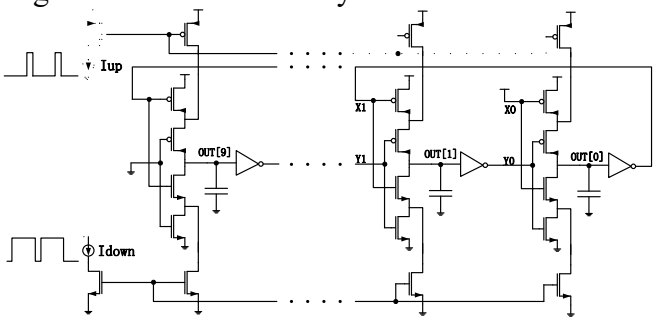


Fig. 3 Current Controller architecture

4. Measured Results

The proposed PLL is implemented in 65nm, 1P10M CMOS technology with a supply voltage of 1.2V. Fig. 4 shows the core chip of this PLL circuit

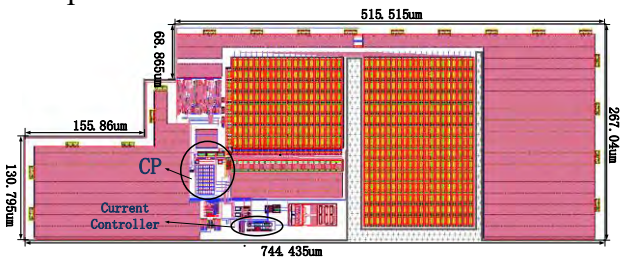


Fig. 4 Layout of proposed PLL

Turning Switches S1~S9 on in sequence, and we sweep output voltage of CP from 0 to 1.2V to see changes of output current. Fig. 5 shows their relationship. The output current can range from 20uA to 420uA with proposed programming method. And CP current can be kept constant within a certain range; dual switches and unity gain buffer make sense.

The change progress of CP current and OUT[9:0] at 6.25GHz is shown in Fig. 6(a). We can see, OUT[9:0] of Current Controller module flip automatically in PLL capture process, and output current of CP also gets larger in turn. Correspondingly, the bandwidth of PLL is broadened. This greatly shortens locking time of PLL. At 6.25GHz, the locking time is only 9.5us. Good jitter performance of proposed PLL is shown in Fig. 6(b). With bandwidth programming method, PLL maximum jitter of 6.25GHz is only 5.52ps.

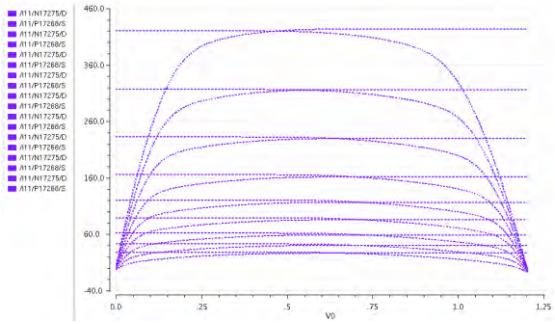
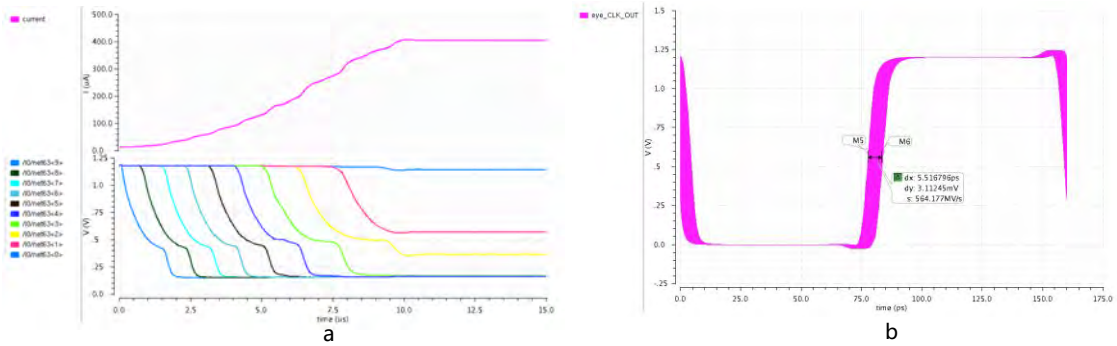


Fig. 5 The relationship between output current and output voltage of CP in different configurations



a b

Fig. 6(a) The change progress of CP current and OUT[9:0] at 6.25GHz
Fig. 6(b) Jitter performance at 6.25GHz

5. Summary

An 1GHz~6.25GHz phase-locked loop (PLL) is proposed in this paper. To trade off jitter performance and locking speed, This PLL uses an adaptive loop bandwidth solution: adopting a current-programmable charge pump to make bandwidth changeable; using a Current Controller module to demonstrate automatic program. Results show this solution works well. Fabricated in the CMOS 65nm 1P10M technology, charge pump can yield currents ranging from 20uA to 420uA, proportional to changeable bandwidths 3MHz~58MHz. The measured jitter and locking time at 6.25GHz are 5.52ps and 9.5us, respectively.

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