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Online Monitoring of MOS Junction Temperature in Power Cycle Test

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***Abstract*—The power cycle test is an important method to test the reliability of the device and eliminate unqualified samples. It is significance to measure various performance of the device. However, the junction temperature of the device changes greatly during the power cycle. Inappropriate high power cycle and duty cycle will make the junction temperature of the device too high, which can directly affect the experimental results and bring about economic losses. Therefore, this paper proposes an online monitoring method of MOS junction temperature during power cycle process, which can effectively prevent the device junction temperature from being too high and at the same time provide an objective basis for the selection of power cycle and duty cycle.**

Keywords—power cycle test; junction temperature; online

I. INTRODUCTION

In the power cycle test, the large pulse power is applied to the device under test, causing the junction temperature of the device to be in an alternating shift of gradually increasing and continuously decreasing, which becomes an important index to evaluate the reliability of the device under test. However, it is very difficult to have a uniform standard for the rated power and power cycle applied due to different devices and different heat dissipation platforms.

Excessive power or prolonged cycle will cause the junction temperature of to exceed the limited temperature, which will affect the reliability of the test results and bring about the risk of thermal failure. Based on the above problem, in this paper, the change of MOS junction temperature during power cycle is monitored online by selecting appropriate temperature sensitive electrical parameters (TSEPs) using electrical method [1]. In order to avoid the interference of test parameters on the power cycle experiment itself, no additional test electrical signals are introduced in the junction temperature test process.

In order to meet the requirements of online monitoring of the junction temperature of MOS devices, the power cycle circuit and the library of temperature calibration curve are optimized.

II. SELECTING TEMPERATURE SENSITIVE PARAMETERS

Selection the TSEPs of MOS devices, many scholars have put forward some useful schemes [2 – 3] in the world, such as, threshold voltage mentioned by H. Chen, V. Pickert [4] and switching current studied by A. Castellazzi [5]. However, the above researchers focused on the junction temperature measurement or the introduction of test signals under on-state of MOS devices, which cannot achieve the trend of online monitoring of junction temperature rise and temperature drop under the power cycle condition. In order to solve this problem, through improving the power cycle test circuit, TSEPs are selected in the power application process and the cut-off process respectively, in order to realize the junction temperature monitoring in the whole power cycle.

During the power cycle, the V_{GS} voltage is constant, two current sources apply a constant current signal to the source and drain of the device, one of which is the power signal I_{MAX} and the other is the temperature drop test signal I_{MIN}. Since $I_{MAX}>>I_{MIN}$, I_{MAX} and I_{MIN} can each correspond to an independent TSEP V_{DS}.

When the device is applied with a power, two current sources work at the same time: $P = I_{MAX} * V_{DS1}$. At this time, V_{DS1} can be used as a TSEP to measure the temperature rise curve of the device. When the power is turned off, the current source is also turned off. The temperature drop curve can be tested by V_{DS2} that is as the TSEP. Since the gate voltage of the MOS is constant throughout the power cycle, the gate voltage cannot be used as an independent TSEP. The test equipment is shown in Fig.1.

FIGURE I. TEMPERATURE CALIBRATION CURVE TESTING EQUIPMENT

$$I_{DS} = \beta[(V_{gs} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2] \quad (1)$$

Since the device operates in the linear region under actual operating conditions, equation (1) can be simplified as follows:

$$I_D = \beta(V_{GS} - V_T)V_{DS} \quad (2)$$

I_{DS} is drain-source current, V_{DS} is drain-source voltage, V_{GS} is gate-source voltage, V_T is threshold voltage, and β is called gain factor:

$$\beta = \frac{\mu_n C_{OX} W}{L} \quad (3)$$

Where C_{OX} represents the gate oxide capacitance per unit area, W represents the channel width, L represents the channel length, and μ_n is called carrier mobility. For equation (2), there are two temperature-related parameters, carrier mobility μ_n and threshold voltage V_T:

$$\mu_n = \mu_n(T_0) \times (\frac{T_0}{T})^2 \quad (4)$$

$$V_T = V_T(T_0) + \Pi(T - T_0) \quad (5)$$

For MOS devices, some studies show that $P < 0$

After finishing formula (2), you can get:

$$\frac{I_D}{V_{DS}} = \frac{\mu_n(T_0) \times T_0^2 C_{OX} W}{LT^2}([V_{GS} - V_T(T_0) + PT_0] - PT)]) \quad (6)$$

In order to simplify the mathematical model, if $\frac{\mu_n(T_0) \times T_0^2 C_{OX} W}{L} = Y$, $[V_{GS} - V_T(T_0) + PT_0] = A$, Y and K are two constant quantities independent of temperature. $A < 0$ when the V_{GS} is smaller and $A > 0$ when the V_{GS} is larger. In the linear region, the ratio of $\frac{I_D}{V_{DS}}$ is a constant value under the same gate voltage and temperature conditions, which can make $\frac{I_D}{V_{DS}} = R_{om}$. Then, according to the above description, it can be obtained:

$$P_{o\mu} = Y\frac{A - PT}{T^2} \quad (7)$$

Available for sorting:

$$P_{o\mu} = \frac{AY}{T^2} - \frac{PY}{T} \quad (8)$$

Because $P < 0$, the R_{om} drops with temperature T rising, and the linear region shows that the slope of the straight line decreases with temperature rising, and the change trend is absolutely monotonous, and the temperature calibration curve shows that there is no influence of temperature blind area.

III. Principle of Power Cycle Circuit and Temperature Calibration Curve

In the application process, only two temperature calibration curves need to be constructed in advance under the specific gate voltage V_{GS}, namely V_{DS2} –T under the I_{MAX} condition and V_{DS1} – T under the I_{MIN} condition. The constant current measurement mode can be used when the power is small under the I_{MIN} condition. The pulse test method must be used to avoid self-heating under the I_{MAX} condition. The test process and results are shown in figure 2 and figure 3.

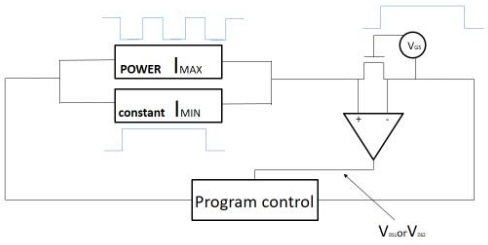

FIGURE II. SCHEMATIC DIAGRAM OF POWER CYCLE PRINCIPLE

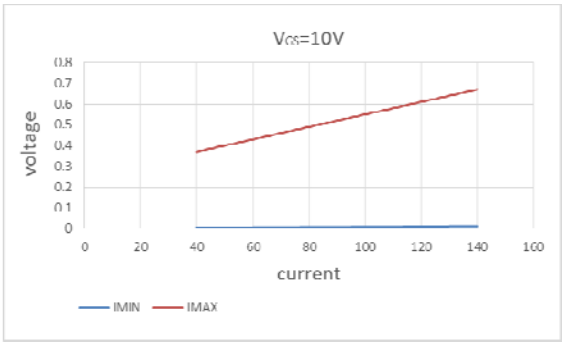

FIGURE III. TEMPERATURE CALIBRATION CURVE DURING POWER CYCLE PROCESS

When power is applied, the first temperature calibration curve can be used to monitor the temperature rise. Under the power off-state, the second temperature calibration curve can be used to monitor the temperature drop trend. In the power application process, the test current source provided the small signal, which has no influence on the working circuit. In the off process, the off-state of the power current source does not interfere with the test signal. Therefore, the above two reasons perfectly realize the aim of non-interference in online acquisition of TSEPs during power cycle.

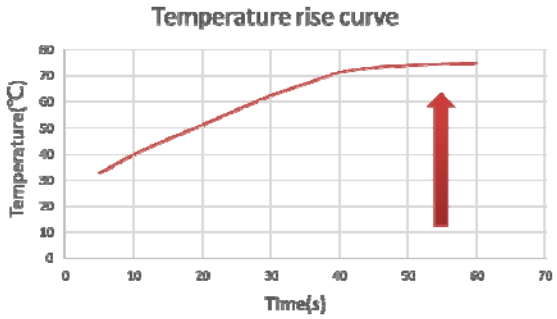

FIGURE IV. SCHEMATIC DIAGRAM OF TEMPERATURE RISE CURVE

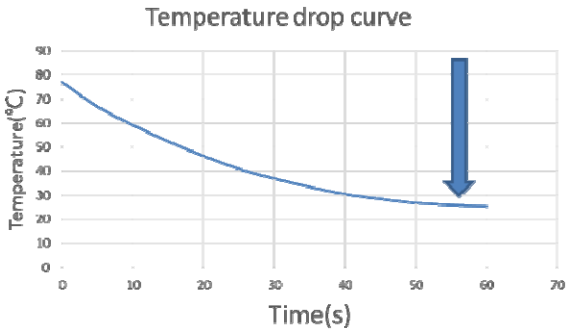

FIGURE V. SCHEMATIC DIAGRAM OF TEMPERATURE DROP CURVE

During power cycle, online monitoring of the temperature rise process and the temperature drop trend have important significance. The junction temperature of the power-induced device increases, and the junction temperature increase causes the load voltage to increase under the constant current condition, thus forming a positive feedback effect of power increase - junction temperature rise - power increase, and the device is easily burnt out of control when the heat dissipation condition is poor. Monitoring the temperature rise state can effectively prevent the failure risk caused by too high junction temperature in time and prevent the junction temperature from being too high in advance. When the power is cut off, the device enters the heat dissipation process, and the too short heat dissipation time will lead to the initial junction temperature of the device not fully cooled when the next power cycle arrives, which will also easily lead to thermal failure.

The temperature rise curve is helpful to control the power cycle and the upper limit of the single power application time avoids the risk of high temperature. The temperature drop curve provides an objective basis for limiting the duty cycle to ensure that the device has enough cooling time to go through the next power cycle under test. Avoiding the influence of too high junction temperature on the experimental results will ensure that the test results obtained by the power cycle experiment are more effective, and at the same time avoid the economic loss caused by high temperature loss, thus having a broad application prospect in engineering.

IV. Conclusion

Aiming at the problem of online monitoring of junction temperature in power MOS device power cycle experiments, through reasonable matching of experimental circuits and selection of appropriate TSEPs, the junction temperature of the device can be measured online without any interference with experimental conditions, and then simplifying the temperature calibration curve and making it more convenient for practical engineering applications. Monitoring the MOS junction temperature is helpful for engineers to master the junction temperature of device, which can avoid failure caused by excessive power and long time, effectively limit the power cycle and duty cycle in the power cycle process, eliminate the influence caused by high temperature damage, and ensure that the experimental results are more accurate and reliable.

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