

The Impact of Dead-time on Synchronous Rectification Circuit Efficiency

Hanshen Wang, Jian Guo, Jingli Gong, Jianfei Chen and Sheng Zhang*

School of Electronic and Optical Engineering, Nanjing University of Posts and Telecommunications, Nanjing, 210003, China.

*Corresponding author

Abstract—In the synchronous rectification circuit, due to the junction capacitance of MOSFETs and other factors, an on-and-off delay problem exists, which further leads to phenomenon of circuit short, circuit heating and inefficiencies. These phenomenon can be reduced significantly by setting an appropriate dead-time to prevent direct conduction from the opposite MOSFETs. However, the current determination of dead-time is investigated mainly empirically and unreasonable setting of dead-time will affect the work of circuit. This paper will discuss the relationship between dead-time and the efficiency of the synchronous rectifier buck circuit, it will draw the conclusion that the increased dead-time can eliminate the self-excited ringing effect and improve the working efficiency of the power supply at low voltage when the output amplitude requirement is satisfied. The experimental verification is carried out with a synchronous rectification Buck circuit with an operating frequency of 20kHz, an input voltage of 20 volts, an output range of 0 to 19 volts and a variable dead-time. The conclusions of this paper are of great significance to the design of power supply circuit, improving its working efficiency and reliability.

Keywords—synchronous rectifier; dead-time; efficiency; ringing effect

I. INTRODUCTION

In the synchronous rectification switching power supply[1,2], the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) [3] with very low on-state resistance is used to replace the traditional rectifier diode, which greatly reduces the loss of the circuit and improves the efficiency of the DC/DC converter. However, whether it is a MOSFET, a GTO thyristor or an IGBT with low on-voltage drop and high input impedance, it has its own junction capacitance and there is an on-and-off delay. As a result of, the two switch transistors of the synchronous rectification circuit conduction simultaneously, and a ringing effect generates[4]. The effect both reduces circuit efficiency and increases the probability of device damage. At present, the method of adjusting the settings of dead-time[5,6] is broadly adopted to avoid the simultaneous conduction of two switching MOSFETs in a synchronous rectification circuit. However, an appropriate dead-time based on PCFF has a great influence on the efficiency of the synchronous rectification circuit[7]. If the dead-time is set too long, the amplitude output range will decrease. If the dead-time is set too short, the circuit will be less efficient. It is studied in this paper that the influence of the setting of dead-time in synchronous rectification circuit on its efficiency.

II. PRINCIPLE AND DESIGN

A. Synchronous Rectification Characteristics

The traditional Buck circuit[8] is shown in Fig. 1. The circuit is mainly composed of a switching transistor Q_1 , a diode VD , an inductor L and a capacitor C .

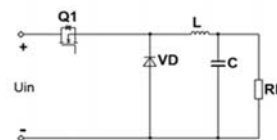


FIGURE 1. BUCK CIRCUIT

When the switching transistor Q_1 is turned on, the diode VD current is zero, and the inductor L current rises linearly. When the switching transistor Q_1 is turned off, the inductor current decreases because of diode freewheeling[9]. Under ideal conditions, no power loss will occur on the diode regardless of whether the switching transistor Q_1 is turned on or off; however, due to the presence of junction capacitance in the diode, the diode takes some time to recover the reverse blocking capability, from forward conduction to reverse turn-off conversion. During that time there will still be current flowing through the diode, resulting in a large loss on the diode. The current waveform during the process of converting the diode from forward to reverse is shown in Fig. 2.

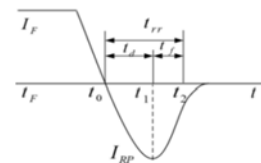


FIGURE II. THE CURRENT WAVEFORM WHEN THE DIODE IS CONVERTED TO REVERSE BIAS

Wherein, $t_d = t_1 - t_0$ is called delay time; $t_f = t_2 - t_1$ is called current fall time; $t_r = t_2 - t_1$ is called reverse recovery time.

It can be seen from the figure that when the diode is converted from forward bias to reverse bias, the forward current I_F gradually decreases to zero. At this time t_0 , since the power diode stores a large number of minority carriers on both sides of the PN junction, reverse resistance is not restored. These minority carriers are drawn out of the diode by the applied reverse voltage, forming a large reverse current, reaching the

peak I_{RP} at the moment t_1 , and then the reverse current drops rapidly; when the diode is conducting, the turn-on voltage drops from 0.6V to 1.2V is generally present. When the circuit passes a large current, the diode will generate a large power consumption, so the traditional Buck circuit is not suitable for working under low voltage and high current. In order to improve the working efficiency under low voltage and high current, people introduce synchronous rectification technology, and the synchronous rectification Buck circuit[10] is shown in Fig. 3.

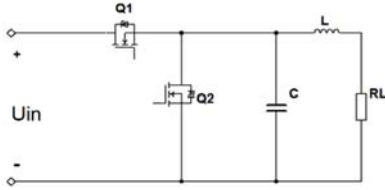


FIGURE III. SYNCHRONOUS RECTIFICATION BUCK CIRCUIT

Synchronous rectification technology takes into account the defects of the freewheeling diode in the freewheeling circuit. The voltage-controlled MOSFET replaces the freewheeling diode. When the switching transistor Q_1 is turned off, the MOSFET Q_2 is turned on to form a freewheeling circuit, which strengthens the control of the freewheeling circuit. Realize the effect of traditional Buck circuit to reduce voltage. When the MOSFET is turned on, the resistance is extremely low. Even if a large current flows, the voltage drop generated on the MOSFET is lower than the on-voltage drop of the diode, and the loss is much smaller than that of the diode, which is suitable for working under the condition of low voltage and high current.

B. Switching Characteristics of MOSFET

Although the efficiency of the DC/DC circuit can be improved by replacing the rectification diode with MOSFET, the technique still has defects, and Fig. 4 shows the switching characteristic curve of MOSFET.

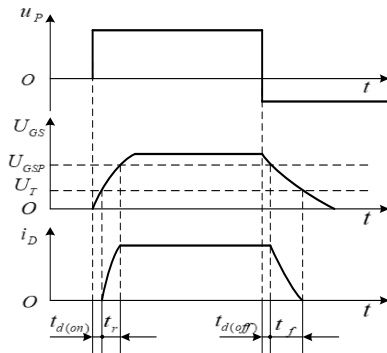


FIGURE IV. SWITCHING CHARACTERISTIC CURVE OF MOSFET

It can be seen that there is a on-and-off delay due to the junction capacitance of MOSFET, and it takes a certain time for the current and voltage to rise and fall[11]. The following definitions are defined for the switching characteristics of the MOSFET:

$$t_{on} = t_{d(on)} + t_r \quad (1)$$

t_{on} is defined as the MOSFET turn-on time, $t_{d(on)}$ represents the turn-on delay time, and t_r represents the rise time; the MOSFET turn-off time t_{off} can also be defined:

$$t_{off} = t_{d(off)} + t_f \quad (2)$$

$t_{d(off)}$ represents the turn-off delay time and t_f represents the fall time.

As can be seen from Figure VI, the turn-off time of the MOSFET is longer than the turn-on time. Therefore, when the two MOSFETs Q_1 and Q_2 in the synchronous rectification circuit are in the process of switching on and off, there will be a period of time when the two transistors are simultaneously turned on. At this time, the resistance between the power source and the ground is very small, which can be approximated as a short circuit. A large current will be generated, causing the MOSFET to heat up, reduce efficiency, and permanently damage the circuit from the physical level. At the same time, since the parasitic capacitance of the switching transistor and the external inductor form an oscillating circuit, the residual current of the inductor generates a ringing phenomenon, which increases the power consumed by the MOSFET[12]. It should be pointed out that other types of power switching devices like GTR, IGBT and other transistors have switching characteristics similar to MOSFETs because they all have junction capacitance.

C. Analysis of the Influence of Dead-time on the Efficiency of Synchronous Rectification Circuit

In order to avoid the above situation, it is necessary to leave a signal for the two transistors to be turned off at the same time when the signal states of the two MOSFETs are interchanged. The time of this signal is called the dead-time[13,14].

The general dead-time setting takes into account the switching characteristics of the MOSFET, so the following definitions can be made:

$$t_d = t_{off} - t_{on} \quad (3)$$

In the formula, t_d is defined as the dead-time. Since the turn-off time of the switch is longer than the turn-on time, a dead-time is added between the original complementary signals; the extension of the falling edge of the switching Q_1 is not matched with the switching Q_2 . The rising edges overlap. Sometimes, we also need to consider the transmission delay t_c of the control signals Q_1 , Q_2 and the above equation can be further corrected to:

$$t_d = t_{off} - t_{on} + t_c \quad (4)$$

If the dead-time setting is reasonable, it can avoid the direct conduction of the switching transistors Q_1 and Q_2 in the synchronous rectification circuit to ensure the safe operation of the circuit. In addition, when the load current is too small, a reverse current appears on the inductor L. When the inductor enters the discontinuous conduction mode (DCM), the parasitic capacitances of the MOSFET, L, C, and R_L form an oscillation circuit, and the circuit has a ringing effect. Dead-time can reduce

the residual current in the inductor, accelerate the attenuation of the oscillation, and suppress the ringing phenomenon.

However, too long dead-time setting can cause additional losses in the body diode conduction and reverse recovery of the MOSFET, reducing the efficiency of the converter. The conduction loss and reverse recovery loss of the body diode can be expressed as:

$$P_{loss,BD|t_d>0} \approx V_f \cdot I_L \cdot t_d \cdot f_{sw} \quad (5)$$

$$P_{loss,BD|t_d>0} = \frac{1}{2} \cdot Q_r(t_d) \cdot V_{HV} \cdot f_{sw} \quad (6)$$

It can be seen that the conduction loss of the body diode is related to its turn-on voltage V_f , average inductor current I_L , dead-time t_d and switching frequency f_{sw} . The body diode reverse output loss is related to the reverse recovery charge Q_r , which is a function of the dead-time t_d .

For this reason, some MOSFET driver chips have dead time between the high and low side output signals. For example, there is a fixed 540 ns dead-time between the two driving signals of IR2109, and the high side output port HO and low side output of the driving chip IR2110. The port LO is independent of each other. The dead-time of the output signal can be artificially set by setting the pulse width of the input signal of the high and low input terminals HIN and LIN.

III. EXPERIMENTAL VERIFICATION AND RESULT ANALYSIS

A. Experimental Circuit

In order to test both the relationship among the dead-time of the synchronous rectification circuit and the self-excited ringing and the dead-time and the circuit efficiency, the circuit is designed shown in Fig.5. The circuit consists of the switching transistor driver and the BUCK topology. The PWM wave of the Microcontrollers output, which drives the FET IRF3250 through the half-bridge driver IC IR2110. Q_1 , L , C_2 , C_3 , and Q_2 form a BUCK topology, and FET Q_2 is used for synchronous rectification.

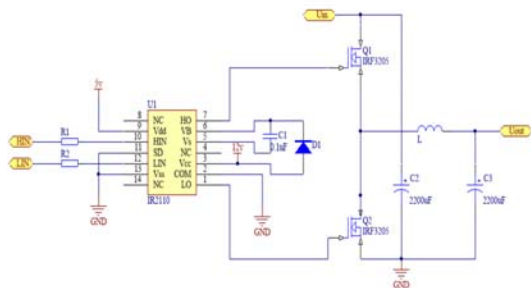


FIGURE V. EXPERIMENTAL CIRCUIT

B. Experimental Parameters

The experimental parameters are shown in Figure V (where the magnitude of the output voltage is achieved by changing the duty cycle of the signal).

TABLE I. EXPERIMENTAL CIRCUIT

Parameter	Value (in units)
Input voltage U_i	20 (V)
Signal frequency f	20 (KHz)
Dead-time D_{time}	0、78、248、336(ns)
Output voltage U_o	0--19 (V)

Fig. 6 shows the voltage waveforms of two MOSFETs corresponding to different dead-time when the output voltage is 10V. It can be seen that when the dead-time between the two transistors is zero, the peak value of the self-excited ringing of the two tubes during the switching between on and off can reach 4.02V; This is mainly due to the current overshoot caused by the switching delay of the MOSFET, the residual current of the inductor and the parasitic capacitance of the MOSFET causing oscillation. As the dead-time increases, the ringing phenomenon on the MOSFET is significantly suppressed. The relationship between dead-time and work efficiency is shown in Fig. 7. When the dead-time is set at about 250 ns, the circuit efficiency reaches the highest value. After that, the increase of dead-time no longer improves the efficiency. It shows that the reasonable setting of the dead time can effectively reduce the loss of the power switching transistor when the synchronous rectification circuit works at low voltage and further improve the working efficiency of the DC/DC circuit. At the same time, it can be seen from the curve that the dead-time can significantly improve the efficiency of the Buck circuit when the output voltage is low (below 5V). As the output voltage increases, the existence of dead-time still has a certain effect on the improvement of efficiency.

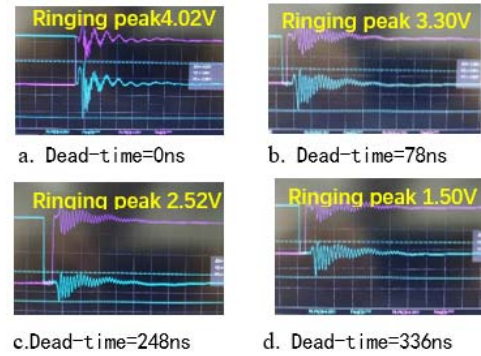


FIGURE VI. SWITCHING WAVEFORMS AT DIFFERENT DEAD TIME

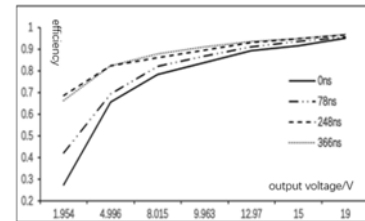


FIGURE VII. POWER EFFICIENCY AND DEAD TIME, OUTPUT VOLTAGE DIAGRAM

IV. CONCLUSION

This paper mainly studies the influence of dead-time on the circuit efficiency in synchronous rectification circuit. By analyzing the working characteristics of the synchronous

rectification Buck circuit, the existence of dead-time is explained, and the short circuit of the circuit can be avoided. It is proposed that the ringing effect in the circuit can be suppressed by using the method of setting the dead-time reasonably; When the output voltage is low, the change of the dead-time is more obvious to the improvement of the circuit efficiency. When the output voltage is increased, the improvement of the circuit efficiency by the dead-time is reduced.

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