Advances in Computer Science Research, volume 89
2019 International Conference on Wireless Communication, Network and Multimedia Engineering (WCNME 2019)

Design of Intelligent Digital Clock Based on FPGA

Zefan Ge[1], Yizhun Peng[2,*], Yuhan Zhang, Shiqian Zhang and Zhou Yang
[1]College of Electronic Information and Automation, Tianjin University of Science and Technology, China
[2]Advanced Structural Integrity International Joint Research Centre, Tianjin University of Science and Technology, Tianjin, 300222, China
[*]Corresponding author

***Abstract*—This paper takes ALTERA EP4CE6E22C8N as the control center, and designs a multifunctional digital clock system based on FPGA, which consists of clock module, timing module, power module, keyboard control module, data decoding module and digital tube display module HDL designs text input for the system logic description language. In the QUARTUSII tool software environment, based on the top-down design idea of FPGA, hierarchical modeling of digital clock circuit is completed by text file input, and the digital clock based on FPGA is constructed jointly by each basic module. After the program is compiled and simulated, download it on the core board to review. This system can realize the function of displaying time in hour, minutes and seconds in turn, calibrating with keys, timing on the hour and alarm clock.**

Keywords—ALTERAEP4CE6E22C8N; FPGA; multi-function digital clock; hardware description language

I. INTRODUCTION

We have entered the era of digital and intelligent, the noticeable character of this epoch is the widely use of various digital products[1]. Owing to the emergence of PLD devices and EDA technology, the electronic system develops rapidly towards the direction of high speed integration. Electronic system which changed the traditional design method, enabled people to implement a variety of functions based on PLD chips, this new design approach allows the designers to define the internal logic and pins of the device individually[2]. Most of the work originally done by the circuit board design is carried out in the chip design. It can not only realize various logic functions through chip design, but also reduce the workload and difficulty of schematic diagram and PCB design due to the flexibility of pin definition, increase the freedom of design, and make the design work more convenient and efficient. At the same time, this design reduces the amount and type of the chip, less volume which makes the product more integrated, It can also save the system consumption, improve the reliability of the system and the working speed, but also greatly reduce the development cycle based on the above advantages. Based on the above advantages, we can know that it is necessary to use the FPGA to study multifunctional digital clock, which can make digital clock products get better development.Our design takes Cyclone EP4CE6E22C8N chip as the control center to design a multifunctional digital clock based on FPGA. The system can display the time, minute, second and have the function of time calibration. The extension function has the alarm system as well as the Hourly chime function and so on. The object of the design is people, so the design must be humanized and practical, so as to bring people convenience[3].

II. INTRODUCTION TO DEVELOPING SOFTWARE AND PROGRAMMING LANGUAGE

Quartus software is the FPGA/CPLD of Altera company provides integrated development environment, is the basis of the single chip programmable system design, It has the advantages of friendly interface and simple and convenient use. Through the Quartus software can easily finish for programmable logic devices throughout the development process.With multiple design input modes, it can complete programming and simulation test on the same platform, fast and convenient for logic device processing. Its interface manager window is shown in figure 1 below. It is mainly composed of five parts: menu bar, tool keys, hierarchical display, workspace and information prompt window[4].

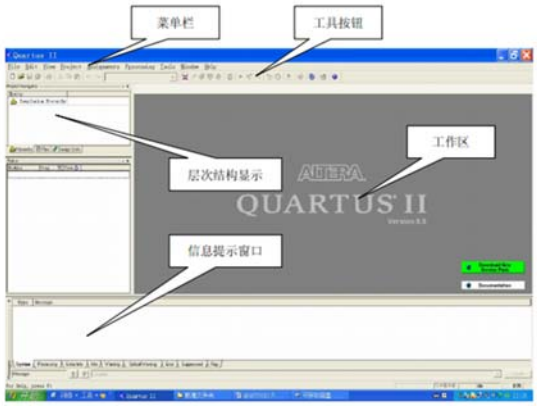

FIGURE I. QUARTUS II SOFTWARE INTERFACE DIAGRAM

The general development process for CPLD is shown in the figure:

FIGURE II. DEVELOPMENT FLOW CHART

III. OVERALL STRUCTURAL DESIGN

This system adopts the intelligent Cyclone IV series development board, and the main chip EP4CE6E22C8N is the fourth generation of the latest product of ALTERA. According

to the design requirements: 1. Design an electronic clock with time, minute and second display and time calibration function. 2. Digital clock is based on 24 hours and 60 minutes and seconds. 3. With alarm clock function and the hour function[5]. Therefore, the intelligent digital clock designed by us has the following functions: setting the time with the alarm clock by four buttons, timing on the hour and displaying. The realization of each function is made up of different modules, and the relationship between each module is shown as figure 3: the module below includes frequency division module, timing module, time telling module, time calibration module, alarm clock module and decoding display module, etc. The functions of each module are explained in detail below[6].

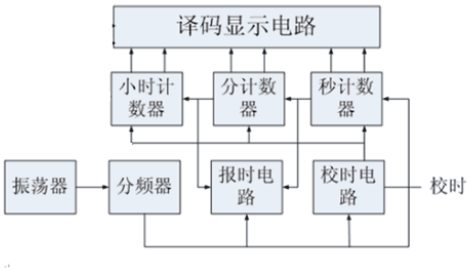

FIGURE III. BLOCK DIAGRAM OF THE WHOLE MODULE

IV. Module Design

A. Frequency Division Module

To make the counting circuit of the 24 - base counter and a 60 - base counter work, we must get a standard clock signal of 1HZ, but the development board of external crystals of 50 MHZ, therefore, we must carry out frequency division processing on the active crystal oscillator of 50MHZ through the frequency division module to get the required clock signal so as to complete the design.The function of the frequency division module is to get a standard signal of 1Hz. We let the frequency division module generate a 1s clock signal and a 0.5 second display time control signal through counting method[7]. The 1Hz standard signal generated by the frequency divider is used as the counting pulse of the counting module.

B. Timer Module

The timing circuit of the system is composed of three parts, which are hour, minute and second counting modules. When the timer receives the 1Hz standard frequency signal from the frequency division module, it begins to time and carry in turn. The hour module is a 24-base counter and the hour and second module is a 60-base counter. All of this design adopted synchronous counters.

C. Time Calibration and Alarm Clock Setting Module

The time calibration module calibrates hours and minutes by pressing s1 and s2. Pressing s1 represents modifying hours and s2 modifies minutes. The alarm clock setting module can set the alarm clock time according to the buttons s3 and s4. Press s3 to set the hour and s4 to set the minute. When the time of timing module is equal to that of alarm clock setting module, the system gives led1 an enable signal, led1 is bright. This means that the alarm has been set. At the same time, when the alarm clock is on the hour, the system will also give led1 an enable signal to make led1 bright[8].

D. LED Display Module

The development board selects four-bit total positive digital tube YLB3641BH as the external display module, and its pin diagram is shown as follows:

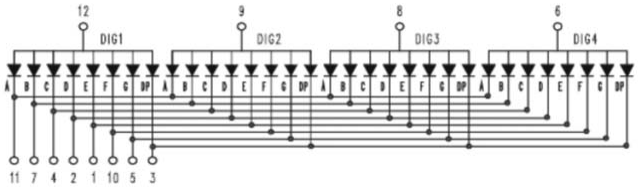

FIGURE IV. FOUR - DIGIT PIN FIGURE

We display the hours and minutes of the clock by using four total positive digital tubes, the first digital tube displays the tens place of the hour, the second digital tube displays the ones place of the hour, the third digital tube displays the tens place of the minute, and the fourth digital tube displays the ones place of the minute. In order to complete the design, we have to firstly design a division program to separate the tens place and the ones place and assign them to different variables, and then send the ones place and the tens place to the digital tube by means of dynamic scanning[9].

V. System Testing

Input the designed program, then verify and simulate it and download it to the development board. The results are shown in figure 5:

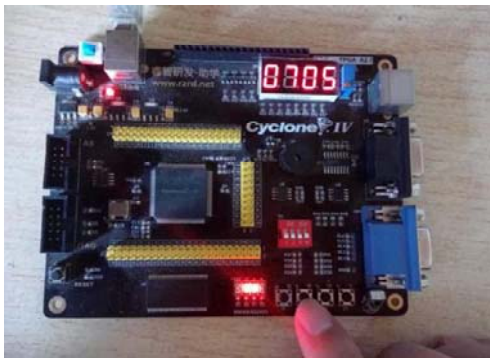

FIGURE V. PHYSICAL PICTURE OF INTELLIGENT CLOCK

As can be seen from the figure, the development board relies on the USB to power it and the display part is composed of four led digital tubes. The first and second digital tubes display for hours, 7 o 'clock in the fi alarm clock. The two buttons used for time calibration are one for each digit pressed. The alarm clock setting button needs to be pressed and held until the desired digit is added. This part is the function of the button control circuit. There are four leds beside the button. The first led is used to tell the time. When the digital clock is on the hour, led1 lights up, indicating the hour is on. The latter three leds are used to display secongure, the third and fourth digit display for minutes, and 5 o 'clock in the figure. There are four buttons in the place where the finger is pressed. The first button is used to calibrate the hour, the second button is used to

calibrate the minute, and the third and fourth buttons are used to set the hour and minute of theds. When led2 is bright, it means the second of digital clock is within 0 to 20 seconds; when led3 is bright, it means the second of digital clock is within 20 to 40 seconds; and when led4 is bright, it means the second of digital clock is within 40 to 60 seconds. Above is the function demonstration of intelligent digital clock design based on FPGA.

VI. SUMMARY

FPGA is a new type of CPLD, which has a large scale and is suitable for logic circuits such as timing and combination. Its role is significant and important because a single programmable logic device can replace dozens or even hundreds of medium-sized WI chips. CPLD has fast response time, good stability, and users can define the logical functions of the system repeatedly through the software platform without affecting the final design. The FPGA design makes the digital circuit system more flexible, and its pin function can be completely defined according to designers' own requirements. Various simulation methods make the test result more accurate and shorter test time. The development direction of programmable logic devices (PLDS) is integration and large-scale, which greatly reduces the volume of digital circuit system and the types of chips used, as well as the cost and space[10].

And the use of FPGA to design digital clock, in fact, only need to occupy a small part of the logical resources. Based on this, we can make it into SOC in the future development direction of digital clock, so that the cost becomes very low. At the same time, the whole module of clock can be combined with other products, which is another huge advantage of digital clock.

REFERENCES

[1] Qiang Zhang. Design and implementation of multifunctional digital clock based on FPGA [J]. Instrumentation user, 2008,15(6):103 -- 104.

[2] Xiaolei Liu, Guangping He.FPGA chip configuration and download [J]. Science and technology information, 2011, (15):109-110.

[3] Peng Ge. FPGA clock design [J]. Modern electronic technology, 2011,34 (11):171-176.

[4] Huang Rui. Design and Implementation of FPGA-Based Digital Frequency Meter[R]. Chongqing college of electronic engineering; Atlantis Press, 2006.

[5] Hu Xiao Ping, Lin Yun Feng. Realization on Decimal Frequency Divider Based on FPGA and Quartus II[R]. Lishui University, Lishui, China.2011,350-356.

[6] Zhimiao Xian. Design and practice of digital system for FPGA/CPLD [J]. Journal of guangxi normal university (natural science edition), 2005,23 (1) :38-41.

[7] Yong Zhang. Analysis of difficulties in making electronic clock based on DS1302 [J]. Journal of jinan vocational college, 2006,6 (3):74-75.

[8] Zhongjian Gao, Maojin Wei. Design of Verilog HDL digital clock circuit [J]. Journal of pingxiang university, 2016,33 (3) : 27-31.

[9] Sigai Yao. Quartus II software for PLD design [J]. BBS, 2009, (6) :62-63.

[10] Juyi Huang. Based on Quartus II 9.0 temporal logic circuit design [J]. Instrument technology, 2014, (6) : 43-44.