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A New Method for Reducing the Leakage Current in the Readout Circuit of Ultraviolet Focal Plane Detector

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Abstract. A readout circuit with low leakage current is presented which performs leakage current suppression and integration linearity enhancement. An additional transmission gate is added to suppress the leakage current by forcing each end of MOSFETs in the transmission gate to be equal so that the discharge circuit of integration capacitor can be completely cut off when the integration circuit is at the stage of integration. It is simulated and implemented in a standard 0.18-μm CMOS process. The results show the leakage current is reduced to 1.5 nA which is 4 times lower compared with conventional circuit. The linearity of integration is 99.9% in proposed integration circuit.

Introduction

The capacitive trans-impedance amplifier (CTIA) is widely used in readout circuits of detectors because of its good performance[1]. However, in the conventional reset stage of CTIA, there have leakage currents when the transmission gate (TG) is turned off. These leakage currents cause the non-linear phenomenon of integration voltage, especially when the photo-generated current of detectors is at pA level or less. In order to reduce leakage currents when the switch is turned off, Zou [2] added 12 MOSFETs to form Dynamic Switch Leakage Compensation structure. Jin Jyh Su[3] and Ishida[4] added 10 and 8 MOSFETs to suppress leakage currents respectively. Although these methods can effectively reduce leakage currents, they are accomplished at the expense of area. For pixel-level cell circuits, these methods are obviously not available. We propose a new structure with only four MOSFETs to suppress leakage currents in readout circuit. This structure can suppress leakage currents to improve the linearity of integration voltage with at least 50% less circuit area.

Structure of Readout Circuit

The proposed readout circuit with low leakage current is shown in Fig. 1. The circuit consists of three parts: Part I: the equivalent model of UFPA, Part II: capacitive trans-impedance amplifier (CTIA) for the integration circuit and part III: Correlated Double Sampling (CDS) structure for the sampling circuit.

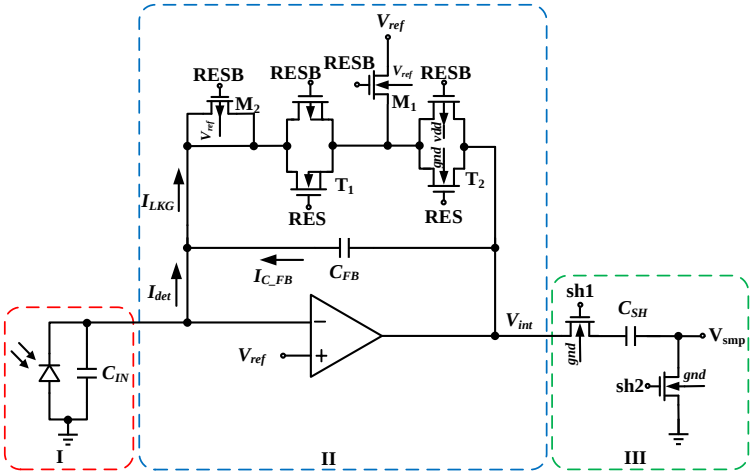


Figure 1. Proposed readout circuit structure

In Part I, UFPA is considered as a photodiode in parallel with a capacitor C_{IN} to generate detect current I_{det}. The charge pulse caused by I_{det} is integrated on integration capacitor C_{FB} of CTIA in Part II and provides the integration voltage V_{int} at output. Next V_{int} is sampled and output in Part III.

In Part II, the capacitor C_{FB} is in the feedback path and used to integrate input signal from Part I. PMOS transistor M_2, transmission gage T_1, NMOS M_1 and transmission gage T_2 form the reset switch of the integration circuit to discharge C_{FB} before the next integration time comes.

In conventional circuit, T_2 is the only reset switch to discharge C_{FB}. Turning on T_2 resets CTIA and set the output of CTIA to V_{ref}. Then, turning off T_2 makes C_{FB} be charged by I_{det} during one integration time. Considering the non-ideal characteristics of the switch, a low current is extracted from C_{FB} and C_{IN} and flows through T_2 at the integration stage of the integration circuit. The leakage current I_{LKG} in the CTIA is the sum of I_{C_FB} and I_{det}:

$$I_{LKG} = I_{C\_FB} + I_{det}\,. \tag{1}$$

The ratio of I_{C_FB} and I_{det} is given by:

$$\left|\frac{I_{C\_FB}}{I_{det}}\right| = A\left(\frac{C_{FB}}{C_{IN}}\right), \tag{2}$$

Where A represents the open-loop gain of the operational amplifier (OPA) in CTIA. Generally, A is large, so I_{C_FB} is much larger than I_{det}, which means I_{LKG} is dominated by I_{C_FB}. We can have:

$$I_{LKG} \cong I_{C\_FB} = \frac{\Delta V_{int} C_{FB}}{\Delta T}, \tag{3}$$

Where ΔT is integration time and ΔV_{int} is the voltage swing after an integration time. As shown in Eq. 3, I_{LKG} is proportional to C_{FB} and ΔV_{int} when CTIA is at the integration stage. As long as the leakage current passes through T_2, it affects the integration output V_{int} and makes integration worse.

It should be noted that when the reset switch is turned off, the main reason for the current flowing through the reset switch is the potential difference in the internal P-N junction of MOSFETs[5, 6].

To remove this difference, we designed the reset switch part of CTIA as shown in Fig. 1. This reset switch consists of not only the transmission gate T_2, but also another transmission gate T_1, NMOS transistor M_1 and PMOS transistor M_2. The timing waveforms of T_1 and T_2 are shown in Fig. 2.

When RES goes to high level and RESB goes to low level, the integration circuit is at the reset stage. T_1, T_2 and M_2 are turned on and M_1 is turned off. C_{FB} discharges through T_1 and T_2. M_2 is turned on to absorb the charge in the circuit to establish its own channel, consequently the potential of C_{FB} can be reset to a lower voltage value than V_{ref}.

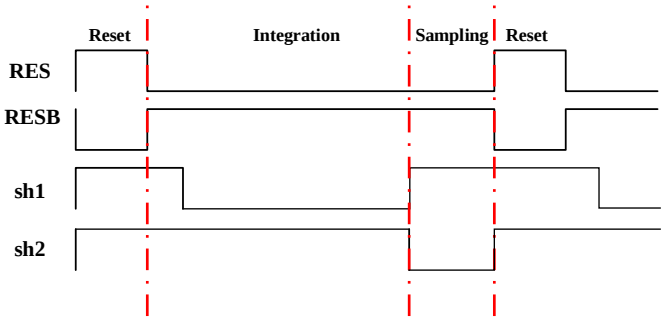


Figure 2. Timing waveforms of reset switch T_1, T_2 and sampling switch sh_1, sh_2

When RES turns from high level to low level and RESB turns from low level to high level, the integration circuit enters the integration stage. T_1, T_2 and M_2 are turned off, M_1 is turned on, and C_{FB} is charged. The voltage of the right end of T_1 is clamped to approximate V_{ref} because of the turning on of M_1 and the left end of T_1 will be stabilized to V_{ref} as well because of the function of the OPA. At this time, the voltage of input, output and the body in T_1 are all set to V_{ref}, so the P-N junction potential difference in T_1 is 0. The leakage current in T_1 and T_2 is suppressed.

CDS structure in Part III is used for sampling circuit. CDS realizes its capabilities through two

periods: (i) Before the reset completes, sh_1 and sh_2 go to high level, the circuit takes the first sampling. After a period of time, sh_1 turns from high level to low level. The noise voltage and initial voltage of the integration circuit are sampled on C_{SH}. At this time, the upper plate potential of C_{SH} is the sum of noise voltage and initial voltage, while the lower plate potential is 0. (ii) After the integration completes, sh_1 goes to high level and sh_2 turns from high level to low level, the second sampling is carried out. Because the charge on the capacitor cannot mutate, the potential of the lower plate of C_{SH} becomes the integration output voltage V_{int}, so the structure can effectively remove the noise effect.

Simulation Results

The proposed readout circuit is implemented and simulated in a 0.18-μm standard CMOS process.

The comparison of I_{LKG} in integration circuit with or without M_1, T_1 and M_2 is shown in Fig. 3. *Line a* shows the I_{LKG} is about 6 nA in the traditional integration circuit of which the reset switch just consists of T_2 for the input current I_{det} of 300 fA. *Line b* shows the I_{LKG} is about 1.5 nA in our integration circuit of which the reset switch consists of M_1, T_1, M_2 and T_2. The leakage current of proposed structure is about 4 times lower than traditional one. The proposed readout circuit can effectively suppress leakage current.

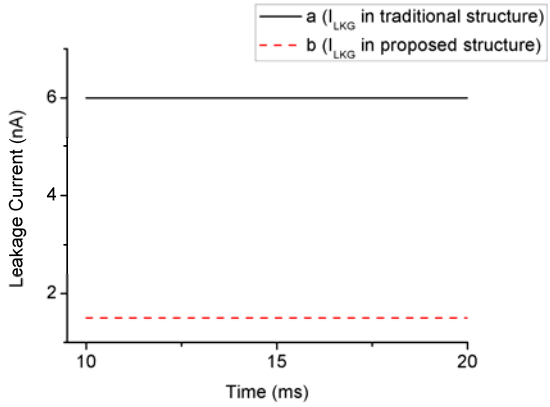
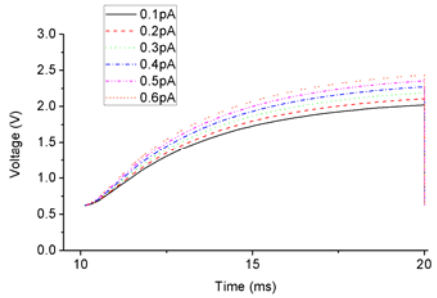


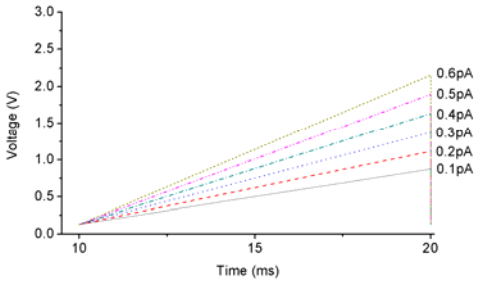
Figure 3. Leakage Current Waveforms in integration circuit

a. I_{LKG} in traditional integration circuit without T_1, M_1 and M_2
b. I_{LKG} in proposed integration circuit with T_1, M_1 and M_2

V_{int} is measured when I_{det} is set from 0.1 pA to 0.6 pA and V_{ref} is set to 600 mV. The waveforms of V_{int} in the structure without M_1, T_1 and M_2 show an initial voltage of 600 mV and a low accuracy of linearity (Fig. 4 (a)). The waveforms of V_{int} in the structure with M_1, T_1 and M_2 have been presented in Fig. 4 (b). The initial voltage of V_{int} is reduced to 130 mV, thus the output with larger integration range can be obtained.



(a)



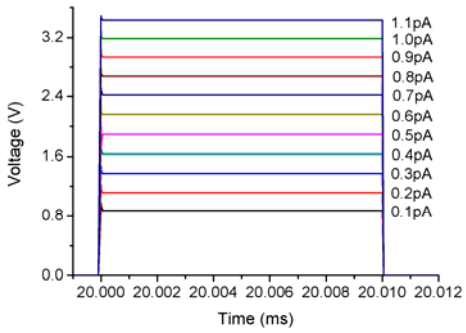
(b)

Figure 4. Integration voltage waveforms

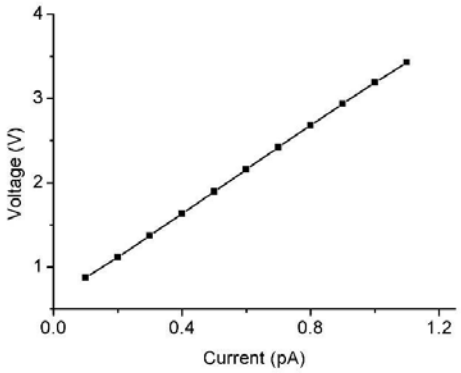
(a). V_{int} in conventional integration circuit
(b). V_{int} in proposed integration circuit

The waveforms of V_{smp} are shown in Fig. 5 (a) when I_{det} various from 0.1 pA to 1.1 pA with 0.1 pA step. The linearity of 99.9% can be obtained by calculating from Fig. 5 (b).

Finally, it can be concluded that the measurement results show good agreement with the analysis.



(a)



(b)

Figure 5. CDS results. (a) the voltage after sampling; (b) the sampling voltage linearity analysis

Conclusion

We have proposed a readout circuit with low leakage current which performs leakage current suppression and integration linearity enhancement. On the basis of transmission gage T_2, additional NMOS transistor M_1, transmission gate T_1 and PMOS transistor M_2 are added to force the voltage of each end of MOSFETs in T_1 to be equal, thus leakage current can be suppressed. The advantage of this design is its low leakage current, high integration linearity and wide output range with less circuit area. Using a standard 0.18-μm CMOS process, the leakage current in proposed integration circuit can be reduced to 1.5 nA which is 4 times lower than in traditional one, and the integration linearity is measured as 99.9%. Compared with conventional readout circuit, the proposed integration structure yields efficient leakage current reduction with less additional components.

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