

Design and Implementation of a High Precision Frequency Meter based on Multimode

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Abstract. Frequency meter logical resource occupancy is the research object of electronic information field. To solve the precision of the frequency meter and reduce the occupation of logical resources, this paper designs a measurement system based on FPGA, which can switch between high frequency and intermediate frequency modes freely. Firstly, the signal generated by the dual-channel DDS function signal generator is input into the conditioning circuit for corresponding processing, and then the high-frequency mode or mid-frequency mode is selected by the DIP switch and input to the FPGA chip for counting. Finally, the measurement results are displayed on the LCD. The digital frequency meter can execute the corresponding functional test according to the mode selected in advance after testing, and it is found that compared with the modeless high-precision frequency meter, the high frequency has less 103 logical resource occupations in the high-frequency mode, and the mid-frequency has less 242 logic resources in themed-frequency mode.

Keywords: Frequency meter; Mode; High precision.

1. Introduction

With the development of the times, the electronics industry technology has also entered an era of rapid development [1]. Digital frequency meters play an increasingly important role in modern industrial production activities and scientific research fields (such as aerospace, electronics, control, etc.). Frequency is crucial parameter that reflects the stability of the system in some control systems and communication systems. We can predict the state of the system at the next moment by grasping the frequency of some systems at the moment [2], and then take corresponding control measures to enhance system reliability. However, In the process of frequency measurement, the choice of the frequency meter is closed to the measurement results. Among them, the high-precision frequency meter is widely used in various fields due to its many merits. Such as small size, fast response speed and high precision.

In recent years, with the widespread application of high-precision frequency meters, frequency measurement methods are also constantly evolving, and their accuracy is also increasing. Among them, frequency measurement method can generate measurement errors when the frequency is low. Cycle measurement method can generate measurement errors when the frequency is high [3]. Obviously, none of the above methods are well applied to the wider frequency measurements. Thus, the counter synchronous parallel counting method came into being. However, in the pursuit of high precision, the use of logical resources has not been greatly improved.

This article uses the FPGA development board and the NiosII processor, adopt three-count synchronous parallel counting method, and add mode selection function to design a broadband high-precision frequency meter based on Multimode. Compared with the modeless high-precision frequency meter, the frequency meter of this design can reduce the logic resources required by the system and reduce the system power consumption while improving the measurement accuracy.

2. Principle of System Frequency Measurement Method

In the frequency measurement method, the gate signal and the signal to be tested have randomness at the rising edge time when the gate signal is different from the signal to be tested, which could cause a random quantization error in the counting result. In the cycle measurement method, the measured signal and the standard signal are random when the signal to be tested is different from the standard

signal, which makes the counting result random. Therefore, from the above analysis, both the frequency measurement method and the cycle measurement method are not suitable for the measurement of a wide range of frequency.

The counter synchronous parallel counting method summarizes the shortcomings of the frequency measurement method and the cycle measurement method [4]. On the basis of them, the counting of the standard high pulse signal and the control of the counter are added[5]. The principle of the three-counter synchronous parallel counting method is as shown in FIGURE 1.

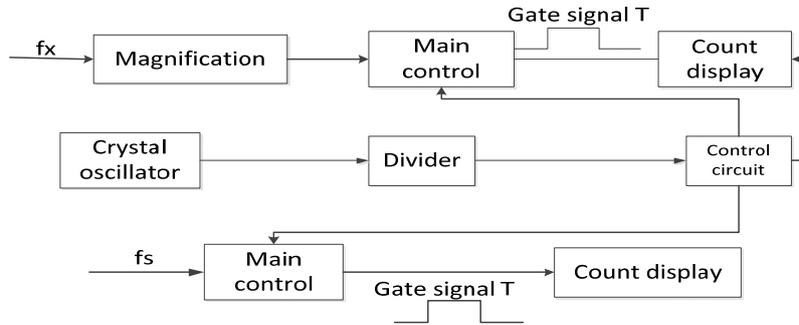


Figure 1. Block diagram of the principle of three counter synchronous parallel counting.

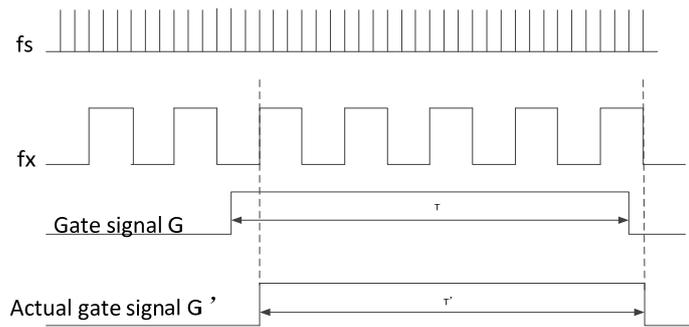


Figure 2. Counter synchronous parallel counting waveform.

From the picture, it can be known that the rising edge of the measured signal does not arrive and the counter does not count, when the rising edge of the gate signal comes. The rising edge of the measured signal comes and starts the counter, when the rising edge of the gate signal comes. When the gate signal ends at the gate time, if the falling edge of the gate time signal comes, the rising edge of the signal under test does not arrive, the counter continues to count, and when the rising edge of the measured signal comes, the counter stops counting and reads at this time. This solves the problem that the gate signal is out of sync with the signal under test. So, a formula can be built as follows:

$$\frac{1}{f_s} \times N_s = \frac{1}{f_x} \times N_x \tag{1}$$

Simplify the above formula to obtain the measured signal f_x :

$$f_x = \frac{f_s \times N_x}{N_s} \tag{2}$$

It can be seen from the above analysis that the counter synchronous parallel counting method measures the counting error regardless of the frequency of the measured signal, but is related to the

frequency and gate time of the standard signal. Therefore, this system selects the counter synchronous parallel counting method as a method of measuring frequency.

3. System Design

3.1 Overall System Design

The signal generated by the dual channel DDS function signal generator is processed by the signal conditioning circuit and sent to the FPGA system. Firstly, the mode is selected by the DIP switch, and then frequency measurement, period measurement, positive duty cycle measurement are sequentially performed and counted separately. Lastly, the measured signal is input to the NiosII processor for data processing and calculation, and the result is displayed on LCD. The mode includes the high-frequency mode and the mid-frequency mode. The counting control module control is mainly responsible for controlling the three counters. The overall design of the system is shown in FIGURE.3.

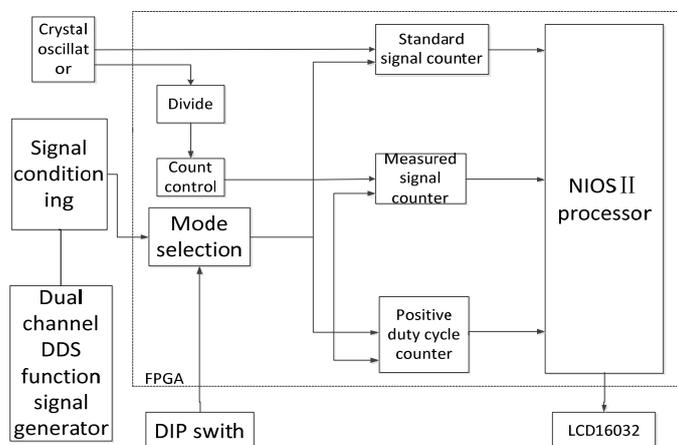


Figure 3. System design block diagram.

Verilog HDL hardware description language can accurately describe the behavior of the design, verify the design structure, design the waveform, allow different abstract levels of description in the same circuit model, and most popular synthesis tools support Verilog HDL hardware description language [6]. Thus, all parts of the design use the Verilog HDL hardware description language.

3.2 Hardware Design

The signal generated by the two-channel DDS function signal generator also requires a series of processing to obtain a valid analog frequency signal [7]. The DDS function signal generator used in this design is TFG6020, which can generate square wave, sine wave and pulse signal. Due to the sine wave generation, the signal conditioning circuit also needs a shaping circuit to convert the waveform generated by the DDS function signal generator into a rectangular wave. For waveform conversion, this design uses a high-speed comparator to shape the sine wave. In addition, the signal conditioning circuit also needs to include an automatic gain control circuit (AGC) to attenuate the large signal, and the small signal is amplified to retain the information of the original input signal to the greatest extent [8]. The high-speed comparator uses the TLV3501 chip, which is a rail-to-rail high-speed comparator with 4.5ns rail-to-rail time and extremely high comparison speeds [9].

The FPGA adopts CycloneIV-EP4CE6E22CBN. The chip is stable, the working crystal frequency reaches 50MHz, the frequency multiplier can be stabilized to 100MHz, and the data can be processed in parallel [9]. The Nios II processor is customized using the Qsys tool under Quartus II software. The Nios II processor is customized using the Qsys tool under Quartus II software. The components used in this design mainly include Nios II processor, clock source, parallel input and output port, EPCS controller, RAM, LCD16032 liquid crystal display and JTAG serial port. These components can be compiled and instantiated according to the required parameters.

3.3 System Measurement Function

3.3.1 Frequency Measurement

The frequency measurement is based on the counter synchronous parallel counting method. The Verilog HDL hardware description language is used to design and implement the circuit structure in the measurement. FIGURE.4 shows the simulation waveform of the frequency measurement.

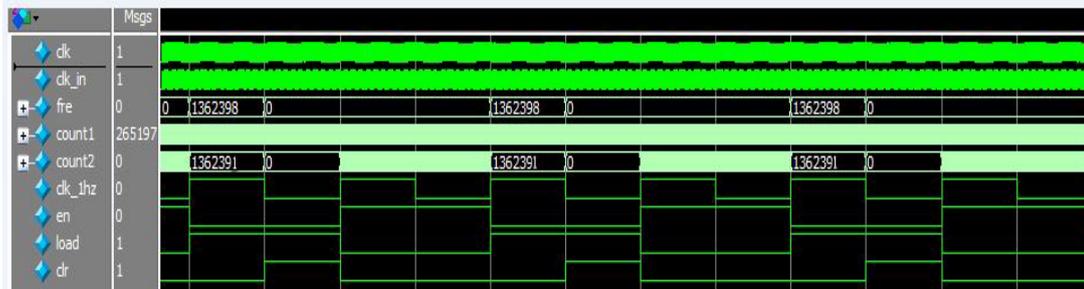


Figure 4. Frequency measurement simulation waveform

The enable signal *en* is obtained by dividing the clock of 1hz by 2, and the load is the inversion of *en*. When *en* is high, *count2* counts into the rising edge of *clk_in*. When the rising edge of load comes, the counter *count2* assigns the frequency value to the output *fre*. When the rising edge of *clr* arrives, both *fre* and *count2* are cleared, start the next measurement. In the testbench file, the measured signal *clk_in* period is 734ns, which is different from the measured value *fre* by 8.

3.3.2 Positive Duty Cycle Measurement

In this paper, the signal obtained by comparing the signal to be tested with the actual gate signal is recorded as the D signal, and the D signal is used as the control signal of the positive duty cycle counter. The result of counting the standard signal during the high level of the D signal is N_d , and the count value of the standard signal is N_s during the entire gate time T' . So, the positive duty ratio can be calculated. The simulation waveform diagram of positive duty cycle measurement in this design is shown in FIGURE 5.

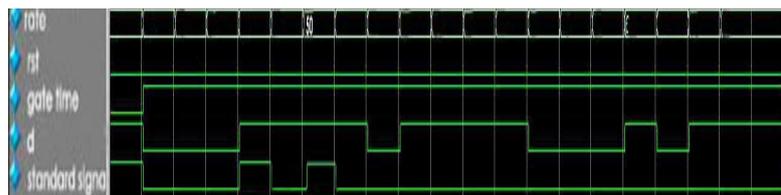


Figure 5. Positive duty cycle measurement simulation waveform

In the above figure, the standard signal count is 4 during the entire gate time, the standard signal count is 2 during the high level of the d signal, and the positive duty ratio is calculated as 50%.

4. Analysis of Results

4.1 Measurement Method Accuracy Analysis

In the actual measurement, the signal source is used to output the signal to be tested and input into the measurement system for various functional tests. The error formula is as follows:

$$RE = \frac{|SV - MV|}{SV} \times 100\% \quad (3)$$

In the above formula, *RE* represents the relative error, *SV* represents the standard value, *RE* represents the signal frequency and *MV* represents the measurements.

When the gate time is 1s, the measurement results and errors of the frequency measurement method and the three-counter synchronous parallel counting method are shown in TABLE 1 and TABLE 2, respectively.

Table 1. Measurement results of the frequency measurement method

standard value /Hz	measurements /Hz	error/%
1000000	999998	0.0002
10000000	9999983	0.0002
100000000	99998542	0.0015

Table 2. Three counter synchronous parallel counting method measurement result

standard value /Hz	measurements /Hz	error/%
1000000	999998	0.0002
10000000	9999983	0.0002
100000000	99998542	0.0014

It can be seen from TABLE 1 and TABLE 2 that in the same gate time, the errors of the mid-band and the high-frequency band using the three-counter synchronous parallel counting method are less than 0.002%.

When the standard signal frequency is 10MHz, the measurement results and errors of the measurement cycle method are shown in TABLE 3:

Table 3. Measurement results of measurement cycle method

standard value /Hz	measurements /Hz	error/%
1000000	1000000	0.0000
3000000	2999999.333	0.0009
300000000	0	100%

In the same way, it can be seen from table 3 that the frequency band error of cycle measured method is large, and the maximum error can reach 100%. Therefore, it can be seen from TABLE 1, TABLE 2 and TABLE 3 that the three-counter synchronous parallel counting method is more suitable for high-precision measurement.

4.2 Analysis of Logical Resource Occupancy under Different Modes

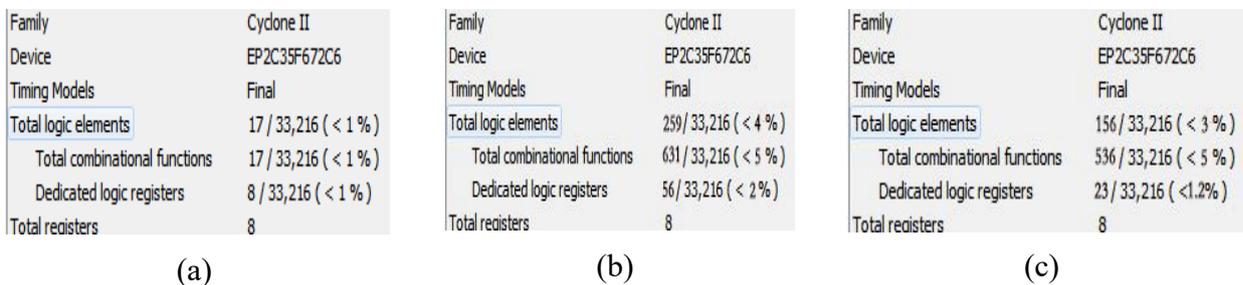


Figure 6. Analysis of logical resource occupancy under different modes

(a), (b), and (c) are the logical resource occupancy graph in the mid-frequency mode, the logical resource occupancy graph in the modeless mode, and the logical resource occupancy graph in the high-frequency mode under the Quartus13.0 software simulation, The total logical resource occupation in (a) is 17, the total logical resource occupancy in (b) is 259, and the total logical resource occupancy in (c) is 156. It can be seen from the above that the logical resource occupation in the high-frequency mode is less than that in the modeless mode, and the logical resource occupation in the mid-frequency mode is less than that in the modeless mode.

5. Conclusion

The frequency meter uses FPGA as the development board, meanwhile, analyzes and compares the traditional frequency measurement method and multi-counter synchronous parallel counting method. Finally, the three-counter synchronous parallel counting method is used to realize the frequency measurement. The high-speed comparator and gain amplifier are used to ensure the maximum guarantee for the Original information of signal, taking full advantages of the FPGA high operating frequency, short design cycle, high flexibility and high reliability to design and implement a complete system design. Compared with the modeless high-precision frequency meter, the high-precision frequency meter based on multimode, improves the practicability and reliability of the system design, and reduces the occupation of logic resources. Experimental results show that the frequency meter designed by this system has high precision, and the method of selecting high-frequency mode at high frequency has low system logic resource occupation, and the method of selecting mid-frequency mode at medium frequency has low system logic resource occupation, which meets the experimental design requirements.

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