

Design of direct digital synthesizers signal generator

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Abstract— An integral element of most radio devices is systems of frequency and signal synthesis. Most of the known circuits use analog elements, which are characterized by the change of parameters under the influence of external factors. However, with the development of digital technology that uses only mathematical calculations and logical functions resistant to changes in external factors, a new method of generating signals was developed, which is called a direct digital synthesis. One of the main types of frequency synthesizers are direct digital synthesizers (DDS). High frequency and phase resolution, the fastest possible transition to another frequency without phase discontinuity, the ability to control the frequency, phase and amplitude through the digital interface are constantly expanding the DDS implementation area in various fields of technology, such as satellite communication, radar-location, radio navigation, measuring equipment, etc. A direct digital synthesis is a method of generating a signal of the desired frequency and waveform using digital resources. Owing to the digital solution, the generated signal has the accuracy inherent in digital systems. The frequency, amplitude and phase of the signal at any given time are known and controlled. With these advantages, direct digital synthesis is increasingly replacing analog solutions. The relevance of the study stems from the lack of domestic equivalents of frequency synthesizer chips, the implementation on the modern element base. The article describes a method for designing a direct digital synthesizer (DDS) with a quarter-wave transformer (QWT) based on FPGA.

Keywords— *designing a direct digital synthesizer, quarter-wave transformer, pseudorandom number generator*

I. INTRODUCTION

The aim of the work is to develop a methodology for designing the base part of a frequency synthesizer based on a direct digital synthesizer (DDS) using FPGA.

The synthesizer diagram is shown in Fig. 1. A quarter-wave transformer uses the symmetry property of the sine to generate a complete signal period. This means that the memory contains samples for only a quarter of the signal wave, which, when applying a certain memory reading algorithm, form a complete period. This technique allows to reduce the amount of memory used by four times.

A complete period requires four table read cycles:

- in the forward direction (from a zero address to the maximum) with a positive sign signal,
- in the backward direction (from the maximum address to zero) with a positive sign signal,
- in the forward direction (from a zero address to the maximum) with a negative sign signal,
- in the backward direction (from the maximum address to zero) with a negative sign signal [1].

In this method of generation, the entire signal swing will range from zero to the supply voltage (U_{sup}) of the device. Therefore, conditionally, the zero, relative to which the positive or negative half waves are measured, will be half the supply voltage ($U_{sup}/2$). And in order to form a half wave there are two ROM read cycles (in the forward and backward direction), and the sign signal determines what it will be, positive or negative, by adding or subtracting the sample value with the defined zero value. Thus, the amplitude of the negative half wave will be between zero and voltage $U_{sup}/2$, and the amplitude of the positive half wave – between $U_{sup}/2$ and U_{sup} .

In this option, the structure of the DDS contains the following blocks:

- phase accumulator (PA),
- quadrant selector (QS),

- read-only memory with sample values (ROM),
- output inverter (OI).

II. MATERIALS AND METHODS

The direct digital synthesizer is based on the Altera Cyclone IV FPGA family, model EP4CE6. The chip is mounted on a debug board, which in its composition has a generator of clock frequency of 50 MHz which we will focus on. The development of the synthesizer program code was conducted using the Verilog language in the Quartus Prime 17.0 Lite Edition environment (Fig. 2).

The main task is to obtain a sine signal in digital form for further application in digital signal processing.

A phase accumulator controls the entire system. It is responsible for setting the frequency using the tuning word, phase control and tuning step. The phase value is changed linearly and is received at the output in digital form [2].

The quarter selector determines in which quadrant a quarter of the wave will be located, depending on the phase value. The output has address values for reading the ROM table and sign signal.

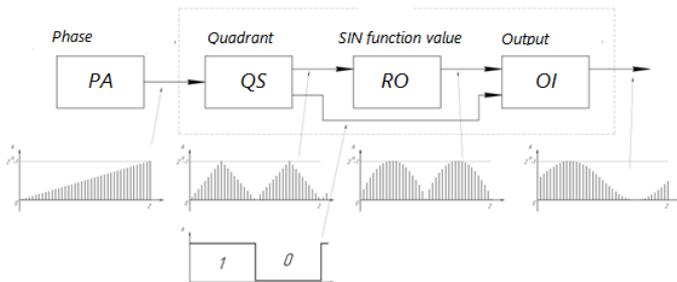


Fig. 1. Block diagram of the frequency synthesizer with a quarter-wave transformer

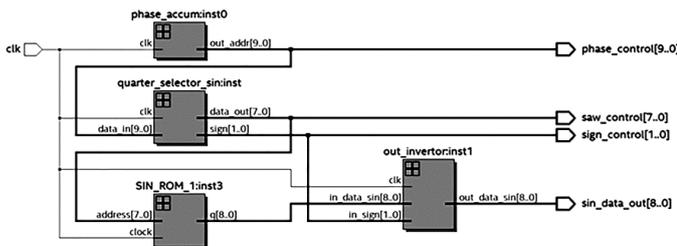


Fig. 2. Diagram of the direct digital synthesizer with a quarter-wave transformer in the Quartus Prime environment

The read-only memory contains sample values for a quarter of the sine signal.

The output inverter is used for the final generation of the sine signal. The input takes the sample values from the ROM and the sign signal from the quarter selector.

At the output of the system, a sequence of discrete sine values is created, which, after processing by a digital-to-analog converter (DAC) and filtering by a low-frequency filter (LFF), takes the form of an analog sine signal [3].

In this configuration, the design procedure is reduced to the determination of such DDS parameters as:

- maximum synthesized frequency,

- clock frequency,
- phase accumulator word length,
- number of ROM cells,
- word length of ROM cells.

The first question to be answered when designing a DDS is the determination of the maximum synthesized frequency. If the aim is to determine it at a known clock frequency, the following formula is used:

$$F_{max} = 0,4 \cdot f_{clk} \tag{1}$$

where f_{max} – maximum synthesized frequency;
 f_{clk} – clock frequency.

If we need to determine the clock frequency at a known maximum synthesized frequency, the following formula is used:

$$f_{clk} \geq f_{max} / 0,4 \tag{2}$$

where f_{clk} – clock frequency;
 f_{max} – the maximum synthesized frequency.

The coefficient 0.4 indicates that the output frequency of the DDS higher than $0.4 \cdot f_{clk}$ cannot be obtained because the reconstruction of the output signal is impossible without a low-pass filter that limits the range of the output signal to approximately 40% of the clock frequency.

After defining the clock frequency, the next step is to calculate the phase accumulator word length. It will affect the frequency tuning step.

The phase accumulator contains:

- a phase increment register containing the tuning word M (frequency code) that sets the entire system to the desired frequency,
- adder that adds the current phase value to a constant number M,
- phase register that contains the current phase value and reboots with a new value when a clock signal is received.

All elements of the diagram have the same word length. The PA is assembled according to the diagram shown in Fig. 3.

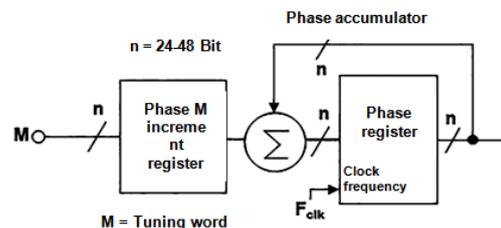


Fig. 3. PA construction diagram

Now, using a known clock frequency, the PA word length can be selected, which provides the tuning step value close to the desired value, using the formula:

$$\Delta f = f_{clk} / 2^n, \tag{3}$$

where Δf – tuning step;
 f_{clk} – clock frequency;
 2^n – phase accumulator word length.

The calculation result is the calculated values of the tuning step for the word length from 24 to 48 at a given frequency.

The frequency of the synthesized signal can be determined by the formula:

$$f_{out} = M \cdot f_{clk} / 2^n \quad (4)$$

where f_{out} – synthesized frequency;

M – tuning word;

f_{clk} – clock frequency;

2^n – phase accumulator word length.

The tuning word M for setting the DDS to the desired frequency is calculated by the following formula:

$$M = 2^n \cdot f_{out} / f_{clk} \quad (5)$$

where M – frequency code;

n – PA word length;

f_{out} – output frequency;

f_{clk} – clock frequency.

If the synthesizer should operate at a fixed frequency, a constant calculated by the formula (5) corresponding to the required frequency is recorded in the phase increment register. The output signal of the PA module should look like a sequence of discrete phase values, where each subsequent value differs from the previous one by the value M . The graph is shown in Fig. 4.

As mentioned above, the basis of the system is the phase accumulator (PA), which manages the entire system. The PA diagram in the Quartus Prime environment is shown in Fig. 5.

In practice, another register is set before the adder (phase increment register - PIR), which has the value of the increment phase denoted by the letter M .

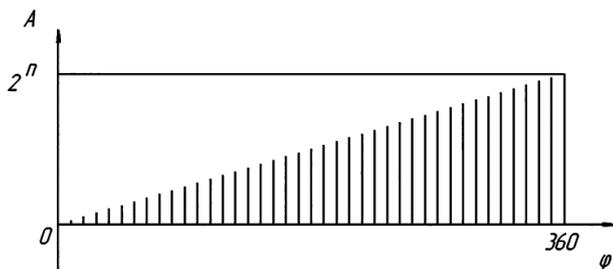


Fig. 4. PA phase output

The main characteristic of the phase accumulator is the frequency tuning step. This setting depends on the clock frequency and word length of the phase accumulator. The word length of the accumulator is selected from the range of 24 - 48 bits, that provides an optimal frequency tuning step [4].

For example, at a clock frequency of 50 MHz, the step can vary from 2.9 Hz to 1.77×10^{-7} Hz respectively.

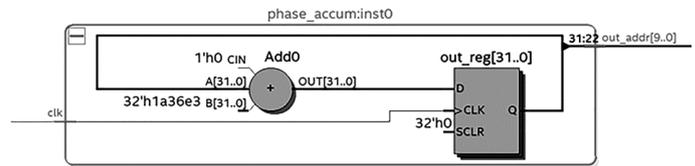


Fig. 5. Diagram of the phase accumulator in the Quartus Prime environment

With the available 50-MHz clock generator, it is possible to provide a frequency tuning step from 2.9 Hz to 1.77×10^{-7} Hz. Table 1 presents the comparative data of the calculated tuning step sizes for different word lengths of the phase accumulator from 24 to 48 bits.

For the designed synthesizer, a 32-bit length was selected, which provides a tuning step of 0.01 Hz.

A tuning word, denoted by the letter M , which sets the tuning step corresponding to a specific frequency, is written to the phase increment register. The contents of the phase increment register can take values in the range:

The word length of the register should be in accordance with the selected word length of the phase accumulator, as well as the word length of the adder.

$$0 \leq M \leq 2^n$$

where n – word length of the phase increment register;

M – number in the phase increment register.

Zero increment corresponds to zero frequency, i.e. constant current at the output, while increment 2^n corresponds to the maximum frequency respectively.

However, as mentioned above, the maximum synthesized frequency satisfying the condition is 20 MHz. Thus, in our case, the value of M will vary within:

$$0 \leq M \leq M(f_{max}),$$

In hexadecimal form it is shown as:

$$0 \leq M \leq 0,66666666_{16}$$

At the output, the phase accumulator has a sequence of binary numbers differing by the M value.

The module has one input to which the clock signal is supplied, and one output that transmits a sequence of values of the instantaneous phase.

The module has no management interface. Instead, the fixed code $M = 32'h418937$ corresponding to the frequency of 50 KHz is written to the phase increment register. In the module, when the positive edge of the clock signal is received, the phase increment value in the adder is added to the current value of the output register. The summation is performed before the counter overflows, after that it resets and starts counting from zero.

The next step is to create a quadrant selector block. This block starts the conversion of phase values into a sine signal.

The phase values from the PA output truncated to the P word length by removing less significant bits are received at its input. Typically, the value of P is in the range of 8 to 16 bits, which is determined by the number of ROM cells used or depending on available resources. The truncation of less significant bits introduces an acceptable minor error, since the bulk of errors and noise occurs at the stage of digital-to-analog conversion with the help of the DAC.

The quadrant selector is designed to form the address sequence to read the contents of the read-only memory (ROM) and to generate the sign signal, which will be used in the final signal generation. It operates as follows. The two most significant bits are selected from the values received at the input of the QS and are considered as signals of the ROM table reading direction and the sign signal [5].

TABLE 1. Dependence of the frequency tuning step on the word length of the phase accumulator at a 50-MHz clock frequency

Phase accumulator (PA) word length	Frequency tuning step
24	2,98023
25	1,49011
26	0,74505
27	0,37252
28	0,18626
29	0,09313
30	0,04656
31	0,02328
32	0,01164
33	0,00582
34	0,00291
35	0,00145
36	0,00072
37	0,00036
38	0,00018
39	0,000090949
40	0,000045474
41	0,000022737
42	0,000011368
43	0,0000056843
44	0,0000028421
45	0,0000014210
46	0,00000071054
47	0,00000035527
48	0,00000017763

The most significant bit P in a complete period changes its state with the frequency corresponding to the sign change of a half wave, and the bit P-1 (penultimate) with the same frequency changes the state as sites of increase and decline of

half waves of the sine signal. Together, the two signals determine which quadrant the sine counts will be located in. A table of signal states for each quadrant is presented below.

TABLE 2. Quadrant code selection signal states

Quadrant number	Bit P	Bit P - 1
1 (I)	0	0
2 (II)	0	1
3 (III)	1	0
4 (IV)	1	1

In fact, the state of the most significant bit P can be directly sent to the output of the QS block as a sign signal, and inside the block the state of the P-1 bit can be processed. When the P-1 bit has a logical zero state, the address value should be increased from zero to maximum, and with the logical unit, reduced from maximum to zero. As a result, the increase and decrease of the address values will correspond to the forward and backward reading of the table. The timing diagram is shown in Fig. 6.

Then, the value of the address is sent to the ROM address input. The ROM can be not only built into the crystal (integrated into the FPGA), but also external, depending on the needs and resources of the developer. With the increase of the cell word length grows the accuracy of the discrete sine value. However, the final accuracy depends on the DAC parameters. Typically, a cell word length is chosen for two bits greater than the DAC word length. Therefore, the ROM cell word length is between 8 and 14 bits.

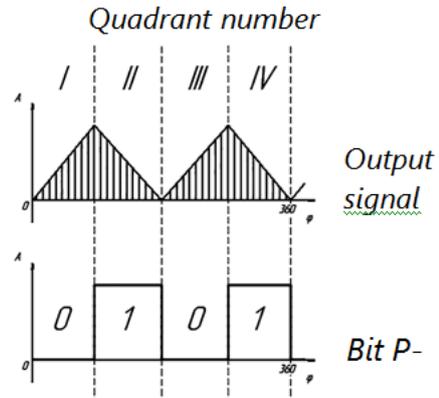


Fig. 6. Timing relationship of the signal reading direction and output values of the ROM read address

With the usual options, when the ROM table contains the values of the full sine period, the values from the PA output are sent directly to the address input of the memory block. In our case, using a quarter-wave transformer, if we repeat this operation, we get only repeated quarters of the sine period at the output.

To form a complete period, the table should be read a little differently. To form a wave between 0 and $\pi/2$ (I quadrant), the values of the table are read in the forward direction, from a zero address to the maximum. To form a wave between $\pi/2$ and π (II quadrant), the values are read in the backward

direction, from the maximum address to zero. To form a wave between $\pi/2$ and $3/2\pi$ (III quadrant), the values of the table are read in the forward direction, from a zero address to the maximum with a negative sign. To form a wave between $3/2\pi$ and 2π (IV quadrant), the values are read in the backward direction, from the maximum address to zero with a negative sign [6].

In order to determine when, with what sign and in what direction to perform reading of the table, a flag signal is used.

Flag signals are two most significant bits of bus values $P+2$, coming from the output of the PA to the input selector. One is responsible for the reading direction (bit $P + 1$), the second one – for the half wave sign (bit $P + 2$). Together they are responsible for the quadrant in which the wave will be formed. A truth table and signal waveform picture are presented below [7].

For each complete reading cycle, there is the change of logical level of the signal, which corresponds to the change of the half wave sign. High level corresponds to the positive half wave, low level – to the negative half wave.

The input of the module data_in receives values from the phase accumulator with a word length of $P + 2$ bits (Fig. 7). Here P means the width of the address of ROM cells, and the word length of the instantaneous phase value is cut by truncating less significant bits to the address value P . The loss of the values of less significant bits does not affect the accuracy, because the value error of the G output signal is dominated by the quantization error component of the digital-to-analog converter. The word length of the address P is generally determined by the number of ROM cells. This dependence can be written as:

$$P = \log_2 k \tag{6}$$

where P – word length of the ROM cell address;
 K – number of ROM cells.

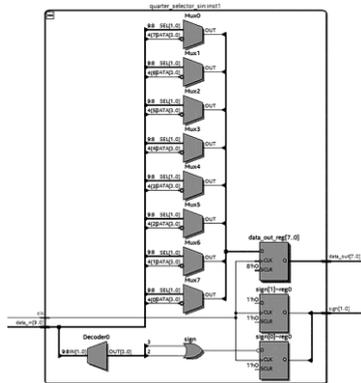


Fig. 7. Diagram of the quadrant selector in the Quartus Prime environment

The ROM contains 256 samples to generate a quarter of the sine wave. For comparison, when using a direct converter, with the values for the complete period recorded and the same memory parameters, it would have required 1024 memory

cells. This is four times more that can be critical for some chips.

The values of the sine samples from the ROM output are received for final processing in the output inverter (OI). Its task, by a sign signal from the quadrant selector, is to invert values of the synthesized half wave, thereby having formed a negative half wave (Fig. 8).

At the input, the module receives instantaneous sine values recorded in the ROM, and the sign signal from the quadrant selector. The main task of the output inverter is to turn the half wave by the signal of the negative sign, thereby having formed the complete sine period.

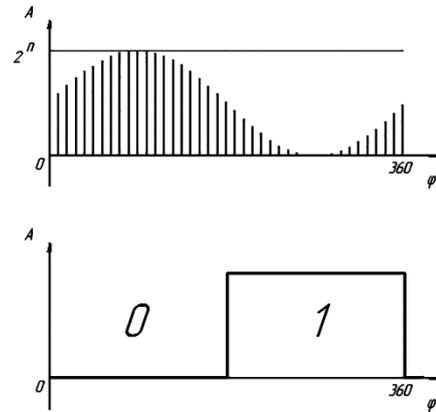


Fig. 8. Work of the output inverter depending on the sign signal of the quadrant selector

Modern ROMs allow addressing from 32 to 65536 cells, which corresponds to the word length of the address between 4 and 16 bits respectively. In this project, the selected word length of the ROM address is equal to 8 bits, which corresponds to 256 memory cells, so the input data of the quadrant selector will have a word length of $8 + 2 = 10$ bits.

III. RESULTS AND DISCUSSION

As stated above, the entire signal swing will range from zero to the supply voltage (U_{sup}) of the device. Therefore, conditionally, the zero, relative to which the positive or negative half waves are measured, will be half the supply voltage ($U_{sup}/2$) [8,9]. And in order to form a positive or negative half wave it is necessary to add discrete sine values to the digital value of the defined zero when a positive half wave signal is received and when a negative half wave signal is received, to subtract the values of samples from the value of the defined zero[10]. Thus, the amplitude of the negative half wave will be between zero and voltage $U_{sup}/2$, and the amplitude of the positive half wave – between $U_{sup}/2$ and U_{sup} .

As a result, connecting all the blocks according to the diagram (Fig. 2), a sequence of discrete sine values is created at the output of the synthesizer. If there is no need to convert to an analog form, the data can be used for mathematical processing. If it is necessary to convert the signal to an analog form, the DAC and the LFF are used.

IV. CONCLUSION

To sum up, the result of the work done on the study of direct digital synthesis is a method that describes the design of a simple frequency synthesizer based on FPGA. The obtained method does not cover all issues on the design related to the selection or the calculation of the DAC and the LFF, the effect of the element parameters of the DDS on the spectral purity of the output signal and other issues related to signal processing. However, the results can be used as a basis for further development of the subject, in-depth study, enhancement and improvement of the synthesizer. In the future, it would be easy to focus the obtained experience and knowledge on the design of synthesizers in die form and improving solutions based on FPGA, creating digital frequency synthesizers of direct digital synthesis on the domestic element base.

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