

Reform Research and Practice on Analog CMOS Integrated Circuits Design Course Based on OBE Mode

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Keywords: *Analog CMOS Integrated Circuits Design, Outcomes-Based Education, current sense*

ABSTRACT The teaching mode based on Outcomes-Based Education (OBE) is one of the newest outcomes in international engineering teaching reforms, which achieves expected study outcomes with student-centered ability-oriented methods. Based on OBE mode, a course design with theory and practice combination in “Analog CMOS Integrated Circuit Design” is proposed and analyzed in this paper. Based on the completely understanding of circuit theory, different design requirements relevant to specific engineering applications are presented to students with different abilities, which can induce positive impacts on improving the design ability of analog CMOS integrated circuits.

1. INTRODUCTION

In the 2016 International Engineering Alliance Meeting, China became a full member of the “Washington Accord” on mutual recognition of international undergraduate engineering degrees. [1] A prominent feature of the “Washington Accord” system is the establishment of “competency-based” certification standards [2], which can effectively evaluate the effectiveness of “educational outcomes” (what students learn). Besides, the ability-related indicators set clear directions and requirements for teachers and teaching institutions to design courses. In the limited teaching time, teachers should not only guide students to master the basic professional knowledge of relevant fields, but also train students to solve practical engineering problems and develop the ability to conduct independent research.

“Analog CMOS Integrated Circuits Design” course is one of the professional core courses of microelectronics major, which plays an important role in student cultivation of analog integrated circuits design theory and engineering capability. Based on Outcomes-Based Education (OBE) mode [3], a high-speed current sense circuit is adopted in this paper to illustrate the proposed reform. On the basis of explanations to circuit principle, different design requirements relevant to specific engineering applications are presented to students with different abilities, which finally requires a complete realization of current sense circuit. Through different teaching designs, a student-centered ability-oriented teaching is really realized in this paper, which can achieve the expected learning outcomes.

2. PROPOSED TEACHING DESIGN

2.1. Principle of Current Sense Circuit

Current sense circuit is an essential part of many power management circuits. For switching-mode power supply, how to accurately and instantly collect the current information on the inductance for system control has become a key technique [4]. Since the function of current sense circuit is to determine the working status of systems, it can be used to prevent the switching-mode power supply from damage under overcurrent or short circuit conditions. Besides, as a necessary technique in current-mode control, current sense circuit can determine the stability and response speed of control loop. One of the conventional structures is the resistor sampling, which is realized by adopting a resistor in series with sensed devices. Except simplification, the system efficiency is greatly affected by the resistance, especially in large-current applications. Using negative-feedback

operational amplifiers and SenseFET technique can proportionally sample the current flowing through power MOSFETs. This circuit can greatly improve the transient response and reduce static power consumption. [5, 6] Figure 1 shows the schematic of proposed current sense circuit.

In Figure 1, I_{LOAD} is the current through power transistors, V_{DD} is 5V power supply voltage, V_{DDLDO} is 1.8V LDO output voltage as an internal power supply, PM1~7, NM1~NM4, NM8~NM11 are 5V transistors, N_{LM1} and N_{LM2} are 1.8V low threshold transistors. The circuit is in charge of proportionally sensing the current I_{LOAD} through power transistors by NM1. With the clamping effect of feedback loop embedded in the circuit, the voltage at node ② is equal to the voltage at node ①. This can make the current through NM1 proportional to that through power MOS, which can be expressed as:

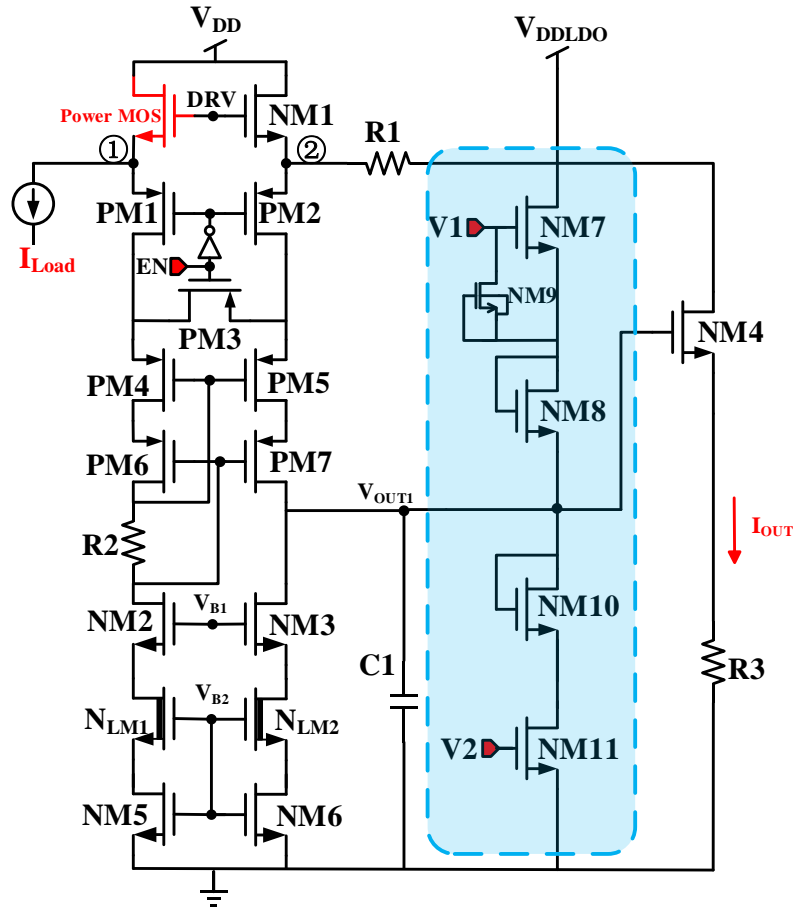


Figure 1 Schematic of proposed current sense circuit

$$\frac{I_{NM4}}{I_{power}} = \frac{S_{NM4}}{S_{power}} \quad (1)$$

where S_{NM1} and S_{power} are aspect ratios of NM1 and power MOS, respectively. The characteristics of feedback loop can be given by:

$$A_V = g_{m_{PM5}} \times R_{OUT1} \times \frac{g_{m_{NM4}}}{1 + g_{m_{NM4}} \times R_3} \times R_{ON_NM1} \quad (2)$$

$$\omega_d = 1 / R_{OUT1} C_1 \quad (3)$$

where $R_{OUT1} \approx g_{m_{PM7}} r_{o_{PM7}} r_{o_{PM5}}$; $g_{m_{PM5}}$ and $g_{m_{NM4}}$ are transconductance of PM5 and NM4, respectively. Due to the equal current value of I_{NM5} and I_{NM6} , the sampling current through NM4 and R_3 is proportional to I_{LOAD} , which can be given by:

$$I_{OUT} = \frac{S_{NM1}}{S_{power}} \times I_{Load} \quad (4)$$

Taken general indicators into considerations, the signal EN shown in Figure 1 is kept at high level. This makes the whole current sense circuit continuously work at the expense of large power consumption. For all the students, it is required to grasp the related circuit theories, such as current mirror, cascode structure, feedback control, and so on, while handling circuit tuning approaches. By this case, the theoretical knowledge and practical applications can be organically combined for students.

For inspiring the students' ability of creation, improved indicators are proposed for fast response with lower power consumption. Besides, the signal EN switches between low and high level each cycle, which means the current sense circuit is required to work only at the stage of current sensing. Therefore, there is a contradiction between low power and fast response in conventional methods, which demands students to create improved structures. For example, the circuit with blue frame in Figure 1 is one effective method. The auxiliary voltage clamping circuit formed by NM7~11 limits the output voltage of the operational amplifier to speed up the circuit. At the same time, it also suppresses the overshoot of V_{OUT1} and prevents the system from false triggering. V1 remains high when EN is low, which means NM7 and NM8 turn on to keep V_{OUT1} at a certain voltage to accelerate startup when the operational amplifier is not operating. V2 is a narrow pulse signal. Because the output capacitance is small for large bandwidth, overshoot often occurs when the operational amplifier starts. At this time, the NM10 and NM11 turn on for a while to suppress overshoot. When the operational amplifier is working normally, V1 and V2 are low, and NM7~11 turn off. The whole operational amplifier only works during the on time of power MOS. During the sleeping period of operational amplifier, only the auxiliary circuit is turned on to maintain the bottom limit of V_{OUT1} . With the part-time and assistant mechanism, fast response can be realized with lower power consumption.

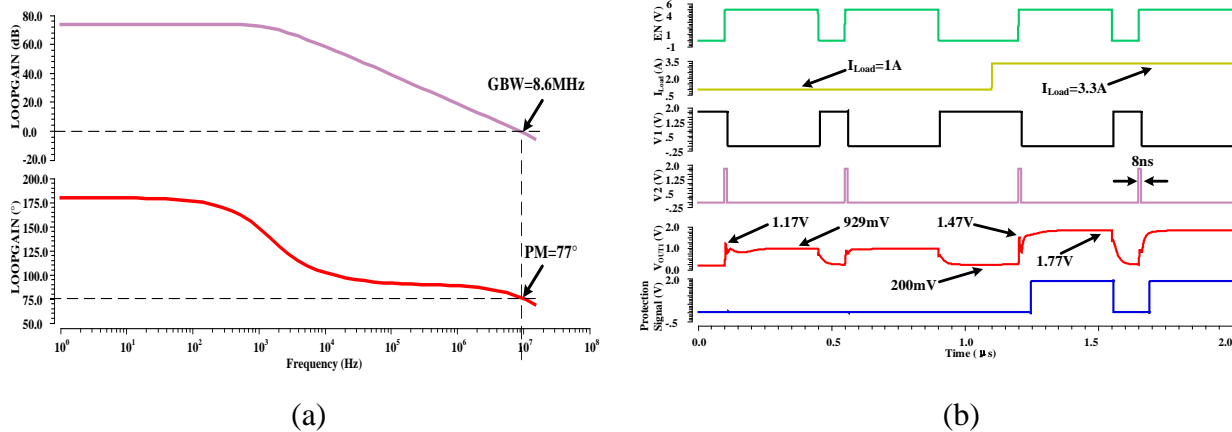


Figure 2 Simulation results. (a) Characteristics of feedback loop, (b) Timing diagrams of current sensing

2.2. Indicator requirements

According to the function of current sense circuit, it's performance should meet the following requirements in Table 1 and Table 2.

Table 1 The general indicators of current sense circuit.

Bandwidth (GBW)	> 8MHz
Phase Margin (PM)	> 60°

Table 2 The improved indicators of current sense circuit on the basis of general indicators.

Working Mode	Part Time
Working Current Consumption	< 3μA
Switching Frequency	> 2MHz

2.3. Simulation results of proposed circuit

The current sense circuit was simulated in a 0.18 μ m standard CMOS process. The characteristics of feedback loop in current sampling are shown in Figure 2 (a), where a 8.6MHz bandwidth and 77°phase margin is realized with 2 μ A on-state current consumption in the proposed structure. Figure 2 (b) is the timing diagrams of the sensing procedure. When $I_{LOAD} = 1A$, the system does not over-current. It can be seen that V_{OUT1} has an overshoot when the EN is turned up, and the narrow pulse signal V2 with a pulse width of 8ns effectively suppresses overshoot. Hence, V_{OUT1} will not cause false triggering for following protection mechanism. V_{OUT1} is 929mV in stable state. When $I_{LOAD} = 3.3A$, the system is in an overcurrent state. V_{OUT1} is 1.77V in stable state and the signal of following protection mechanism is changed to high level. When EN is low, the control signal V1 is high, and the output voltage is kept at about 200mV to ensure the lower limit of the operational amplifier's output voltage for accelerating the transient response.

3. Summary

Based on the teaching design of current sense circuit, the circuit principle is completely explained to students. Two different design requirements are provided to students with different abilities, which include a series of general indicators and a series of improved indicators. In the proposed teaching reform of "Analog CMOS Integrated Circuits Design" course, the OBE mode runs through the entire teaching process. In the teaching of analog integrated circuits design, actual engineering design capabilities are emphasized on the basis of theoretical knowledge. Besides, the student-centered ability-oriented concept is deepened in the proposed method, which can realize individualized teaching and inspire potential abilities of students. By this method, expected learning outcomes can be achieved by students with different abilities, so as to expand and maximize the ability of solving practical engineering problems in analog integrated circuits design.

Acknowledgment

This research was financially supported by the reform project of University of Electronic Science and Technology of China education, Industry-university cooperative education project approved by Ministry of Education, and National Natural Science Foundation of China (61674025).

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