On the Efficiency of China's Semiconductor Industry Based on the Meta-frontier DEA

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ABSTRACT
Due to the Sino US trade war in recent years, the semiconductor industry in mainland China has faced strong international competition. The industry has been taking actively strategic transformation and upgrading technical level and the government policy has also greatly supported and assisted. Since there are three categories in the industry-upstream, middle and downstream, their technical levels and capital investment are also different, so the main supporting direction of government should be focused to avoid improper resource allocation. In this paper, the concept of meta-frontier DEA will be used to calculate the technology gap ratio (TGR) of sub-industries to understand the efficiency differences between the three ones for avoiding the traditional efficiency evaluation method which can only consider the same technical level. Finally, a forward better policy direction based on this study is offered.

Keywords: *Semiconductors, Meta-frontier DEA, Technology gap ratio, Technological capabilities.*

1. INTRODUCTION

This paper mainly discusses the differences of performance of IC design, IC manufacturing and packaging test, which are three major sub-industries in the semiconductor industry in mainland China.

Firstly, literature review focuses on the comparison between meta-frontier DEA and traditional DEA.

Secondly, the input-output variables that affect the performance of enterprises are adopted. In order to meet the requirements of DEA model, the number of DMUs should be larger than 2 times of that input adds output variables, only IC-design and IC-manufacturing industries will be discussed in this study.

Finally, through further in-depth analysis, draw a conclusionand put forward policy recommendations.

2. LITERATURE REVIEW

More and more attention has been paid to the method of efficiency evaluation based on the meta-frontier DEA model. The basic concept is first seen in Hayami (1969) [1] and Hayami, Y., & Ruttan, V. W., (1971) [2], who first put forward the concept of meta-production, which regards as the envelope curve of the general production function in the neoclassical school. Battese (2002) [3] regards meta-production as the envelope of the most efficient production point and the assumption is that all producers do not have the same production technology. For example, there will be different levels of production technology due to differences in countries, regions, and sub-industries which even in the same main industries etc., so when estimating efficiency, all manufacturers should not be regarded as having the same level of production technology. These firms should be grouped and then the efficiency values of each group should be estimated respectively. Then, the efficiency values estimated by the meta-frontier of individual firms and the efficiency values estimated by each group are divided; the technology gap ratio (TGR) is obtained and used for the main index of evaluation. Rao et al. (2003) [4] used both DEA and SFA methods to estimate the common production boundary, aiming at 97 countries in four regions, including Africa, America, Asia and Europe, to evaluate the differences of agricultural productivity across regions. Battese et al. (2004) [5] adopted a linear programming method and panel data to calculate the meta-frontier production frontier of Indonesian textile industry, and compared the differences of technical efficiency and technology gap ratio among different regions and technical levels. For the industry of semiconductor, there are little evaluation method of

meta-frontier method but other methods used. Hongkuan Li et al.(2018) [6] adopted a framework based on generalized three-stage DEA model, grey relational analysis theory and disparity disassembly. They found that China's semiconductor industry, except package test, has overall increasing innovation efficiency with different trends and levels. A lower level innovation will restrict the further improvement for the innovation efficiency. A range of input redundancies were found mostly in manufacturing and equipment and that comes from the concerted support of government to particular companies. Xiaoyang Zhoua et al. (2019) [7] used a hybrid method to study the performance issues of semiconductor industry in China. The empirical results show that a significant efficiency gap between China and the US existed in the IC industry during 2008–2017 and the most one is in IC packaging & testing segment since more redundant inputs of labour investment in China. A special result is that the performance improvement of IC packaging & testing is relatively obvious than the other two segments. It seems that a labour orient input had played an important role for the efficiency improvement for specific segment but will lose the strength gradually. Even the above researches have find attractive results for the efficiency of semiconductor industry in China, the discussion for the pre-classification of different segment of the industry seems not be mentioned. In Taiwan, Chingren CHIU et al. (2018) [8] explored the performance of semiconductor industry in Taiwan basing on the meta-frontier approach and evaluated dynamic performance with the Malmquist productivity index. The results show that the negative growth among semiconductor industry segments in Taiwan is different. The negative growth of IC packaging and testing companies and IC design ones are from a backward movement in technical change, but that of IC manufacturing companies are caused from a pure technical efficiency decline. It will cause the attention of that the different efficiency among those different segments (or say as sub-industry) in a industry through the above researches.

In this study, the meta-production concept proposed by Battese (2002) [3] will be used as the performance envelope to classify the upstream, middle stream of semiconductor industry in China, and try to discuss the efficiency of different semiconductor sub-industries .

3. RESEARCH METHODS

A set of *S* peer DMUs each with *N* inputs and *M* outputs is considered; the *xki* and *yli* are separately denoted as the values of the *k-th* input ($k \in Q_+^N$, Q_+^N represent input vector) and the *l-th* output ($l \in Q_+^M$, Q_+^M represent output vector) of DMU*i* ($i \in Q_+^S$, Q_+^S represent DMUs vector) (Chingren CHIU et al., 2018) [8]. The meta-technology set in period *t* can be represented as follows:

$$W^{n,t}(x^t, y^t)=\{(x^t, y^t)=x^t \text{ produce } y^t\} \quad (1)$$

The directional meta-distance function in period *t* is defined as follows:

$$\overrightarrow{DF}^{n,t}\left(x^t, y^t, -d_x, d_y\right)=\sup\left\{\alpha^{n,t}: \left(x^t-\alpha^{n,t}d_x, y^t+\alpha^{n,t}d_y\right)\in W^{n,t}\right\} \quad (2)$$

Where the non-zero direction vector $d=\left(-d_x, d_y\right)$ determines the directions where inputs and outputs are scaled. The DMUs could be divided into *Z* groups. *T*he group technology set can be defined as $W^{z,t}$, and The *z* group directional distance function in period *t* is defined as $\overrightarrow{DF}^{z,t}\left(x^t, y^t, -d_x, d_y\right)$, *z=1,2,…,Z.*

The ratio of technical efficiency of the meta-frontier (TE^n) and that of the *z-th* group frontiers (TE^z) is referred to as the technology gap ratio (TGR^z) and is a number between 0 and 1. When the TGR^z is closer to 1, it means the technical efficiency of the group frontiers is closer to the technical efficiency of the meta-frontier, conversely, farther away. Because the semiconductor industry is mostly order oriented, the Input-oriental model would be considered. According to the Moore's law, BCC model is taken for comparison.

Revenue and net profit are taken as outputs and COG, net fixed assets and R&D are as inputs. The data source is the annual report data published and based on the year-end date in 2019 when the Sino US trade war was starting. Since the number of downstream companies of IC test and packaging are less than 10, it will not be judged when the numbers of DMUs are less than 2 times of that input adds output variables. This sub-industry will not be discussed. 46 listed semiconductor companies (upstream: IC-design 23, middle: IC-IDM 23) are selected where deducting missing data, negative net profit and special treatment from the stock exchanges of Shanghai and Shenzhen.

4. RESULTS

From the table 1 which represents the efficiency value of IC-design companies separately by meta-frontier model and general BCC model, there are 19 companies be found the TGR is 1, that much more efficient companies are found by meta-frontier model than by BCC model. Contrarily, from the table 2 which represents the efficiency value of IC-Manufacturing companies, it shows that there are more inefficient companies be found. Only 3 companies has the TGR=1. It is less than the 7 efficient companies found by BCC model. From the view of average value, the TGR is 0.99 higher than 0.84 by BCC model in IC-Design industry; in IC-Manufacturing industry, the TGR is 0.85 lower than 0.88 by BCC model.

Table 1.IC-Design companies' efficiency estimated by meta-froniter model and BCC model

NO	DMU	Cluster	Technology Gap Ratio	Score (BCC)
1	ICD1	1	1	1
2	ICD10	1	1	1
3	ICD11	1	0.997871236	0.769237644
4	ICD12	1	1	0.708838391
5	ICD13	1	0.977752802	0.900718614
6	ICD14	1	1	1
7	ICD15	1	1	0.937789919
8	ICD16	1	0.981350069	0.75436684
9	ICD17	1	1	0.842456981
10	ICD18	1	1	1
11	ICD19	1	1	1
12	ICD2	1	1	1
13	ICD20	1	1	0.648262581
14	ICD21	1	1	1
15	ICD22	1	1	1
16	ICD23	1	1	1
17	ICD3	1	1	0.435501129
18	ICD4	1	1	0.749668236
19	ICD5	1	0.974638059	0.738167954
20	ICD6	1	1	0.542687009
21	ICD7	1	1	0.744935336
22	ICD8	1	1	0.827136046
23	ICD9	1	1	0.652312001
	Mean		0.997026616	0.837046899

Table2. IC-Manufacturing companies' efficiency estimated by meta-frontier model and BCC model

NO	DMU	Cluster	Technology Gap Ratio	Score (BCC)
24	ICI1	2	0.994274173	0.939718041
25	ICI10	2	0.989733431	0.854516217
26	ICI11	2	0.936347258	0.930996063
27	ICI12	2	0.748189196	0.786618759
28	ICI13	2	0.775964728	0.761138491
29	ICI14	2	0.747653059	0.783793431
30	ICI15	2	0.662140208	0.851535347
31	ICI16	2	1	1
32	ICI17	2	0.614116068	0.75436684
33	ICI18	2	0.88623109	0.900023691
34	ICI19	2	0.770401068	1
35	ICI2	2	0.996595297	1
36	ICI20	2	0.899483792	0.797138606
37	ICI21	2	0.7567609	0.922847629
38	ICI22	2	0.773415674	1
39	ICI23	2	0.931337484	0.959670407
40	ICI3	2	0.954118563	0.952731612
41	ICI4	2	1	1
42	ICI5	2	0.684464885	0.700439571
43	ICI6	2	0.770565413	0.754628159
44	ICI7	2	0.737210659	0.593316691
45	ICI8	2	1	1
46	ICI9	2	0.951680152	1
	Mean		0.851334048	0.880151285

5. CONCLUSION

Through the meta-frontier DEA model, the efficiency value of each company from the sub-industry groups can be re-examined. As the result shows, more efficient enterprises can be found in IC design group, and less efficient ones in IC manufacturing group; from the perspective of average efficiency value, the overall efficiency of IC design industry has a higher value, while that of the IC manufacturing industry is lower. Therefore, if meta-frontier model is not be used, it will be thought that the two sub-industries have similar efficiency status, the government will adopt the policy of rain and dew. However, in fact, the IC design industry is closer to application markets, theywill respond quickly to show better efficiency. Only the IC manufacturing industry needs more policy support.

AUTHORS' CONTRIBUTIONS

Chiencheng Lin: Topic and research frame construction, theory finding, paper writing.

Gwohau Ding: publication finding, corresponding.

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