A Grid-Connected ZVS Single Phase Full Bridge Inverter with DF THI PWM Scheme

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Abstract. This paper proposes the modulation scheme for grid connected full bridge inverter of single phase configuration to achieve ZVS condition with auxiliary switch. The THI PWM strategy is employed to control the auxiliary switch which is evolved from ZVS THI PWM, the DF modulation scheme is incorporated to generate auxiliary switching pulse. The ZVS THI PWM scheme is employed simultaneously on grid connected full bridge inverter and its performance is observed. The ZVS condition of inverter switches is also achieved by short circuit pulses generated from auxiliary switching pulses. The proposed control scheme with THI PWM and DF modulation scheme is modeled, the performance of full-bridge inverter of single phase configuration with control scheme is analyzed using MATLAB. The results depict that the proposed converter control scheme exhibits better performance compared to DF SPWM.

1 Introduction

The single phase full bridge inverter is the most commonly used inverter topology for uninterrupted power supply and domestic small scale l PV generation systems for residential, commercial and industrial purposes depending upon the utilization of electrical power [1]. The power ratings of inverter are designed based on the application. The developments of inverters are being done since its invention with different modules or methods.

The inverter is relied upon to work with higher frequency to reduce the filter size but the switching losses which rapidly increases with the switching frequency makes it difficult to operate and control the high switching frequency converters. In single phase inverter topology the MOSFET switching frequency is also influenced by the body diode's poor dynamic performance. During the process of reverse recovery in the diode, the high dv/dt and di/dt may also damage the device. MOSFET is rarely employed compared to IGBT with fast anti-parallel in the full-bridge topology with hard switching. For above reasons, the full-bridge inverter with hard switching is restricted below 20 kHz, which results in low power density and large filter sizes.

The predecessors had proposed many topologies to minimize the reverse recovery issue of MOSFET. The H6 inverter topology is proposed with two diodes and two transistors in which the body diode of the MOSFET is activated. Dual buck converter

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in the external circuit bypass these body diode of MOSFET thereby reducing the losses in the MOSFET. In such topologies, where four phase legs are employed with one series MOSFET and one external diode the requirement of the filter inductors also increases, thereby increasing the filter size. However, the switching frequency is still a major concern in these topologies because the switching devices are triggered by hard switching.

Alternatively, in order to mitigate the reverse recovery and to minimize the switching loss the soft switching method is applied, and well addressed by the authors in the literature. The Zero Voltage Switching (ZVS) for all the switching devices are achieved in the resonant dc link three-phase inverter (RDCL) in [2] and active clamping resonant dc link three-phase inverter (ACRDCL) in [3] but by the use of discrete pulse modulation, undesirable sub-harmonics are caused.

In the recent years, a number of single phase inverters with soft switching technique are also proposed [4, 5]. The ZVS condition is acquired by utilizing the high reverse recovery energy from the external slow recovery anti-parallel diodes in the resonant dc-link full bridge inverter which are employed by the active-clamping technique and classical bipolar PWM scheme [4]. However, the voltage stress of the inverter is higher than the dc bus voltage. By changing the auxiliary resonant branch configuration and a modified unipolar PWM scheme is applied to achieve the Zero voltage switching in ZVS dc link single phase inverter in to clamp the device voltage to the dc bus voltage [5]. From the above topologies, the ZVS full-bridge inverter [4, 5] have simple structure but the inverter modulation scheme in [4] has high circulation loss. In order to optimize the performance, a novel ZVS THI PWM with DF modulation scheme is proposed. To control the energy flow in the auxiliary resonant branch [6, 7], a new method which generates short circuit pulse in every switching cycle with the help of adjustable technique. This proposed for the purpose of executing the ZVS scheme. The ZVS third harmonic injection scheme with DF modulation is proposed. MOSFETs are employed to obtain ZVS for both main and auxiliary switches are realized. The filter size is reduced with higher switching frequency. According to the different load conditions, the duration of the short-circuit stage varies for optimizing the efficiency in both light and heavy load cases.

2 Literature Survey

The ZVS method of soft switching in full bridge inverter is commonly used method of switching; many modifications have been made to improve the output of the inverter. The -polar PWM scheme and the reverse recovery energy of the diodes is applied for applying active clamping technique to the resonant dc-link full bridge inverter [4]. Here, the ZVS condition is obtained by using the high reverse recovery energy of the external slow recovery anti-parallel diodes. The disadvantage is the voltage stress on the inverter switches is higher than the dc bus voltage.

In [5], in order to achieve ZVS by the configuration of the auxiliary resonant branch is changed and a modified unipolar PWM scheme is applied for implementing ZVS scheme. With this, the voltage stress on the switch is reduced and clamped to the dc link voltage. The PWM scheme employed in [5] can be used for controlling the inverter

output. To acquire system optimum performance and to attain ZVS at various load power factors. The features of inverter [5] are all the switches are operated in zero voltage switching mode, the resonant inductor control the di/dt by reverse recovery, lossless capacitive snubber's are used for reducing the turnoff losses. Hence the voltage stress to the devices is only the DC bus voltage.

The simple ZVS-PWM [10] commutation cell is employed in to achieve a new ZVS PWM single phase inverter. Here, the main switches are use ZVS turn-on and turn-off except for the auxiliary switches whereas the ZCS turned on and turnoff. The soft switching is employed to attain the ZVS. The two small coupled magnetics in one resonant pole is employed in with a novel soft switching inverter to ensure the main switches operating at zero voltage switching (ZVS) at zero load to full load and the auxiliary switches at zero current switching (ZCS) with small current stress and load capability. The outstanding features of coupled magnetics are capacitor charge has no limitation; commercial use of half bridge module; the peak current of auxiliary switches and diodes are reduced because during the switching transition, the transformer primary and secondary windings are sinking or supplying the resonant current; simplified gate timing control because of non-unity of couple magnetics. Anyhow, the problem is that the magnetizing inductor cannot be reset in the basic ZVS inverter using coupled magnetics.

To achieve the ZVS in single phase full bridge inverter, the soft switching technique is employed instead of hard switching. The soft switching in PWM technique also suppress the reverse recovery and the switching losses are reduced. The above mentioned inverter topologies employ soft switching technique to achieve ZVS turn-on and turn-off.

3 Modelling

The auxiliary resonant branch is established between the dc-link and the dc-to-ac converter which is shown in Fig. 1, the capacitors Cr1–Cr4 are paralleled to respective inverter switches with anti-paralleled diodes to ensure ZVS-turn on of the switches during resonant process.

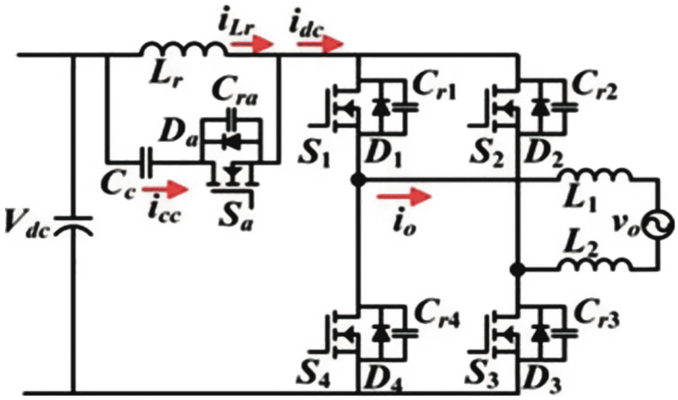

Fig. 1. Full-bridge dc-to-ac converter of single-phase

The modeling of the dc-to-ac converter can be attained with the control of auxiliary switch across the resonant. It is controlled with uni-polar THI-PWM and DF modulation scheme where the auxiliary switch is turned-on and turned-off twice in a switching cycle.

The ZVS-turn on of the switches in dc-to-ac converter and the auxiliary switch (Sa) of resonant branch is achieved in two stages with DF modulation in combination with uni-polar THI PWM. The first resonant process involves in ZVS-turn on of dc-to-ac converter switches and the later resonant stage helps in ZVS turn-on of auxiliary switch.

In Fig. 2, the resonant circuit and its equivalent helps in determining the currents in the switches which are discharged by the resonant inductor current and charges the auxiliary switch capacitor installed across it but the load current flows without involving in the resonant process. It can be known from (1)

$$i_{Lr} + i_{Cra} = i_{Cr1} + i_{Cr2} \tag{1}$$

$$\begin{aligned} i_{Lr} &= -|i_{Cr3}| - |i_{Cr4}| - |i_{Cra}| \\ &= -|i_{Lr}| \end{aligned} \tag{2}$$

After the first resonant process, the switches S2, S4 must be turned-off with the THI-PWM scheme so capacitors paralleled to these switches are charged during the later resonant process as in Fig. 3.

The ZVS turn-on of the auxiliary switch (Sa) is realized during the second resonant process which adds the advantage to the full-bridge dc-to-ac converter of ZVS. The currents in the resonant process is known from (3)

$$i_{Lr} + i_{Cra} = i_{Cr2} + i_{Cr4} + i_0 \tag{3}$$

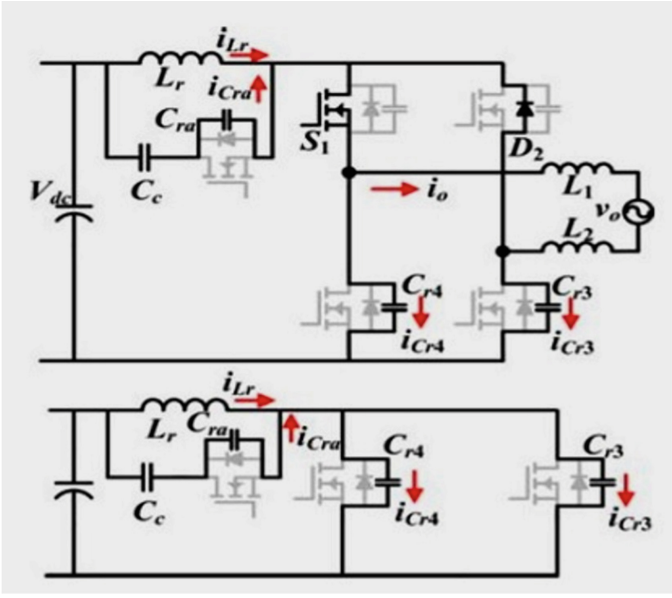

Fig. 2. Resonant circuit and its equivalent circuit with uni-polar THI PWM

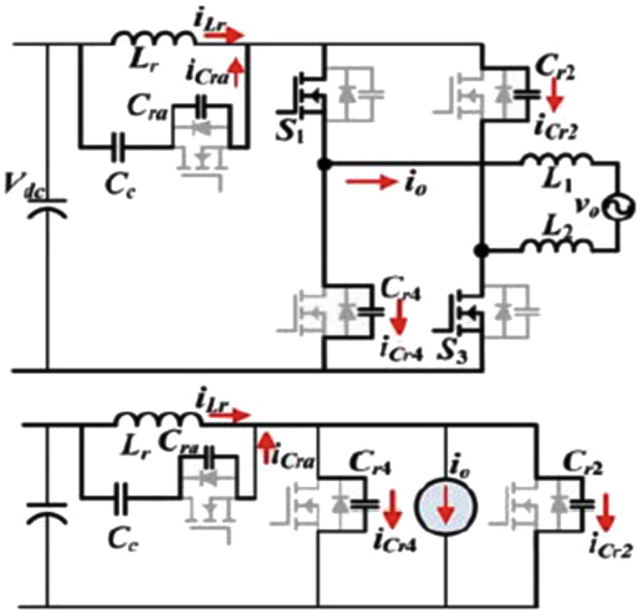

Fig. 3. ZVS-turn on of Auxiliary switch with second resonant process

$$\begin{aligned} i_{Lr} &= |i_{Cr2}| + |i_{Cr4}| + |i_{Cra}| + |i_0| \\ &= |i_{Lr}| \end{aligned} \tag{4}$$

The Eq. (4) signifies that the inductor current is reversed before the second resonant process so that the resonant inductor must be charged with larger amplitude than the paralleled capacitor resonant currents and the load current. After the resonant process, the S1, S3 switches are ZVS turned-on as in Fig. 2 and the diodes D2 and D4 charges the resonant inductor with the reverse recovery current when the stage of reverse recovery starts but the reverse recovery current increases the circulation current loss in light load conditions.

Here, the short-circuit pulse is proposed to charge the resonant inductor with the DF THI-PWM. Instead of using the anti-parallel diodes for charging the resonant inductor, the charging path is realized by switching-on all switches of dc-to-ac converter with the short-circuit pulse. The dc-side voltage charges the resonant inductor and the proposed short-circuit pulse can adjust its energy according to the load current amplitude at instants.

The proposed model of full-bridge dc-to-ac converter of single-phase configuration with DF THI-PWM and short-circuit pulse is implemented. The pulses for the auxiliary switch is achieved by the carrier of triangle wave of double the frequency of the carrier of triangle wave employed for the realization of dc-to-ac converter pulses which is compared with the THI-PWM reference wave. The short-circuit pulse is complementary of the auxiliary switch pulses with some delay.

THI-PWM

The third-harmonic PWM is analogous to the selected harmonic injection strategy and it is executed in an indistinguishable way from sinusoidal PWM. It has a distinctiveness that the reference signal used (Vr) is not sinusoidal however comprise of both a fundamental signal component (V1) and a third-harmonic signal component (V3) [8, 9]. Subsequently, the resulting reference function from the peak-to-peak voltage amplitude of waveform does not surpass the DC supply voltage Vs, rather the fundamental component is high is magnitude compared to the supply Vs. Reference voltage Vr is compared with signal that is of frequency three times that of the of fundamental frequency and magnitude is 1/6th of that of the fundamental amplitude. The output voltage generated by THI PWM strategy is 1.15 times the output generated by SPWM.

The amplitude peak of the reference signal of THI PWM is reduced as it is a flat-topped waveform. Due to which, the linear modulation index increases and the width of the pulses also increase. Thereafter, the magnitude of the output voltage increases. The number of pulses generated reduces and the switching loss becomes low.

The sinusoidal PWM is the simplest modulation strategy to understand but the DC bus supply voltage is not completely utilized. Because of this issue, the THI PWM technique is employed to enhance the inverter execution. The sinusoidal PWM method causes diminish most extreme output voltage. For this situation, an expansion of most extreme achievable output voltage is studied. Subsequently, by essentially adding a third harmonic signal to each of the reference signals, it is conceivable to acquire a noteworthy adequacy increment at the output voltage without loss of quality, as represented in Fig. 4.

On the other hand, the reference signal takes two maxima at wt = π/3 and wt = 2π/3 equal to 1. The first and third harmonic equations are given by

$$V_1 = \mathrm{V}_{1max} \sin wt \tag{5}$$

$$V_3 = \mathrm{V}_{3max} \sin(3wt) \tag{6}$$

Therefore, when wt = π/3, the first harmonic of the output voltage (line to neutral) takes the value Vbus/2. By substituting in Equation

$$`V_{bus}/2 = \mathrm{V}_{1max} \sin(\pi/3) \tag{7}$$

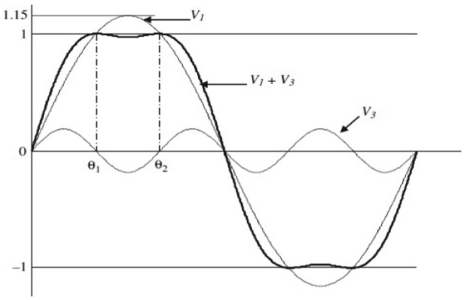

Fig. 4. Third Harmonic Injections to the Reference Signal

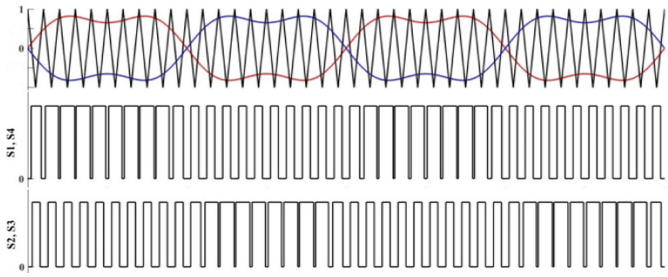

Fig. 5. Generation of THI PWM pulses

Accordingly, the amplitude of the first harmonic results

$$V_{1max} = V_{bus}/1.732 \tag{8}$$

There is no significant decay in the quality of the wave form. In each phase the third harmonic wave given as reverence is given by

$$V_{1max} \sin wt + V_{3max} \sin(3wt) \tag{9}$$

The Eq. (9) represents the THI PWM for phase voltage injected into the PWM.

The generation of gate pulses through THI PWM strategy is represented in the Fig. 5. The frequency of reference signal decides the frequency of inverter. The carrier signal frequency is higher than the reference signal by which the number of gate pulses is generated. The THI PWM strategy provides better output voltage than SPWM and the number of pulses are reduced due to which switching losses becomes low.

4 Switching Scheme

The scheme of switching pulses to trigger the switches of dc-to-ac converter for the switch S1, the sine-reference wave is injected with its third fundamental frequency to attain the THI-reference and is compared with the carrier triangle-wave. The resultant signal is sampled to OR logic with the short-circuit pulse (Vsc) which is the enhanced pulse for the switch S1. For the S4 pulse, the resultant signal of the S1 is complemented with NOT logic and is sampled to OR logic with the short-circuit pulse (Vsc) and vice-versa for S3, S4 switches with a reference wave of 180° phase shift.

The auxiliary switch pulses are attained by comparing the THI-reference signal with the carrier of triangle wave of frequency which is double the carrier signal frequency of main switches. This resultant signal is combined with the resultant pulses of S1, S3 switches using OR logic to obtain (Vgsa). And the complementary of this Vgsa with unit delay results in the short-circuit pulse (Vsc). The pulse generation circuit is represented in Fig. 6.

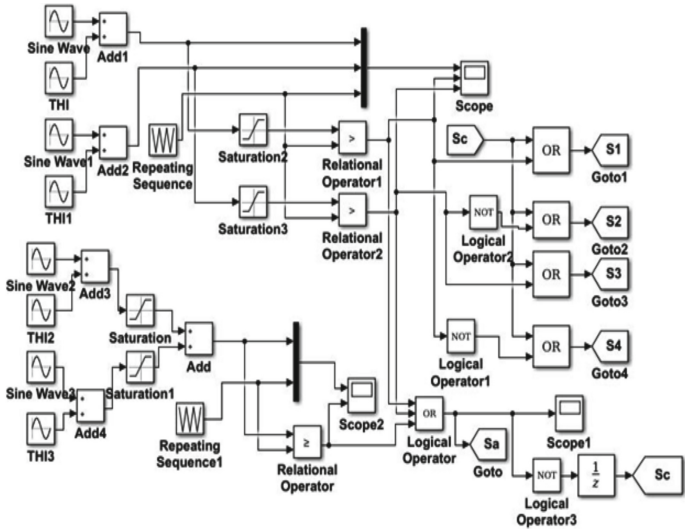

Fig. 6. Switching Scheme of proposed model

5 Control Strategy

The control scheme of DF THI-PWM and short-circuit pulse on full-bridge dc-to-ac converter of single-phase configuration is proposed. This control scheme is an enhanced PWM where the ZVS THI-PWM and DF THI-PWM is obtained simultaneously to achieve ZVS of dc-to-ac converter and ZVS of auxiliary switch of resonant branch. The proposed model can be implemented with open-loop as well as feedback-loop conditions.

Closed-Loop Condition

The block diagram of closed-loop full-bridge dc-to-ac converter with ZVS THI and DF THI PWM is represented in Fig. 7. It is mainly to generate the pulses to attain better output voltage at the dc-to-ac converter. The grid-voltage is sampled as the reference voltage in per unit value and is fed to PLL block to maintain same phase for the signal to be generated. The phase from PLL is combined with the reference current iref and compared with the load current. This error is fed to the PI controller which produces the voltage signal. This signal is combined with the output voltage (V0) and is utilized as the reference voltage to generate the pulses. The reference signal from the feed-back replaces the reference sine-wave in the open-loop condition and generates the pulses for the auxiliary switch of resonant branch in full-bridge grid connected dc-to-ac converter. This pulse is combined with the resultant signal of S1, S3 as mentioned in the switching section to produce auxiliary pulse. The short-circuit pulses evolved from the auxiliary pulses with unit delay can be utilized to adjust the resonant inductor energy avoiding the high reverse recovery current.

The phase output of PLL and the output grid current (i0) is sampled and fed to ZVS THI-PWM block where this sampled signal is utilized as the reference signal instead of sine-wave of fixed magnitude and phase to generate pulses for switches S1, S2, S3, S4 respectively as shown in Fig. 6 (Table 1).

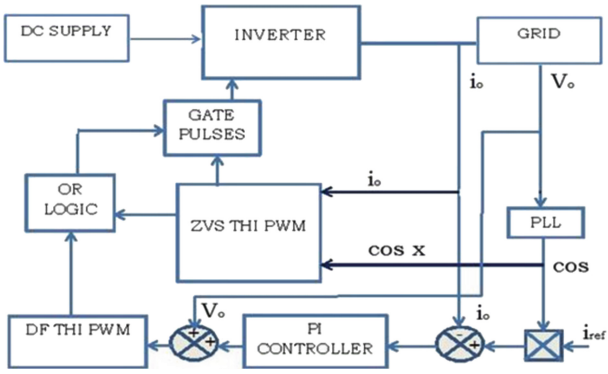

Fig. 7. Block Diagram of Closed-loop of full-bridge dc-to-ac converter with ZVS THI and DF THI PWM

Table 1. Parameters of the Model

Parameter	Symbol	Value
Dc voltage	V_{dc}	360 V
Grid Voltage	V_o	230 V rms
DC bus capacitor	C_{bus}	1.5 mF
Filter Inductor	L_1 and L_2	140 μH
Resonant Inductor	L_r	7.2 μH
Clamping Capacitor	C_c	20 μF
Parallel Capacitor	C_{ext}	0.576 nF
Parasitic Capacitor	C_{osse}	0.192 nF

6 Simulation Results

The proposed circuit is modeled using MATLAB Simulink is represented in Fig. 8. It is controlled with the DF THI-PWM and DF SPWM simultaneously at both open-loop and feedback-loop condition.

Open-Loop Condition with DF SPWM & DF THI-PWM

The DF SPWM scheme of control is similar to DF THI-PWM and it is implemented along with short-circuit pulse to attain ZVS of auxiliary switch as well as switches of dc-to-ac converter. The output voltages of the proposed model with comparison of DF SPWM and DF THI-PWM are represented in Fig. 9. The variation of the output voltage magnitude in the open-loop condition is not appreciable.

The FFT analysis of the proposed model with the DF SPWM scheme of control at open-loop condition is represented in Fig. 10. The magnitude of output voltage can be known from below Fig. 10 as 251.9 V with the THD of 4.98%.

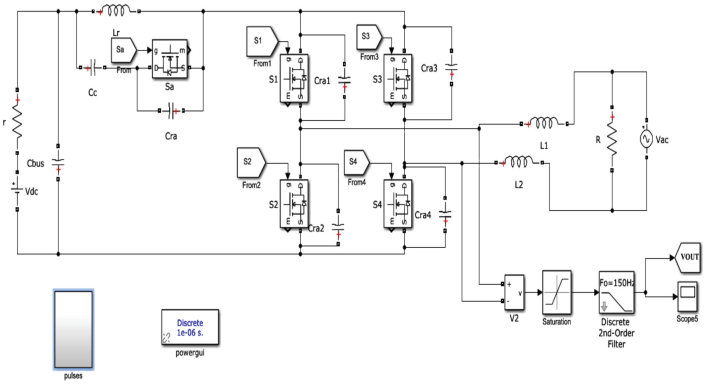

Fig. 8. Circuit diagram of Proposed model

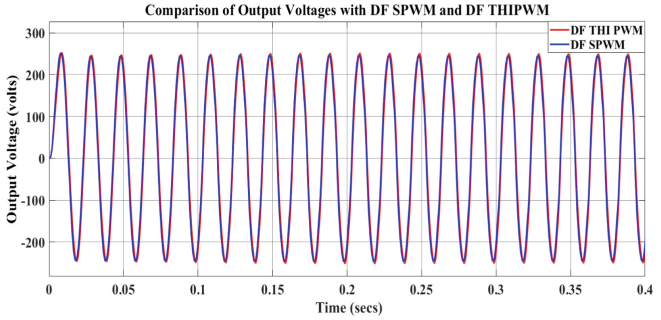

Fig. 9. Output Voltages with DF THI-PWM & DF SPWM

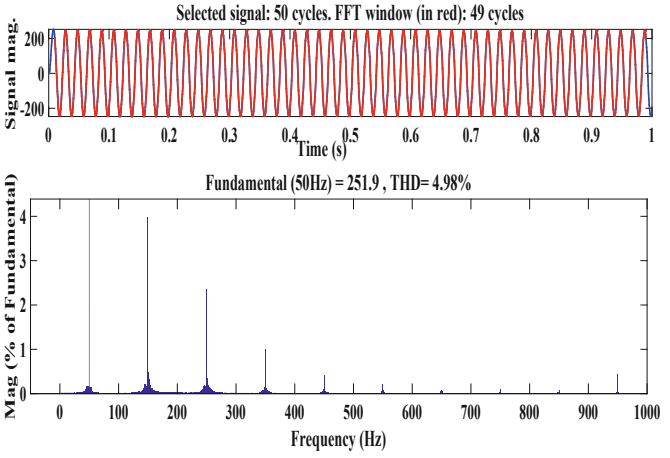

Fig. 10. FFT analysis with DF SPWM at open-loop condition

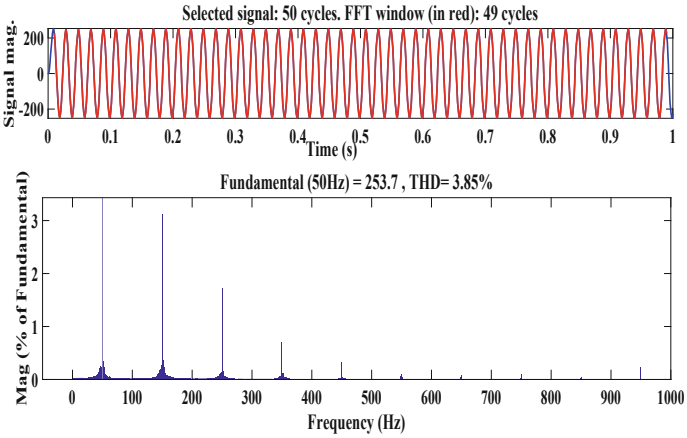

Fig. 11. FFT analysis with DF THI-PWM at open-loop condition

Table 2. Comparison of DF SPWM & DF THI-PWM at open-loop condition

PWM TYPE	Output voltage (v)	THD%
DF SPWM	251.9	4.98%
DF THI-PWM	253.7	3.85%

The FFT analysis of the proposed model with DF THI-PWM scheme of control at open-loop condition is represented in Fig. 11.

The magnitude of output voltage can be known from the Fig. 11 as 253.7 V with the THD of 3.85%.

From the above open-loop condition analysis, the DF THI-PWM is better compared to DF SPWM in-terms of voltage and THD but the output voltage is beyond rated (Table 2).

7 Closed Loop

In the closed-loop condition, the proposed model is implemented with the DF THI-PWM and DF SPWM along short-circuit pulse. The feedback system is designed with PLL and PI controller where the grid voltage in per unit value is considered as reference voltage to produce the reference carrier signal for DF THI-PWM and ZVS THI-PWM. The Fig. 12 represents the feedback loop for DF THI-PWM and ZVS THI-PWM.

The resultant signal from the feed-back loop is fed to the ZVS THI-PWM and DF THI-PWM blocks to generate pulses. By comparing the resultant signal DF_THI with the triangle carrier wave and these pulses are combined with the resultant pulses of S1, S3 using OR logic to achieve auxiliary pulses which attains the ZVS condition of auxiliary switch. The short-circuit pulse is a complementary of auxiliary switching pulse

with unit delay which is combined with the pulses of each switch in the circuit model to attain the ZVS of the dc-to-ac converter switches represented in Fig. 13.

The proposed circuit model is implemented with both DF SPWM and DF THI-PWM scheme of control along with short-circuit pulse and their output voltages are compared which is represented in Fig. 14. The variation of output voltages can be observed from the Fig. 14 which indicates that the output voltage of this dc-to-ac converter with DF THI-PWM and DF SPWM is more.

The FFT analysis of the proposed model with the DF SPWM scheme of control at closed-loop condition is represented in Fig. 15. The magnitude of output voltage can be known from below Fig. 15 as 236.6 V with the THD of 3.97%.

The FFT analysis of the proposed model with DF THI-PWM scheme of control at closed-loop condition is represented in Fig. 16.

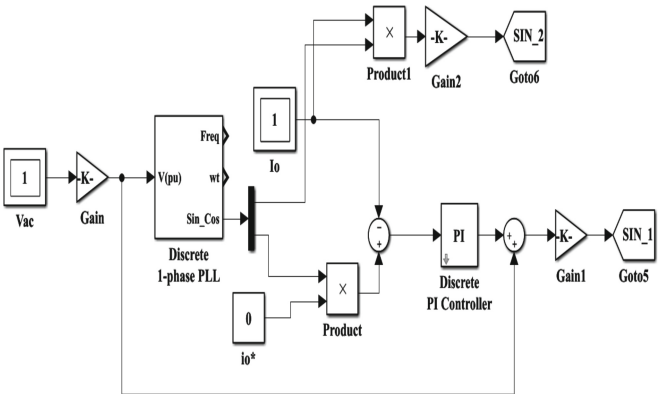

Fig. 12. Feedback loop for DF THI-PWM and ZVS THI-PWM

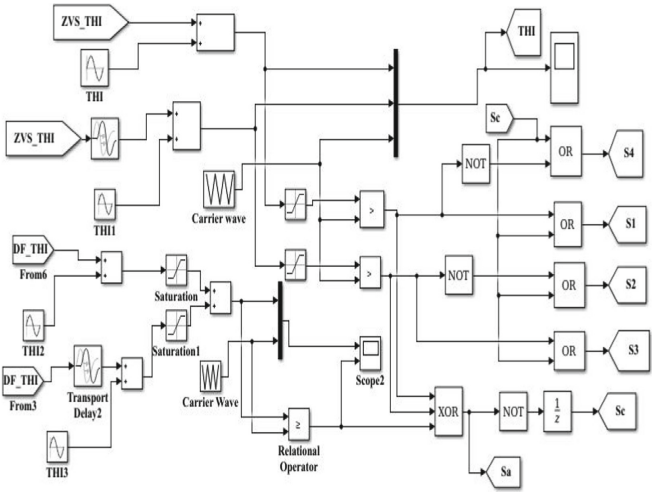

Fig. 13. Switching control scheme of DF THI-PWM and ZVS THI-PWM

The magnitude of output voltage can be known from the Fig. 16 as 243 V with the THD of 2.54%.

From the above closed-loop condition analysis, the DF THI-PWM is better compared to DF SPWM in-terms of voltage and THD (Table 3).

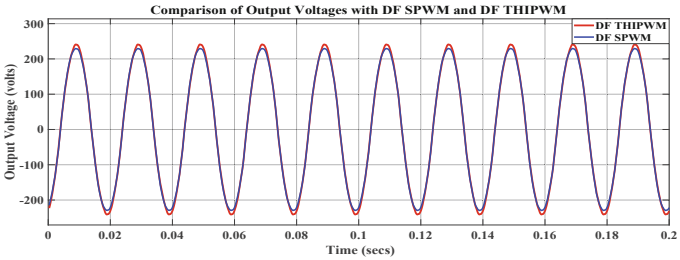

Fig. 14. Output Voltages with DF THI-PWM & DF SPWM with feed-back control loop.

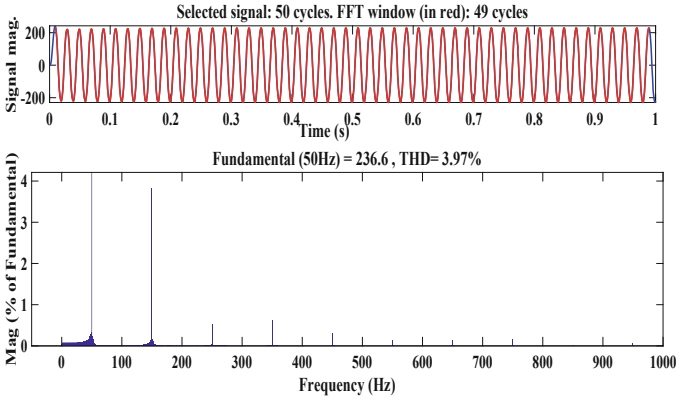

Fig. 15. FFT analysis with DF SPWM at closed-loop condition

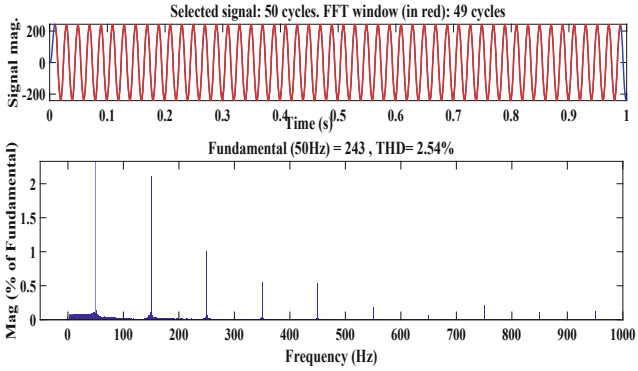

Fig. 16. FFT analysis with DF THI-PWM at closed-loop condition

Table 3. Comparison of DF SPWM & DF THI-PWM at closed-loop condition

PWM TYPE	Output voltage (v)	THD%
DF SPWM	236.6	3.87%
DF THI-PWM	243	2.54%

The results of the present circuit with DF SPWM and DF THI-PWM along short-circuit pulse at open-loop and closed-loop conditions is performed and is observed that the DF THI-PWM with closed loop condition has better voltage and THD performance.

8 Conclusion

The ZVS full-bridge inverter of single phase configuration with grid connected is implemented with ZVS THI and DF THI PWM strategy is proposed. In this, the ZVS operation of auxiliary switch and dc-ac converter switches is achieved with THI PWM and DF modulation scheme. By implementing this converter control scheme, the output voltage of the inverter is controlled and observed that the output voltage is more compared with the DF SPWM strategy and also the THD percentage of output voltage is less compared with DF SPWM. From the results it is observed that the proposed strategy requires low rated inductor in the filter, thereby reducing the cost of filters. Hence, it can be concluded that the proposed control scheme provides better voltage, reduction in switching losses and THD. This leads to reduced filter size which minimizes the filter cost.

References

1. Xue, Y., Chang, L., Kjaer, S.B., Bordonau, J., Shimizu, T.: Topologies of single-phase inverters for small distributed power generators: an overview. IEEE Trans. Power Electron. **19**(5), 1305–1314 (2004)
2. Divan, D.M.: The resonant DC link converter - a new concept in static power conversion. IEEE Trans. Ind. Appl. **25**(2), 317–325 (1989)
3. Divan, D.M., Skibinski, G.: Zero-switching-loss inverters for high power applications. IEEE Trans. Ind. Appl. **25**(4), 634–643 (1989)
4. Mezaroba, M., Martins, D.C., Barbi, I.: A ZVS PWM full-bridge inverter with active clamping technique using the reverse recovery energy of the diodes. In: Proceedings of the IEEE Industrial Electronics Society, pp. 621–626 (2002)
5. Gurunathan, R., Bhat, A.K.S.: Zero-voltage switching DC link single phase pulsewidth-modulated voltage source inverter. IEEE Trans. Power Electron. **22**(5), 1610–1618 (2007)
6. Chen, Y., Hu, G., Du, C., Chen, M., Xu, D.: A soft-switching full-bridge inverter with high efficiency. In: Proceedings of the IEEE Energy Conversion Congress and Exposition, pp. 2737–2744 (2013)
7. Hu, G., et al.: SiC full-bridge grid-tied inverter with ZVS-switching. In: Proceedings of the Energy Conversion Congress and Exposition, pp. 2773–2780 (2014)
8. Namboodiri, A., Wani, H.S.: Unipolar and bipolar PWM inverter. Int. J. Innov. Res. Sci. Technol. **1**(7), 237–243 (2014)

9. Nagasai, K.B., Jyothsna, T.R.: Harmonic analysis and application of PWM techniques for three phase inverter. Int. Res. J. Eng. Technol. **3**(7), 1228–1233 (2016)
10. Chen, Y., et al.: A ZVS grid-connected full-bridge inverter with a novel ZVS SPWM scheme. IEEE Trans. Power Electron. **31**(5), 3626–3638 (2016)