Optimized Hybrid Buck DC-DC Converter with QFT Controller

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Abstract. The present research work discuss about a hybrid DC-DC buck converter with QFT controller which is intended to reduce the power component voltage stress. The conventional buck converter with split switched inductor and cross connection of uni-direction switch results in Cross Inductor Hybrid dc-dc buck converter (CIHBDC). The capacitor electro static excitation and inductor electromagnetic response steady state values are obtained by theoretical steady state analysis. A closed loop feedback along with QFT controller design is also applied to enhance the performance. The dynamic PSIM experimentation and MATLAB simulation results are illustrated here for performance evaluation. A 100 W, 48 V supplied converter topology which outputs controlled 12 V is designed to portray the steady state analysis. Particle Swarm Optimization (PSO), Differential Evolution (DE) and hybrid algorithm of PSO and DE called PSODE approach is applied to optimize the components of the presented converter. Further the output control voltage as fitness function is evaluated with the considered optimization algorithms.

Keywords: Cross Inductor Hybrid DC-DC buck converter (CIHBDC) · QFT controller · step-down structure · experimental results · steady state analysis Particle Swarm Optimization and differential evolution (PSODE) Algorithm

Terminology

V_o	*Output Voltage*
V_{in}	*Input Voltage*
I_o	*Load current*
D	*Duty Cycle*
M	*Conversion Ratio*
QFT	*Quantitative Feedback Theory*

1 Introduction

The DC/DC converters are categorized into three classifications depending upon their applications. They are (1) voltage stabilization for Low-power electronic equipments, (2)

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medium-power applications as IC technology exciters and (3) high power applications such as power factor correctors. The active switch and its operation its duty cycle (D) deals conversion ratio (M) in basic DC-DC converters [1]. The output voltage (V_o) is varied by varying duty cycle in spite of dynamic changing load current (I_o) or input voltage (V_{in}).

Basic problem in these converter topologies are resulting in very large or very minute voltage conversion ratio (M). This will make the converter topology operate at extreme values of the duty cycle (D) i.e. ranging below 0.1 or above 0.9 in step down and step up converters respectively. Because of severe values of duty cycle the efficiency will be impaired and they enforce barriers for the transitory response [2]. Upon investigation studies researchers come up with methods like single switch series converter topologies [3], using pulse transformers, soft switching methods [4], ON/OFF operated inductor/capacitor topologies [5] were the some of the prominent techniques. Beginning from the switched-capacitor cells, ON/OFF inductor-capacitor topologies for better performance are developed and cited in [6]. A discussion on acquiring better conversion ratio is stated in a series studies mentioned in [7–9] and [10] just by embedding switching C- and L blocks.

The CIHBDC under different modes of operation of buck converter with parasitic consideration are explained in Sect. 2. State space analysis is explained in Sect. 3. QFT based control design is explained in Sect. 4. Simulation results are presented and clearly explained in Sect. 5.

2 CIHBDC Converter

The CIHBDC is a Cross inductor Hybrid DC-DC converter (Switched inductor DC-DC Buck Converter). Conversion ratio (M) of the CIHBD topology which purely depends on active switch (S) duty cycle of the DC-DC converter is D/1-D. The conversion ratio is purely depending on duty cycle of active switch. The DC-DC converter operating with minute value of duty cycle results in acquiring the main objective of very small conversion ratio has to compromise with poor efficiency and problems related to momentary response. The Cross-inductor DC-DC converter is used in order to nullify this problem.

2.1 Modes of Operation

The converter topology is shown below (Fig. 1):

For the CIHBDC there exist two operating modes of conduction under continuous conduction mode. The modes of operation are reported in Table 1 below in accordance with their operation.

Mode-I (Switch S-ON):

Mode-II (Diode D1, D2-ON):

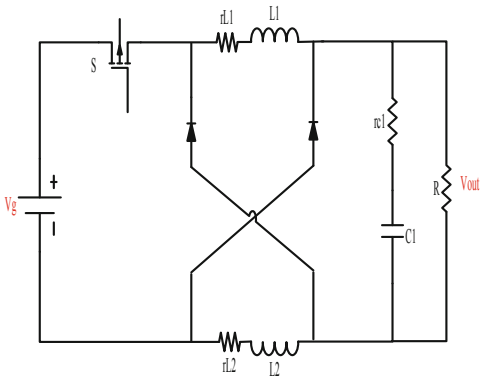

Fig. 1. Cross inductor Hybrid DC-DC converter topology.

Table 1. Charging and discharging region illustration.

Operation	**HBDC**	
	$0 < t < DT_s$	$DT_s < t < T_s$
Switches	S_1	-
Diodes	-	D_1 D_2

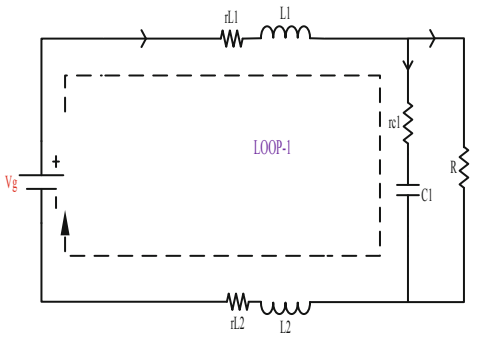

Fig. 2. Equivalent circuit during ON-time operation.

Applying the volt-second balance to the inductors the Voltage gain expression is obtained and compared with buck converter as shown in Fig. 4.

$$V_o = V_g\left(\frac{d}{2-d}\right) \tag{1}$$

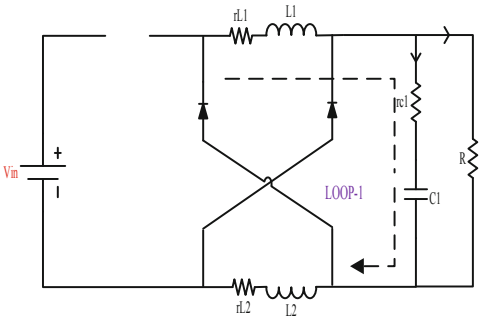

Fig. 3. Equivalent circuit during OFF-time operation.

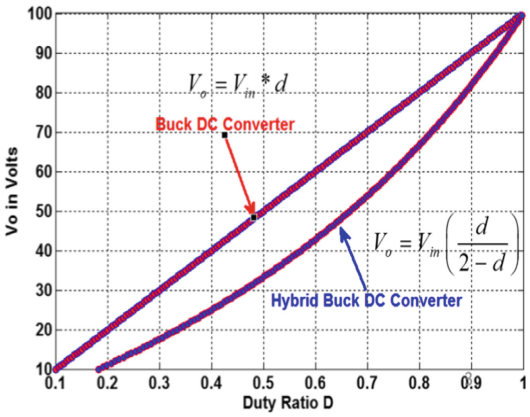

Fig. 4. Comparison of duty cycle variation between buck and Hybrid buck converter.

Upon performing the steady state analysis, the converter the state-space models of converter were formulated discussed in the subsequent section.

3 Dynamic Modeling

The high frequency operating requirements and applications of DC-DC converters in digital control and digital circuits is increasing day by day. This requires the steady state analysis and modeling of discrete-time DC-DC converters. This further enhanced the scope and increase in interest to design direct digital compensator.

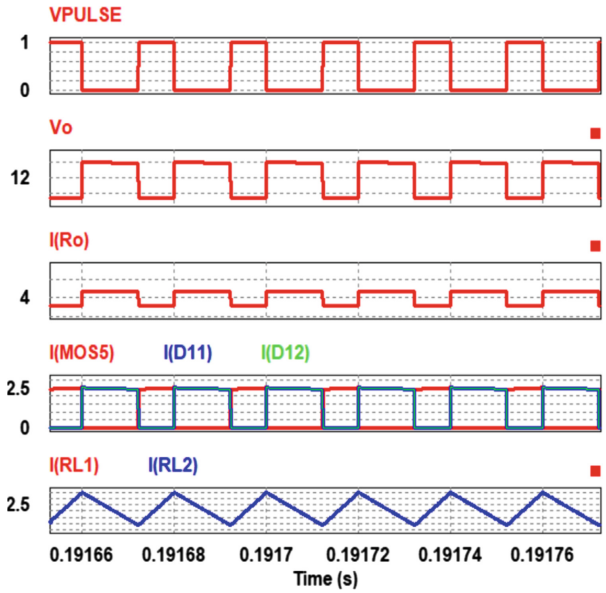

Fig. 5. Steady state voltages and currents a) PWM signal b) Output Voltage c) Load current d) Switch and Diode currents e) Inductor Currents.

From Fig. 2 we get the following equations:

$$\frac{di_{L1}}{dt} = \frac{1}{2L_1}\left(V_g - i_{L1}(R_{L1} + R_{L2} + K_1) - V_{C1}K_2\right) \tag{2}$$

$$\frac{di_{L2}}{dt} = \frac{1}{2L_2}\left(V_g - i_{L2}(R_{L1} + R_{L2} + K_1) - V_{C1}K_2\right) \tag{3}$$

$$\frac{dV_{C1}}{dt} = \frac{1}{C_1}\left(i_{L1}\left(1 - \frac{K_1}{R}\right) - V_{C1}\frac{K_2}{R}\right) \tag{4}$$

The matrix form of above three equations is:

$$A_1 = \begin{bmatrix} \frac{-(R_{L1}+R_{L2}+K_1)}{2L_1} & 0 & \frac{-K_2}{2L_1} \\ 0 & \frac{-(R_{L1}+R_{L2}+K_1)}{2L_2} & \frac{-K_2}{2L_2} \\ \frac{1}{C_1}\left(1 - \frac{K_1}{R}\right) & 0 & \frac{-K_2}{R*C_1} \end{bmatrix} B_1 = \begin{bmatrix} \frac{1}{2L_1} \\ \frac{1}{2L_2} \\ 0 \end{bmatrix} E_1 = \begin{bmatrix} K_1 & 0 & K_2 \end{bmatrix}$$

From Fig. 3 we get the following equations:

$$\frac{di_{L1}}{dt} = \frac{1}{L_1}(-(K_1 + R_{L1})i_{L1} - V_{C1}K_2) \tag{5}$$

$$\frac{di_{L2}}{dt} = \frac{1}{L_2}(-(K_1 + R_{L1})i_{L2} - V_{C1}K_2) \tag{6}$$

$$\frac{dV_{C1}}{dt} = \frac{1}{C_1}\left(i_{L1}\left(1 - \frac{K_1}{R}\right) - V_{C1}\frac{K_2}{R}\right) \tag{7}$$

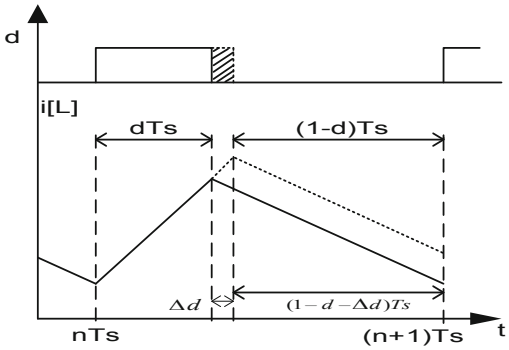

Fig. 6. Trailing and leading edge modulation schemes.

The matrix form of above three equations is:

$$A_2 = \begin{bmatrix} \frac{-(R_{L1}+K_1)}{L_1} & 0 & \frac{-K_2}{L_1} \\ 0 & \frac{-(R_{L2}+K_1)}{L_2} & \frac{-K_2}{L_2} \\ \frac{1}{C_1}\left(1-\frac{K_1}{R}\right) & 0 & \frac{-K_2}{R*C_1} \end{bmatrix} B_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} E_2 = \begin{bmatrix} K_1 \; 0 \; K_2 \end{bmatrix} \tag{8}$$

The discrete time small-signal (DTSS) model is given by:

$$\hat{x}[n] = \phi\hat{x}[n-1] + \gamma\hat{d}[n-1] \tag{9}$$

Generally the trailing-edge and leading-edge PWM schemes are used in the HBDC converters. But an OFF-time sampling based trailing-edge PWM is used in CIHBDC which is as illustrated in Fig. 8. The implementation of such topology and its mathematical investigation is specified in [1]. The CIHBDC topology of its kind is a single-input single output (SISO) system, meant to target better voltage regulation. The design procedure of such converter control design is done through the following mathematical model:

$$[\dot{X}] = [A_i][X] + [M_i][I_z] \tag{10}$$

$$[Y] = [E_i][X] + [J_i][I_z] \tag{11}$$

Usually the DC-DC converters design of this kind suffers with structured or unstructured uncertainties. A strong controller design with noise rejection and dynamic start up response features is very much required. This in-turn has to suck out the noise of switching and stabilize the system.

4 QFT Based Controller Design

As per the order of the day a dynamically energy varying PV systems need dynamically challenging and storage operated systems. The same phenomenon happens with varying loads in the DC-DC distribution utility system. These are termed as uncertainties which might worsen the operation of the system. Such uncertainties are often seen even in DC-DC Converter topologies relating to source and load variations, these are referred to as destabilizing effects. To overcome such uncertainties a design of apt controller is very much required. The QFT is one of the solutions to address this problem towards detection and aligning the cooperation between performance specifications and parameter uncertainties. The QFT is a like a two degree freedom control problem. Here the feedback controller is meant to address the disturbances and feed forward controller to deal the plant uncertainties. The QFT controller block by block schematic for current mode control, voltage mode control and load disturbance rejection is illustrated in Fig. 5, for voltage and current mode control loops and output disturbances. QFT controller monitors and governs the startup response and disturbance rejection response communicating the main plant.

The following expressions were considered for developing controller design (Table 2).

The group bounds of CIHBDC are shown in Fig. 6. The loop shaping phenomenon with the Controller design is illustrated in Fig. 7. The bode stability analyzed controller framing loop gain, complementary Sensitivity and Sensitivity is shown in Fig. 8 (Figs. 9 and 10).

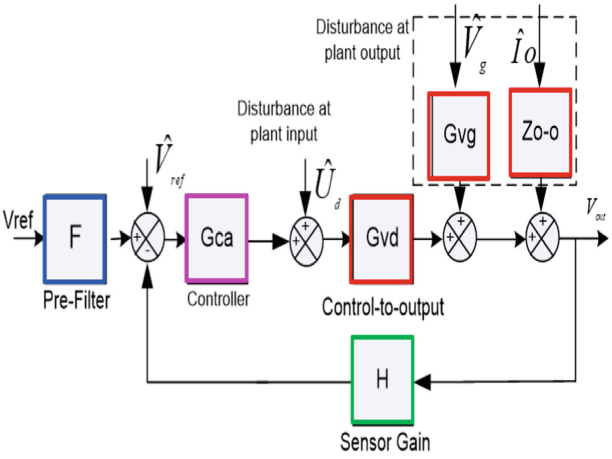

Fig. 7. CIHBDC with QFT control mechanism.

Table 2. DTSS model transfer function/s (TF).

Control-to-output TF: $G_{id}(z)$	$\frac{\hat{i}_{L_2}(z)}{\hat{d}(z)} = [\eta^{'}(zI-\phi)^{-1}\gamma]$
Source-to-output TF: $G_{ig}(z)$	$\frac{\hat{i}_{L_2}(z)}{\hat{v}_g(z)} = [\eta^{'}(zI-\phi)^{-1}\gamma + F^{'}]$
Load current-to-output TF: $G_{io}(z)$	$\frac{\hat{i}_{L_2}(z)}{\hat{i}_o(z)} = [\eta^{'}(zI-\phi)^{-1}\gamma + J^{'}]$

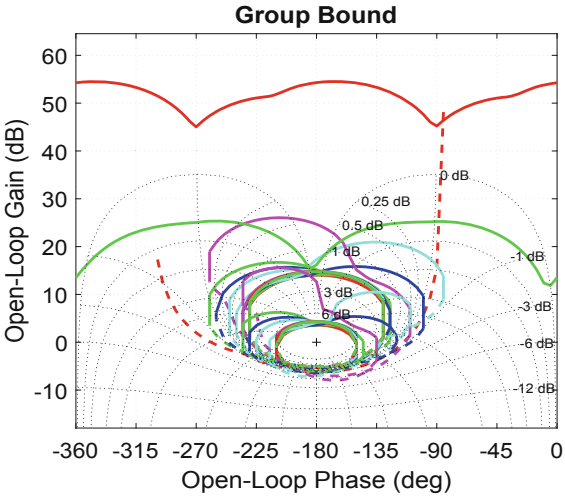

Fig. 8. The group bounds of CIHBDC.

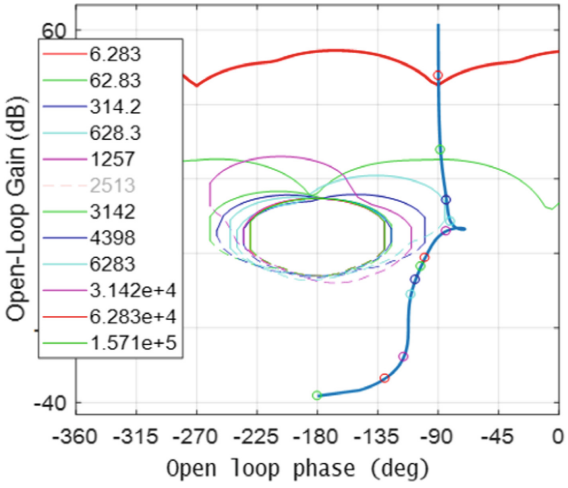

Fig. 9. Controller design using Loop Shaping.

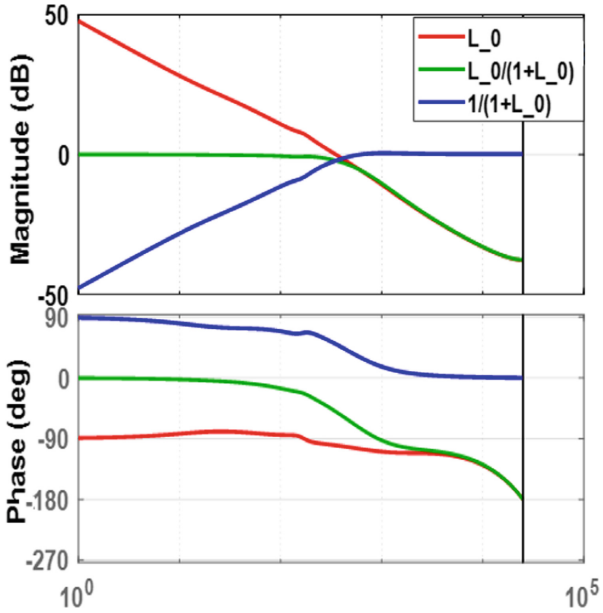

Fig. 10. Illustration of controller framing loop gain, complementary sensitivity and sensitivity with Bode stability criterion.

The controller was designed using QFT in discrete mode and is given in Eq. 12.

$$G_{c\_d} = \frac{0.3(z - 0.92)(z - 0.907)}{(z - 1)(z - 0.8)} \tag{12}$$

The following session discusses the optimization of inductors and capacitors.

Upon designing of controller the optimization is applied to identify appropriate inductors and capacitors with swarm birds inspired PSO Algorithm [11], Darwin's theory inspired DE Algorithm [12] and hybrid PSO & DE algorithm called PSODE algorithm [13]. The flow chart of the hybrid PSODE algorithm is as follows (Fig. 11):

The results are shown in Fig. 12 and the comparison is shown in Table 3 (Figs. 13 and 14).

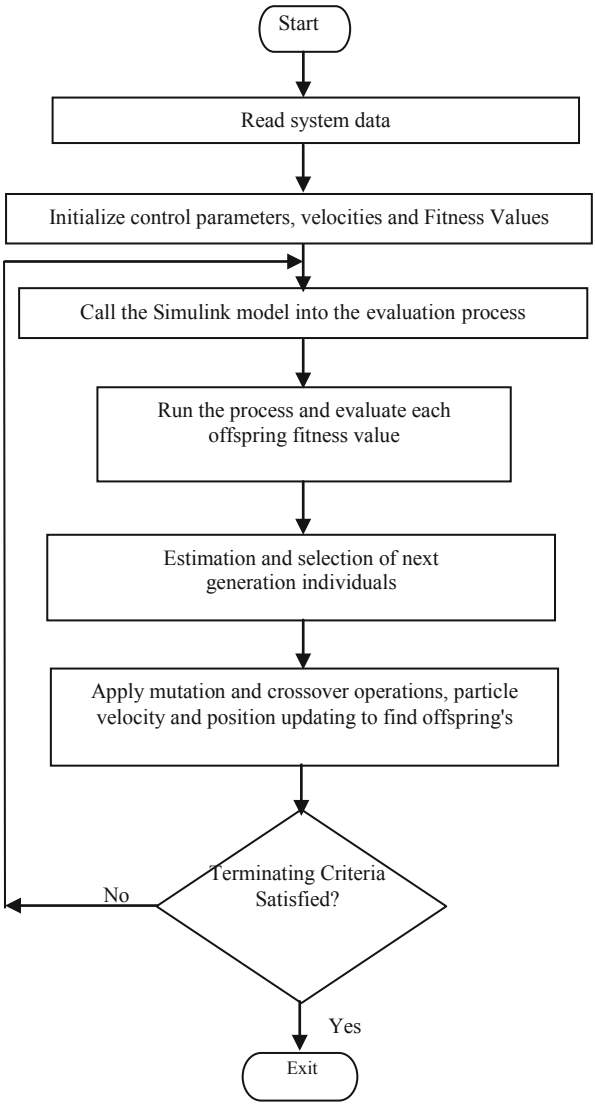

Fig. 11. PSODE scheme flow chart illustrating PSO & DE.

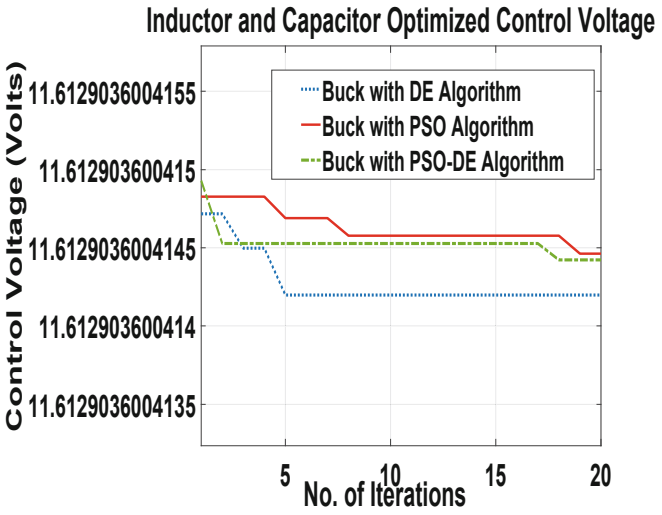

Fig. 12. Inductor and capacitor optimized control voltage.

Table 3. Comparison of parameters with different algorithms

	Inductance (μH)	Capacitance (μF)	Control Voltage (V)	Time of optimization (s)
PSO	1267.5	1023.015	11.612903600414198	100.435
DE	457.51	49.606	11.612903600414462	93.5060
PSODE	508.07	488.73	11.612903600414423	102.54

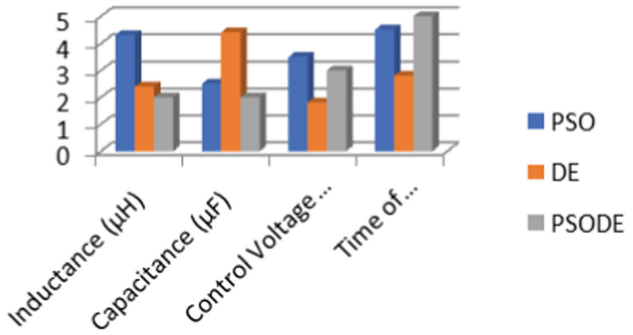

Fig. 13. Optimization comparison illustration of CIHBDC.

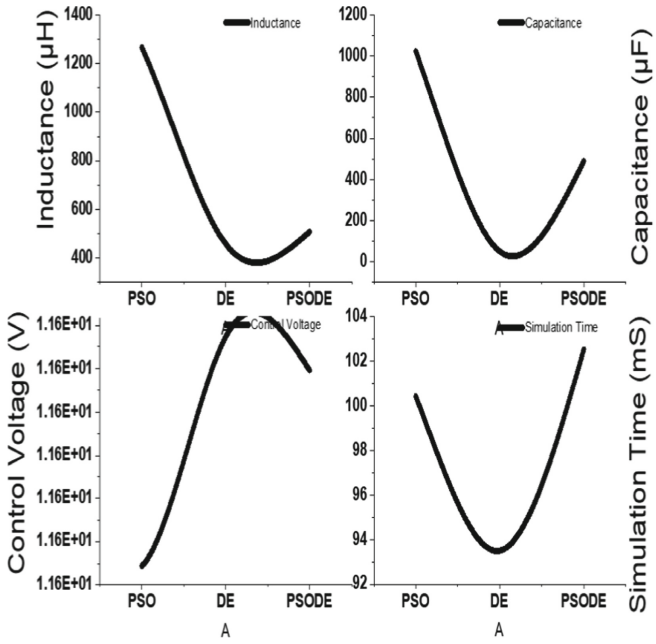

Fig. 14. Performance comparison of PSO, DE, PSO-DE.

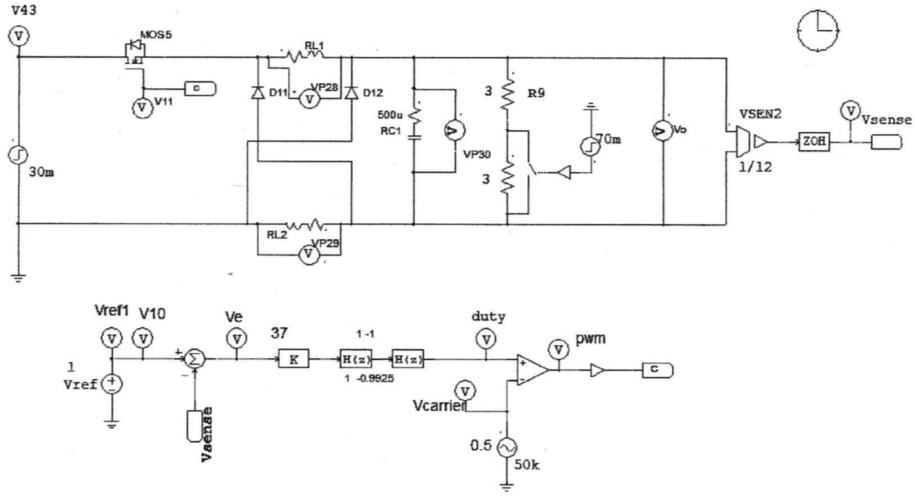

Fig. 15. Closed loop controller of CIHBDC.

5 Topology Simulation

The CIHBDC model is simulated and the output waveforms are verified with source disturbance and load disturbance to analyze the performance of the controller (Fig. 15).

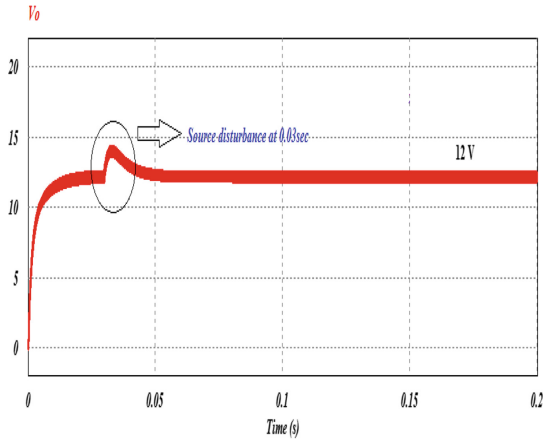

Fig. 16. Output voltage with source disturbance.

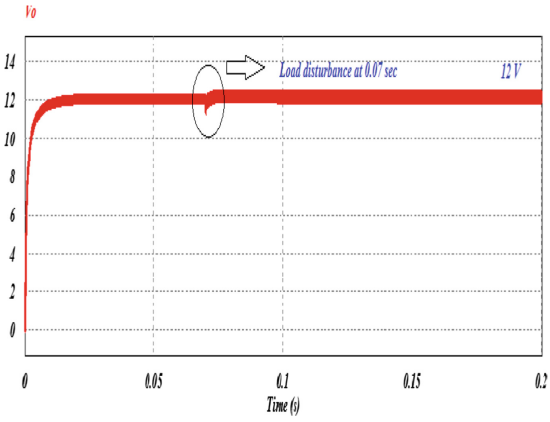

Fig. 17. Output voltage with load disturbance.

The designed and developed plant is analyzed and the simulation results for the load output voltage with source disturbance and load disturbance are obtained as shown below in Fig. 16 and Fig. 17.

6 Conclusion

The steady state analysis of the proposed CIHBDC is performed, the results of its kind illustrates and recommends the excessive bucking operation. The group bounds and loop shaping is carried out with effective QFT based robust controller. The converter topology parameters are further optimized with PSO, DE and PSODE algorithms. The results show the efficacy of the disseminated algorithms. The converter dynamic simulation and the optimization control voltage evaluations are presented and the regulation of the voltage

is achieved. The dynamic simulations are carried out in PSIM and optimization is carried out in MATLAB environments.

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