Research of Highly Reliable Drive and Control Technology Based on APSOC

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Abstract. With the development of industrial field, the requirements of miniaturization, high integration, strong computing performance and high reliability are put forward for servo controlers. The traditional control platform has some problems, such as complex system and small promotion space. Therefore, the research on PMSM high reliability control technology based on APSOC is proposed, and the customized IP core is developed and applied as the servo control parallel coprocessor. The overall scheme of the servo system is introduced, the corresponding software and hardware design and control strategy research are realized, the drive control system of permanent magnet synchronous motor is built and verified, and the hardware area is reduced by 50%, It also realizes the stable operation of the servo mechanism and the accurate control of PMSM, which provides a new generation of general technology platform for the efficient, high-precision and reliable control of servo control.

Keywords: APSOC · PMSM · High reliability · Control and drive

1 Introduction

At present, most servo control and drive systems use DSP and arm as the control platform. However, with the development of aerospace and aerospace fields, the control driver is required to be miniaturized, intelligent, highly reliable, multi axis synchronous control and so on [1]. The high integration apsoc chip Zynq has strong computing power and rich functions, which provides a new idea for PMSM drive control [2]. Zynq incorporates a dual core arm Cortex-A9 processor with a dominant frequency of 667 MHz. Compared with the 80–100 M dominant frequency of ordinary MCU, ARM chip has stronger computing power. Moreover, FPGA uses programmable logic to realize parallel processing, and the interface development is flexible. FPGA and arm complement each other to jointly improve the high reliability and high precision control of the motor [3, 4].

2 Hardware Design Based on APSOC

This paper uses Zynq-7000 series chip XC7020-CLG484 as the core of integrated drive control, proposes a fully programmable system on chip servo control architecture, and

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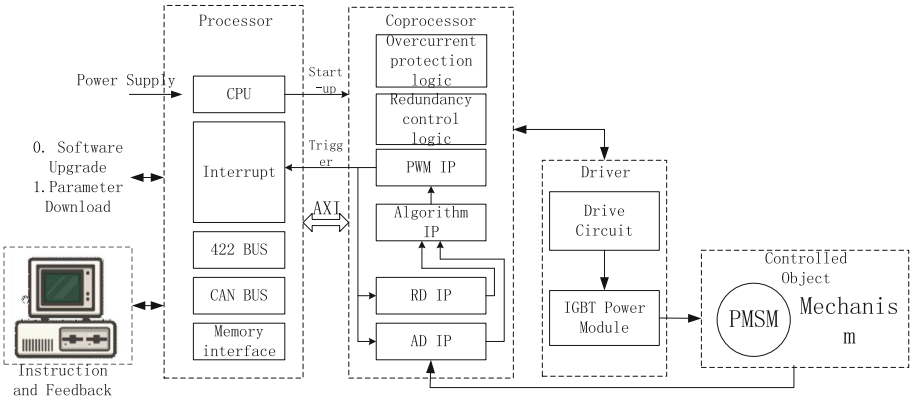

Fig. 1. Servo Control Drive Integrated Architecture

develops a servo control coprocessor with multiple IP cores such as AD acquisition, rotary transformer acquisition, PWM control, overcurrent protection, and integrates them into a current loop and SVPWM control algorithm IP core, which gives full play to the PL side parallelism advantage of zynq and better completes the drive control of servo mechanism, The main frequency is increased from 120 m to 667 M, which not only improves the real-time performance of the system, but also reduces the volume of the controller, and solves the problems of low integration of the existing control architecture, serial control, slow operation speed and so on [5, 6].

The hardware principle of the control and drive platform is shown in Fig. 1, which mainly includes the controller and driver. The controller is mainly composed of zynq7020 minimum system, secondary power conversion circuit, 422 communication circuit, CAN communication circuit, memory interface circuit, LVDT processing circuit, rotary transformer regulating circuit, temperature sampling circuit, solenoid valve control circuit, etc., Zynq7020 integrates a processor (PS) and a large-scale programmable logic resource (PL) system. The driver is mainly composed of drive circuit, IGBT power module, bus voltage acquisition circuit, phase current acquisition circuit, etc., and finally realizes the position control of permanent magnet synchronous motor and servo mechanism.

3 ZYNQ System Software Design

3.1 Software Startup Process

The starting process of zynq7020 is Arm (PS) first, and then it is determined to start from QSPI Flash by reading registers, and then the bit file of FPGA is loaded through the software part of arm system.bit to FPGA (PL), start the logic function of FPGA, copy the program from QSPI flash to DDR3 and start to execute the program. The startup process is shown in Fig. 2.

3.2 Self Customized IP Core

According to the principle block diagram of the control drive system, the software of the system is divided into Arm and FPGA according to the function and performance

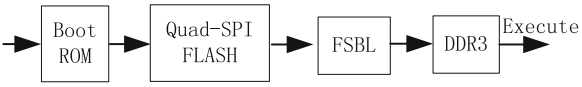

Fig. 2. Zynq Startup Process

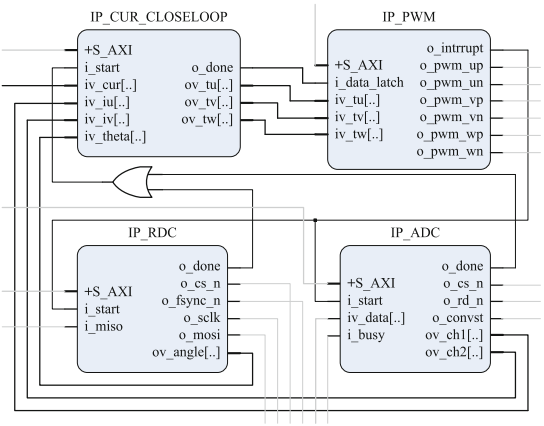

Fig. 3. Hardware IP Core Algorithm Diagram

Table 1. Resource Allocation

IP Name	Function	Clock Distribution
Algorithm IP	SVPWM algorithm and current closed loop	100M
AD sampling IP	External ad7606 analog-to-digital conversion	50M
RD IP acquisition IP	Ad2s1210 rotary transformer reading	50M
PWM module IP	Timed interrupt	100M
Overcurrent protection	Overcurrent protection	100M

requirements. The Arm end is mainly to realize the speed loop and position loop algorithm of the servo mechanism, and the FPGA end is mainly to realize the current loop and space vector algorithm of the servo mechanism.

As shown in Fig. 3, under the vivado 2018.3 platform, a variety of IP cores such as current loop and SVPWM, analog acquisition, rotary transformer acquisition, PWM control, overcurrent protection, etc. have been developed to form a parallel coprocessor. Table 1 shows the clock allocation and functions of self customized IP cores.

Questa Sim simulation is carried out for the current loop and SVPWM algorithm, and the IP core motor control algorithm is verified. The simulation is shown in Fig. 4, and the timing and data comply with PMSM control logic [7, 8].

Establish servo PMSM control engineering files in vivado, and allocate FPGA pins according to the hardware platform. After compilation, according to statistics, the overall

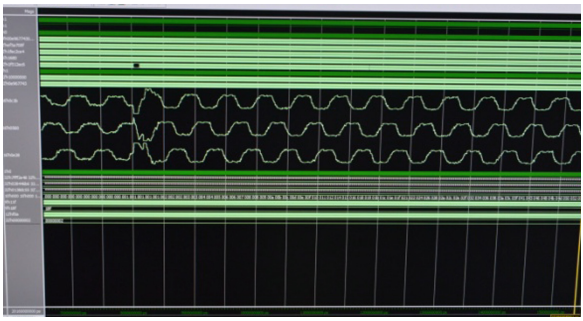

Fig. 4. SVPWM and Current Loop Simulation Waveform

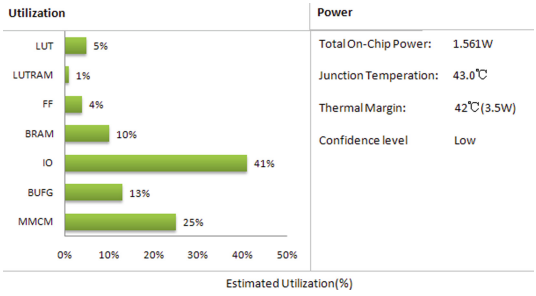

Fig. 5. Hardware Resource Occupancy

hardware resources occupy about 5%, of which DSP and Bram resources are mainly used for current loop matrix multiplication. The overall power consumption of the system on chip is about 1.561w, and the chip surface temperature is about 43 °C. The occupation of hardware resources is shown in Fig. 5.

3.3 Data Communication

The communication mode of PL and PS end is interrupt signal, EMI interface and Axi GP bus. The arm of PL end and FPGA work together through high-speed axi4 Lite bus. The interrupt signal is to trigger closed-loop interrupt for PS end and PL regularly and enter the interrupt program. The Emio interface realizes the transmission of control signals. Axi4 Lite bus has four interfaces: general interface Axi_GP, high-speed transmission interface Axi_HP, accelerated consistency interface Axi_GCP and DMA, according to different communication rate requirements, select the corresponding communication interface.

There are three types of data communication between arm and FPGA in this paper. The first one is servo control program, displacement and speed instructions and parameters. PC completes PMSM performance parameter download through CAN bus, and Parameters are stored in the internal E2PROM; It is upgraded to flash of arm through CAN bus software, and then the arm side accesses FPGA to modify the corresponding

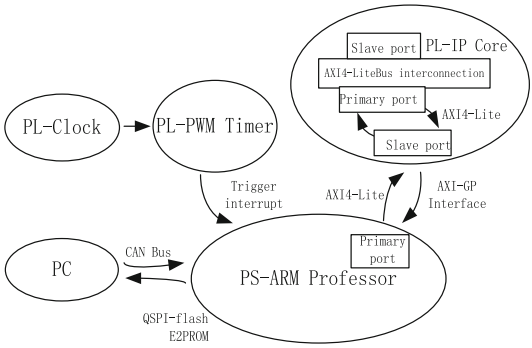

Fig. 6. Internal Communication Scheme

registers; The second is some special registers of FPGA. Arm obtains the current running state of FPGA by checking these special registers; The third is FPGA operation data. Users need to monitor these operation status variables in real time. The first and the second require low data transmission rate, so the communication common interface between PL and PS Axi_GP can meet [9]. See Fig. 6 for details.

4 Research on Control Driven Strategy

4.1 Running Sequence

The system operation sequence is mainly executed in PS and PL. The algorithm and calculation process at PL end of servo control sequence are executed in parallel; During the operation of the servo mechanism, in order to avoid the switch timing error caused by the simultaneous power on of the control power and the power power, the startup judgment of the servo motor is added in the software to avoid the error caused by the accumulation of the closed-loop integral of the power on.

Transplanting the current loop, overcurrent protection and space vector algorithm with large amount of code from the traditional arm end to the FPGA end can not only customize the switching frequency, but also greatly reduce the operation execution time of the system software. After calculation and statistics, under the working condition of 10 K interrupt frequency, the closed-loop execution time of apsoc platform is reduced from 40 μs to 20 μs; Since the platform is used for ultra-high speed motor control, in order to improve the speed and accuracy of PMSM control, the switching frequency is increased from 10 K to 15 K, the phase current is reduced from 80 A to 42 A under the same working condition and load, and the motor speed is increased from 17000 rpm to 20000 rpm, as shown in Table 2.

4.2 Closed Loop Control Strategy

Figure 7 is the closed-loop control block diagram of the system. The servo system collects LVDT position sensor information, which is voted by the software displacement voting algorithm, enters the system position loop after first-order filtering, and then is used

Table 2. Motor performance comparison table

Switching Frequency	Saturation Speed	Phase Current Peak
10 k	17000 rpm	80 A
12 k	18500 rpm	60 A
15 k	20000 rpm	42 A

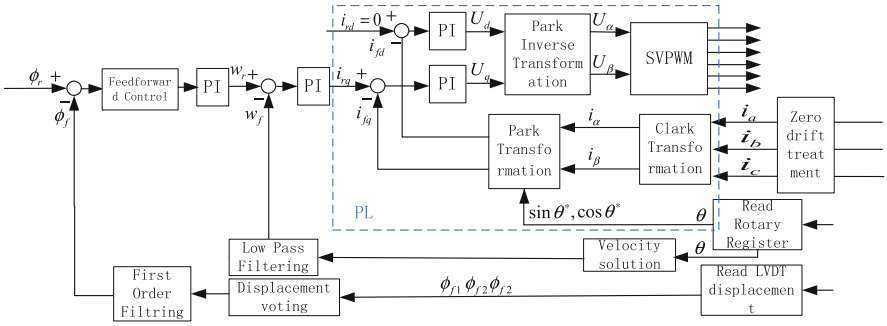

Fig. 7. Closed Loop Control Algorithm

as the command input of the speed closed-loop of the permanent magnet synchronous motor after feedforward control and PI limiting control. The actual speed of the motor is calculated by the position information collected by the rotary demodulation circuit as the feedback of the speed closed-loop; The output of the speed closed-loop is used as the input of the d-q axis vector control. After the phase current is sampled by the Hall current sensor and processed with zero drift, it enters the current closed-loop algorithm to participate in the operation. Finally, the PWM chopper signal with adjustable frequency and complementary dead zone is output to control the normal operation of power drive and IGBT module, so as to realize the control of servo mechanism [10].

In the motl, because the displacement feedback adopts the way of converting ad into digital quantity, the low-pass filter is used to filter the introduced interference [11–13]. The discrete and iterative method is used in the software to realize this process, and the realization formula is

$$Y(n) = a * X(n) + (1 - a)Y(n - 1) \tag{1}$$

5 System Test

According to the test requirements, the test platform is built, and vivado 2018.3 and SDK are used to realize the code development and debugging. The tester sends sinusoidal displacement command ± 6 to the control driver through the CAN bus, and the frequency is 0.02 Hz. As shown in Fig. 8, the control driver drives the servo mechanism to realize

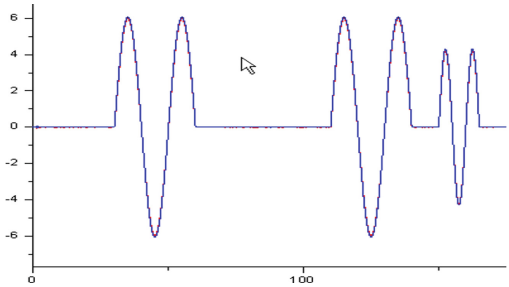

Fig. 8. Mechanism displacement sine curve tracking

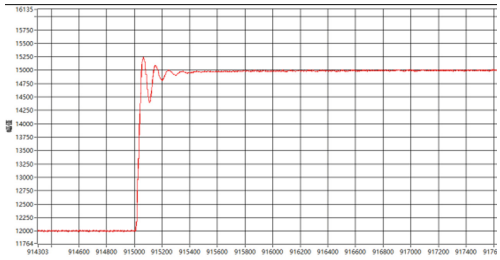

Fig. 9. 15 Mpa–15000 rpm Speed following

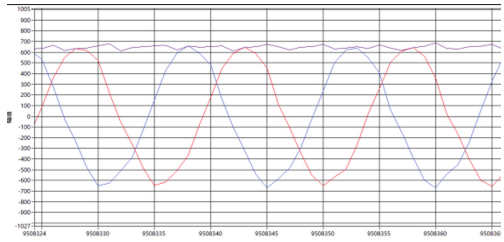

Fig. 10. 18 Mpa–10000 rpm Current loop curve

sinusoidal displacement stable tracking and trajectory control. As shown in Fig. 9, the given speed of 15000 rpm, 4.0 N·m under the rated load, the motor speed command tracking situation. Under the rated load of 4.0 N·m and the rotating speed of 10000 rpm, the UV phase current and q-axis current waveforms are shown in Fig. 10. Through the test verification, the mechanism and motor run smoothly, the control accuracy is high, the current waveform is smooth, the torque ripple is small, the control drive efficiency and reliability are greatly improved, and the ultra-high speed control of PMSM is also realized to meet the use needs.

6 Conclusion

In this paper, the control research of permanent magnet synchronous motor and servo mechanism based on apsoc makes full use of the platform advantage of logic zynq to improve the operation speed of the system and the control performance of the motor. Make full use of the resources of the system, reduce the volume of the control platform, reduce the design cost, and realize the high reliable control of PMSM.

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