Research on Improved Resolver-to-Digital Conversion Method and Its Application Based on FPGA

Qijia Zheng[1,2(✉)], Shuping Meng[1,2], Sixian Sun[1,2], Yang Jiang[1,2], and Yang Hu[1,2]

[1] Beijing Institute of Precision Mechatronics and Controls, Beijing, China
qijia_zheng@163.com
[2] Laboratory of Aerospace Servo Actuation and Transmission, Beijing, China

Abstract. According to the demand of high integration of servo motor control system, a method of resolver-to-digital conversion (RDC) based on FPGA is proposed. This method adopts the technology of synchronous excitation and peak sampling, which can realize the peak sampling of sine signal and cosine signal of resolver through low-speed and high-precision ADC. The method realizes high-precision angle-to-digital conversion by CORDIC algorithm and closed-loop tracking algorithm. Based on the principle of this method, a improved servo motor controller is developed and applied to the servo system. The comparison test between the improved servo motor controller and the traditional controller is carried out. The test results show that the resolver-to-digital conversion method is correct and feasible. The improved controller developed based on this method has normal function and better dynamic characteristics.

Keywords: RDC · Servo · Motor Control · FPGA

1 Introduction

The resolver is used for coaxial installation with the motor to obtain the rotor angle. Compared with photoelectric encoder, magnetic encoder and other sensors, resolver has the advantages of high mechanical installation strength and strong environmental adaptability. Therefore, resolvers are widely used in aerospace, aviation, weapons, ships and other fields. The resolver-to-digital converter converts the resolver signal into shaft angle digital signal for servo motor control or robot control [1].

The traditional resolver-to-digital conversion usually uses the conversion chip to complete the resolver decoding [2]. This method has the advantages of simple circuit and high conversion accuracy. However, a single chip can only complete one channel axis angle digital conversion. For the synchronous control demand of multi-channel servo motor, it can only be solved by increasing the number of chips, which cannot meet highly integrated design requirements. It is urgent to study the extendable multi-channel synchronous resolver-to-digital conversion technology.

Reference [3] and reference [4] have studied the method of square wave excitation of the resolver based on FPGA, and considered the frequency characteristics caused

L. Yan and J. Na (Eds.): ICFPMCE 2022, AHE 10, pp. 25–35, 2023.
https://doi.org/10.2991/978-94-6463-022-0_4

by square wave excitation. Reference [5] has studied using phase-locked loop (PLL) tracking algorithm to complete resolver-to-digital conversion. This method is realized by DSP and its excitation signal is obtained from PWM module of the DSP. The research on the sampling of the rotation signal is basically realized by the principle of oversampling the sine and cosine feedback signals with high sampling rate ADC [6].

In this paper, a conversion method of resolver-to-digital based on FGPA is proposed. Through synchronous excitation peak sampling technology, a low-speed high-precision ADC can be used to realize the peak sampling of sine and cosine feedback signal, and a high-precision digital conversion of resolver is realized through CORDIC algorithm and closed-loop tracking algorithm. Based on the principle of this method, a improved servo motor controller is developed and applied to the servo system. The test data results show that the improved controller based on this method has better dynamic characteristics compared with the traditional servo motor controller.

2 Methodology

2.1 Resolver and Its Principle

The composition of the resolver is shown in Fig. 1.

By applying the excitation signal U_R with frequency f_R and amplitude E at the input terminals $R+$, $R-$, the feedback signals U_{SIN} and U_{COS} with the same frequency as the excitation signal are obtained at the sine and cosine output terminals respectively. The relationship between feedback signals and resolver shaft angle φ is:

$$\begin{aligned} U_R &= E \times \sin\theta \\ U_{\sin} &= E \times k \times \sin\phi \sin\theta \\ U_{\cos} &= E \times k \times \cos\phi \sin\theta \end{aligned} \tag{1}$$

The traditional resolver-to-digital conversion method is based on the integrated chip to demodulate the resolver signals. This circuit includes detector, multiplier, integral circuit and low-pass filter circuit, which leads to the lag of shaft angle detection, affects the motor control accuracy, and is not easy to expand the multi-channel synchronization [7, 8].

The conversion method in this paper adopts synchronous excitation peak sampling and digital demodulation based on FPGA, it has the advantages of fast conversion speed, high precision and high system integration.

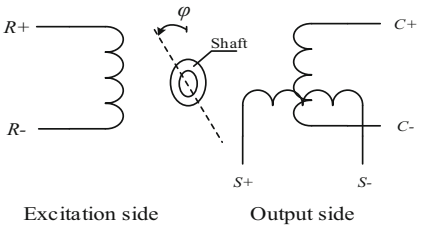

Fig. 1. Composition of resolver

2.2 Synchronous Excitation Peak Sampling

The output signal of the resolver is an AC signal, which can be regarded as a modulated sinusoidal wave formed by rotor angle information. The modulation method is amplitude modulation. Therefore, it is necessary to demodulate the sine and cosine modulated waves output by the resolver to obtain U_{SIN} and U_{COS} signals.

2.2.1 Generation of Excitation Wave

The optimal working frequency of the resolver used in this paper is 10 kHz, so the excitation wave frequency is selected as 10 kHz. Using the look-up table method, the 10 kHz sine wave excitation signal is modulated to 1 MHz square wave carrier in FPGA to generate the excitation signal SPWM modulation wave.

Using the second-order analog low-pass filter, the cut-off frequency is selected as 20 kHz, the 1 MHz carrier signal of the SPWM modulation wave of the excitation signal is suppressed, and the 10 kHz sine wave excitation signal is restored as the input of the resolver.

2.2.2 Peak Sampling

The principle of synchronous excitation peak sampling is shown in Fig. 2.

Since the resolver can be regarded as amplitude modulation, the output signal and excitation signal always keep phase synchronization. The excitation signal of the resolver and the ADC sampling convert signal are synchronously triggered by the 10 kHz timer flag inside the FPGA, and the phase lag caused by the analog low-pass filter and the line parasitic capacitance is compensated by the phase compensator, so that the sampling time of the AD conversion is the same as the peak value of the resolver. The timing chart of synchronous peak sampling is shown in Fig. 3.

The synchronous excitation peak sampling method not only simplifies the peak sampling circuit and improves the amplitude detection speed, but also avoids the motor PWM chopping time and reduces the sampling noise by adjusting the compensation value of the phase compensator.

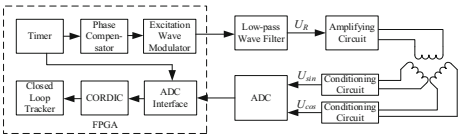

Fig. 2. Schematic block diagram of synchronous excitation peak sampling

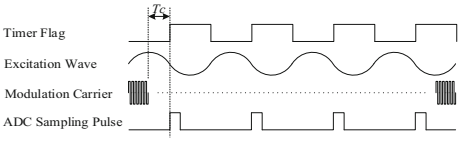

Fig. 3. Timing chart of synchronous excitation peak sampling

2.3 CORDIC Algorithm

CORDIC algorithm can calculate trigonometric function and inverse trigonometric function. The open-loop method to calculate the rotor angle is using U_{SIN} and U_{COS} signals to obtain the shaft angle φ through the Eq. (2).

$$\phi = \arctan\left(\frac{U_{SIN}}{U_{COS}}\right) \tag{2}$$

The table lookup method can be used to realize arctangent operation in digital system. However, with the improvement of accuracy, the table lookup method consumes a lot of system resources, especially for multi-input and output systems. CORDIC algorithm solves the contradiction between system resources and operation accuracy, and can use less system resources to realize trigonometric function operation and inverse trigonometric function operation [9, 10].

The basic principle of CORDIC algorithm is the Eq. (3), namely plane rotation equation of Cartesian coordinate system.

$$\begin{bmatrix} x_2 \\ y_2 \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} x_1 \\ y_1 \end{bmatrix} \tag{3}$$

Equation (3) divides by $cos\theta$ to get the pseudo rotation equation shown in Eq. (4).

$$\begin{aligned} \frac{\hat{x}_2}{\cos\theta} &= x_1 - y_1 \tan\theta \\ \frac{\hat{y}_2}{\cos\theta} &= y_1 + x_1 \tan\theta \end{aligned} \tag{4}$$

In Eq. (4), let $tan\theta$ be 2^{-i} to get the iterative equation shown in Eq. (5).

$$\begin{aligned} \frac{\hat{x}_{i+1}}{k} &= x_i - d_i y_i 2^{-i} \\ \frac{\hat{y}_{i+1}}{k} &= y_i + d_i x_i 2^{-i} \\ \hat{z}_{i+1} &= z_i + d_i \theta_i \\ k &= \frac{1}{\prod_1^i \cos\theta_i} \end{aligned} \tag{5}$$

In Eq. (5), d_i is the direction operator. When the rotation direction is counterclockwise, d_i is 1, and on the otherwise, d_i is -1; k is the scaling factor.

After 16 iterations, the scaling factor k can be considered as a constant 0.60725. Therefore, $cos\theta$ may not be considered in iterative operation, instead, multiply the result by the scaling factor k. In practice, the 2^{-i} operation can be equivalent to the right arithmetic shift, and the accumulation of z_i can use the look-up table method.

Set initial angle θ is 0, x_1 is the cosine value, y_1 is the sine value, and the sign of direction operator d_i is opposite to that of z_i. After 16 iterations, z_{16} is the arctangent calculation result.

The maximum angle range that can be calculated by 16 iterations is $-99.88°$ to $99.88°$, that is, CORDIC algorithm can realize the calculation of trigonometric function and inverse trigonometric function in one and four quadrants. For the calculation from

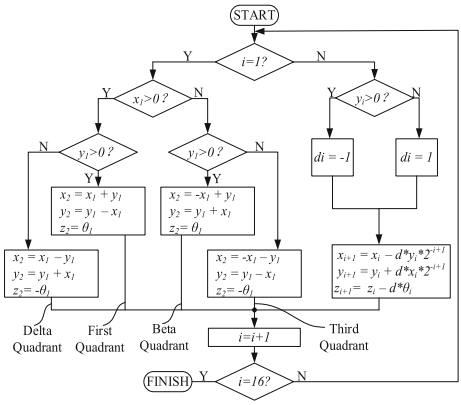

Fig. 4. Extended open-loop CORDIC algorithm flow chart

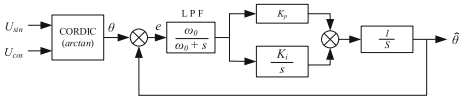

Fig. 5. Block diagram of improved closed-loop tracking algorithm

−180° to 180°, the CORDIC algorithm needs to be extended to the second and third quadrants.

The quadrant of arctangent operation of CORDIC algorithm is extended by using the iterative algorithm flow in Fig. 4.

2.4 Closed-Loop Tracking Algorithm

The method using CORDIC to calculate the arctangent shaft angle φ is an open-loop calculation method, which is easy to receive noise interference, resulting in wrong output results. Closed-loop tracking algorithm can improve this problem.

The improved closed-loop tracking algorithm first performs CORDIC arctangent operation on the input signals of U_{SIN} and U_{COS}, and inputs the operation results to the closed-loop tracking link composed of low-pass filter, PI controller and integrator. The structure block diagram of the improved closed-loop tracking algorithm is shown in Fig. 5.

3 Simulation Analysis

3.1 Open-Loop CORDIC Simulation

The open-loop method uses CORDIC algorithm to directly perform the arctangent operation to obtain the angle output. Simulation software is used to verify the output results of the open-loop algorithm. The input signal range of U_{SIN} and U_{COS} is −200–200 mV, and the angle output result is −180–180°. The relationship between the angle result and

Table 1. SNR of three algorithms

SNR/db	Open-loop algorithm	Traditional closed-loop algorithm	Improved closed-loop algorithm
Group 1	28.7	35.5	35.7
Group 2	27.7	34.2	33.8
Group 3	28.2	34.7	34.6

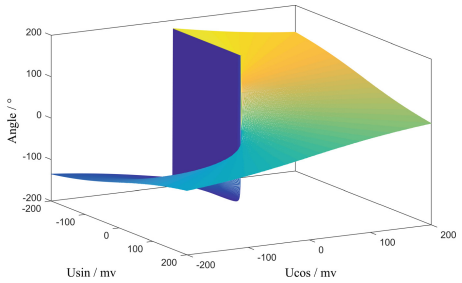

Fig. 6. Simulation results of open-loop algorithm

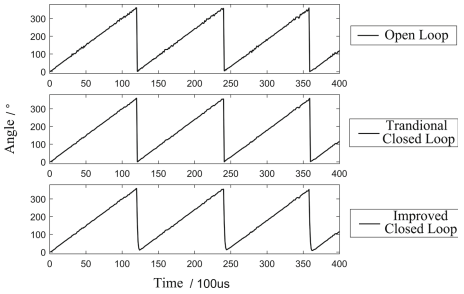

Fig. 7. Simulation results of anti-interference of three algorithms

input signals plotted in the X-Y-Z coordinate system is shown in Fig. 6. The angle output of the open-loop algorithm is consistent with the theoretical calculation result (Table 1).

3.2 Anti-interference Performance Simulation

The open-loop algorithm is fast to calculate the angle, but it will completely transfer the interference noise on input signals to the angle results. The closed-loop tracking algorithm can suppress the interference noise by type II tracker.

The U_{SIN} and U_{COS} input signals are artificially added into the noise signal to assess the anti-interference ability of the open-loop algorithm, the traditional closed-loop algorithm and the improved closed-loop algorithm. The angle output results of the three algorithms are shown in Fig. 7.

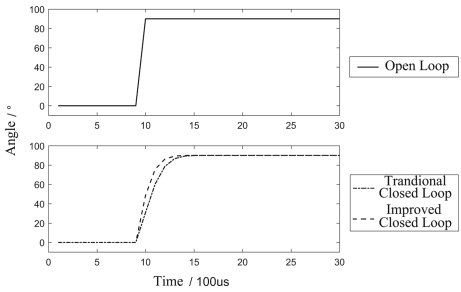

Fig. 8. Response curves of three algorithms to step input

Calculate the signal-to-noise ratio (SNR) of the angle output results of the three algorithms by using the Eq. (6).

$$SNR = 10 \times \log_{10}\left(\frac{\sum (Vs - \overline{Vs})^2}{\sum (Vs - Vn)^2}\right) \tag{6}$$

The simulation data results of the three algorithms are shown in Table 1.

It can be seen that both the traditional closed-loop algorithm and the modified closed-loop algorithm have higher signal-to-noise ratio and better anti-interference performance than the open-loop algorithm.

3.3 Dynamic Performance Simulation

The rapidity of output results of the three algorithms is assessed by step input. The traditional closed-loop algorithm and the improved closed-loop algorithm use the same PI regulator parameters. The response curves of the three algorithms to step input are shown in Fig. 8.

The open-loop algorithm has the fastest response to step input, followed by the improved closed-loop algorithm, and the traditional closed-loop algorithm has the slowest tracking.

Based on the above analysis, among the three algorithms, the open-loop algorithm has fast tracking performance, but is vulnerable to noise interference; The traditional closed-loop tracking algorithm has poor dynamic characteristics, while the improved closed-loop tracking algorithm has both anti-interference ability and tracking speed.

4 Implementation and Test

4.1 FPGA Implementation

Based on the principle of synchronous excitation peak sampling technology and improved closed-loop tracking algorithm, the shaft angle digital conversion is realized in FPGA. The composition of RTL level circuit is shown in Fig. 9.

The excitation wave modulator is used to generate sinusoidal pulse width modulation wave, and use the low-pass filter circuit to restore the sinusoidal excitation signal; ADC

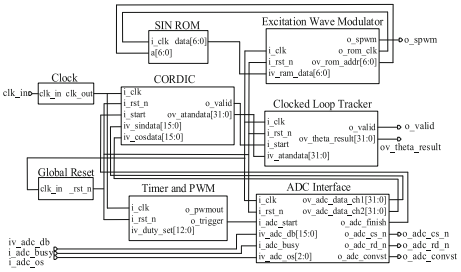

Fig. 9. Schematic diagram of RTL level circuit

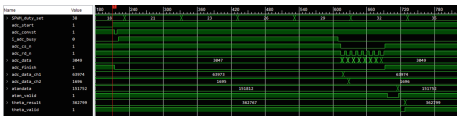

Fig. 10. Waveform of FPGA online logic analyzer monitoring

interface module is used to collect sine and cosine feedback digital signals after external ADC conversion; CORDIC arctangent module is used for arctangent calculation; The closed-loop tracking algorithm module is used to realize the closed-loop tracking and result output of the rotor angle; The timer module is used to synchronize the timing relationship between the excitation signal generation module and the ADC sampling module.

The on-line logic analyzer is used to monitor the signal flow in FPGA to verify the correctness of the conversion method. The ADC sampling result code value is 16 bits, and the output result code value of the closed-loop algorithm is 32 bits, of which the lower 16 bits are decimal digits, and the physical meaning is (0–2π) rad/s. The waveform of online logic analyzer is shown in Fig. 10.

The U_{SIN} and U_{COS} code values of ADC sampling are 63974 (signed number −1592) and 1696 respectively, and the output code value of closed-loop tracking algorithm is 362799, which is 5.536 rad/s after conversion, which is consistent with the theoretical calculation value.

4.2 Application Verification

The architecture of the improved servo controller is shown in Fig. 11.

In the servo system test, the Servo Tester Based on digital bus is used to obtain the data of servo linear displacement and motor rotor angle. The curve of linear displacement and rotor angle is shown in Fig. 12. It is verified that the digital conversion method of shaft angle is effective, the output result is correct, and the servo system works normally.

Compare the servo system using the improved servo motor controller with the servo system using the traditional controller. The frequency characteristic comparison data results are shown in Fig. 13.

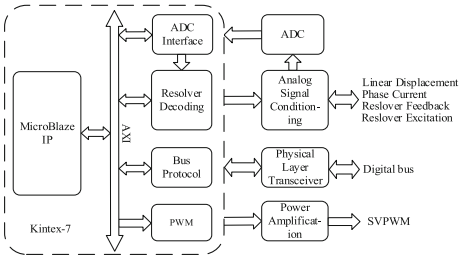

Fig. 11. Architecture block diagram of improved controller

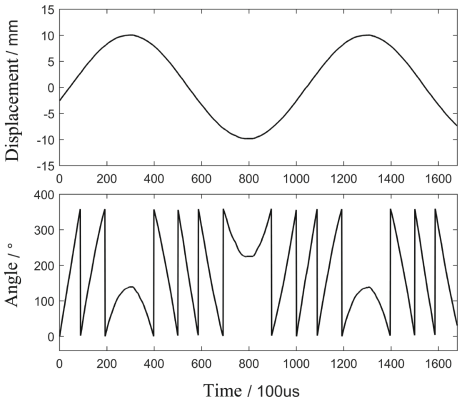

Fig. 12. Curves of liner displacement and rotor angle

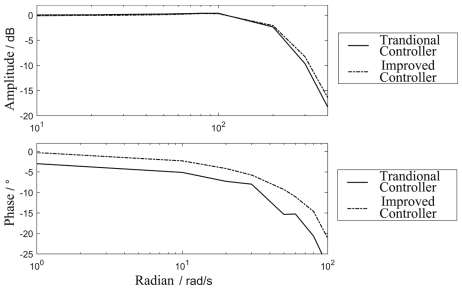

Fig. 13. Comparison diagram of frequency characteristics

The comparison results show that frequency characteristics of the servo system based on the improved servo motor controller have higher bandwidth, larger phase margin and better dynamic characteristics than the traditional servo.

5 Conclusion

This paper presents a resolver-to-digital conversion method based on synchronous excitation peak sampling technology and improved closed-loop tracking algorithm. The

synchronous excitation peak sampling technology realizes the digital demodulation of the feedback signal of the resolver. Through the simulation and analysis of the output results of the open-loop method, the traditional closed-loop tracking algorithm and the improved closed-loop tracking algorithm, the improved closed-loop tracking algorithm is finally selected, and the CORDIC algorithm and the improved closed-loop tracking algorithm are implemented in FPGA. Based on this method, a improved servo control architecture is designed and tested in the servo system. The function is normal and the performance is better than the traditional servo motor controller. With high-precision ADC, the conversion accuracy reaches 16-bit, the actual conversion time is 3.57 μs, and the theoretical tracking rate can reach 125k rps. The feasibility and practicability of this method are verified.

References

1. Zare, F., Nasiri-Gheidari, Z., Daniar, A.: A reliable integrated resolver for high precision radial-linear position measurement. In: 2021 IEEE 13th International Symposium on Diagnostics for Electrical Machines, Power Electronics and Drives (SDEMPED), pp. 1–5 (2021)https://doi.org/10.1109/SDEMPED51010.2021.9639446
2. Ren, L., Sun, S., Xiao, C., Li, Z., Song, H.: Research on fault diagnosis and position synthesize technology of resolver suitable for servo motor control. In: CSAA/IET International Conference on Aircraft Utility Systems, AUS 2020, pp. 244–249 (2020). https://doi.org/10.1049/icp.2021.0469
3. Shi, T., Hao, Y., Jiang, G., Wang, Z., Xia, C.: A method of resolver-to-digital conversion based on square wave excitation. IEEE Trans. Industr. Electron. **65**(9), 7211–7219 (2018). https://doi.org/10.1109/TIE.2017.2782228
4. Sabatini, V., Di Benedetto, M., Lidozzi, A.: Synchronous adaptive resolver-to-digital converter for FPGA-based high-performance control loops. IEEE Trans. Instrum. Meas. **68**(10), 3972–3982 (2019). https://doi.org/10.1109/TIM.2018.2884556
5. Sun, J.-D., Cao, G.-Z., Huang, S.-D., Qiu, H.: Software-based resolver-to-digital converter using the PLL tracking algorithm. In: 2016 13th International Conference on Ubiquitous Robots and Ambient Intelligence (URAI), pp. 719–723 (2016). https://doi.org/10.1109/URAI.2016.7734100
6. Huan, L., Zhong, W.: On estimation algorithm of angular velocity for servo motors with resolvers. In: 2018 Chinese Control and Decision Conference (CCDC), pp. 4019–4024 (2018).https://doi.org/10.1109/CCDC.2018.8407821
7. Saneie, H., Nasiri-Gheidari, Z., Tootoonchian, F.: An analytical model for performance prediction of linear resolver. IET Electr. Power Appl. **11**(8), 1457–1465 (2017)
8. Saneie, H., Daniar, A., Nasiri-Gheidari, Z.: Design optimization of a low speed small scale modular axial flux permanent magnet synchronous generator for urban wind turbine application. Scientia Iranica (2021)
9. García, R.C., Pinto, J.O.P., Belini, A.B.: Estimation of angular speed and park matrix from resolver position sensor signals without using trigonometric functions. In: 2018 IEEE XXV International Conference on Electronics, Electrical Engineering and Computing (INTERCON), pp. 1–4 (2018). https://doi.org/10.1109/INTERCON.2018.8526400
10. Wu, Z., Li, Y.: High-accuracy automatic calibration of resolver signals via two-step gradient estimators. IEEE Sens. J. **18**(7), 2883–2891 (2018). https://doi.org/10.1109/JSEN.2018.2806894