A Practical Design of Common Emitter Amplifier with Swamping Resistance and Bypass Capacitor

Dwi Novianto[1](✉), Risky Via Yuliantari[1], and Warindi Warindi[2]

[1] Electrical Engineering, University of Tidar, Magelang, Indonesia
nopi_jte@untidar.ac.id
[2] Electrical Engineering, University of Mataram, Mataram, Indonesia

Abstract. Amplifier is commonly used on signal processing. Class-A Amplifier is an amplification system which can amplify whole wave. Although it can amplify whole wave, it requires proper bias and collateral AC/DC load line. To set collateral AC/DC load line, Higher current through collector (IC) make better collateral. Better collateral between AC/DC load line can minimize clipping output wave but it is power consuming.

Keywords: common · emitter · amplifier · AC · load line

1 Introduction

Common Emitter Amplifier is used on wide purpose [1] because the signal amplified is not distorted although it has low efficiency [2]. The example purposes of Common Emitter Amplifier are amplifier signal on 56-161GHz bandwidth [2], LNA (Low Noise Amplifier) on 140–220 GHz bandwidth [4] and audio signal amplification [5]. Due to many purposes, determining Q point (Quiescent Point), DC (Direct Current) and AC (alternating Current) load line are important to avoid clipping signal.

Common Emitter Amplifier with bias voltage-divider and coupling capacitor from emitter to ground is depicted in Fig. 1.

For AC analysis, input signals enter through input terminal and pass Cpin than affect the collector current. So, the collector current become input signal with 180° phase shift. Signal form Collector goes through Emitter than pass bypass capacitor Cpe because capacitive reactance decreases when the AC signal pass. It is occurred because of Eq. (1).

$$X_c = \frac{1}{2a2\pi \mathrm{fC}} \tag{1}$$

The higher frequency, the lower capacitive reactance. Due to bypass capacitor, signal gain becomes

$$A_v = \frac{R_C}{r_e} \tag{2}$$

S. Sugiman et al. (Eds.): MIMSE-M-E 2022, AER 216, pp. 160–171, 2023.
https://doi.org/10.2991/978-94-6463-078-7_18

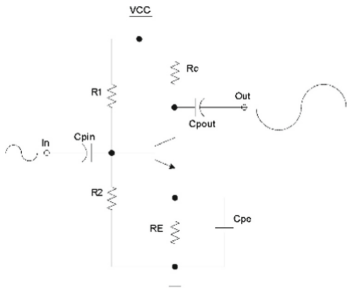

Fig. 1. Common Emitter Amplifier with Voltage Divider Bias and Bypass Capacitor.

where,

$$r_e = \frac{25mV}{I_C} \tag{3}$$

Although the gain is greater than other topology of Bipolar Transistor Amplifier, it is impractically used without considering AC and DC load line. There are two reasons why that schematic is impractically. First, schematic gain on Fig. 1 is dependent on the re where it is dependent on the temperature. To minimize temperature dependency, swamping resistance will be added between emitter and RE. Second, If the quiescent point is not in the middle of AC and DC load line intersection, the output signal will be clipped. So, in this paper will discuss about determine the component value of Common Emitter Amplifier to get proper quiescent point and output signal.

2 Common Emitter Amplifier

2.1 Common Emitter Amplifier with Swamping Resistance

Reducing temperature effect to amplifier gain, swamping resistance (R_s) between emitter and R_E is installed. To vary the amplifier gain, R_E can be replace with potentiometer which the middle foot is connected to C_{pe}. It is depicted on Fig. 2. In AC analysis, I_{AC}

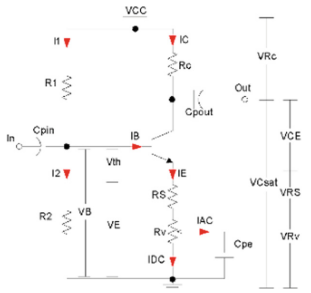

Fig. 2. Common Emitter Amplifier with Voltage Divider Bias, Swamping Resistance and Bypass Capacitor.

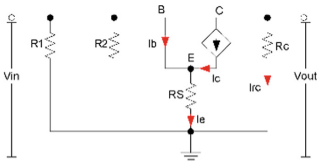

Fig. 3. Equivalent Circuit for AC Analysis

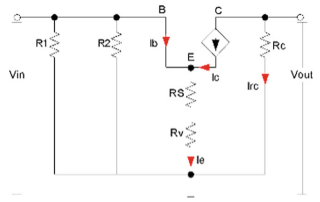

Fig. 4. Equivalent Circuit for AC Analysis with Potentiometer calculated

(AC current) from emitter goes to R_S than through C_{pe} because of question (1) and Rv in in the maximum value. Neglected the capacitive reactance of C_{pe}, the equivalent circuit can be drawn as Fig. 3.

Ignoring the direction, I_e and I_{rc} are equal because $I_c = I_{RC}$ where $I_b << I_e$. So, I_b is neglected and $V_b \approx V_e \approx V_{in}$. Therefore, gain equation is wrote as Eq. (4).

$$Gain_{AC} = \frac{V_{out}}{V_{in}} = \frac{I_c R_c}{I_e(r_e + R_S)} = \frac{R_C}{(r_e + R_S)} \tag{4}$$

Because r_e value depend on the temperature, R_S is needed to minimize temperature impact to gain value [6]. The recommendation value for R_S is $\geq 10r_e$ [7]. Gain will decrease when R_v is decreased as well. So, the equivalent circuit can be redrawn as Fig. 4. When the R_v is turn down, R_v value should be included in gain formula.

$$Gain_{AC} = \frac{R_c}{(r_e + R_s + R_V)} \tag{5}$$

Depend on the Fig. 4, signal current will be reduced by Rv and gain also decrease.

2.2 Calculation of Components Value

Looking at Fig. 2, DC current IC flows from VCC through RC, collector, emitter, RS, RV than ended to the ground. So, finding the transistor is the first step to determine value of IC, hfE (current gain) and determining V_{CC}. After determining them based on datasheet, don't forget to find voltage saturated condition between collector and emitter. Second step is, calculate RS using Eq. (5)

$$R_s \geq 10r_e \tag{6}$$

than calculate VRS using Eq. (6) and (7)

$$V_{Rs} = I_E R_S \tag{7}$$

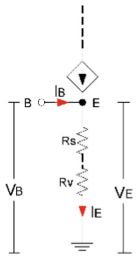

Fig. 5. Equivalent Circuit for Modeling Base Resistance

Where

$$I_C \approx I_E \tag{8}$$

Third step is, calculate the voltage of RV. It can be calculate using Eq. (8)

$$V_{R_v} = I_C R_V \tag{9}$$

Value of RV depend on value of potentiometer in the market. The lowest value of RV, the highest voltage output swing will be got because V_{R_V} has a big role on value of boundary between triode and saturation region. It is depicted on Fig. 7 and written in Eq. (9)

$$V_{C_{\text{Sat}}} = V_{CE} + V_{R_S} + V_{R_V} \tag{10}$$

The fourth step is finding the value of RC. It can be got with Ohm Law, but voltage of RC should be calculated first using Eq. (10)

$$V_{R_c} = V_{cC} - V_{C_{\text{sat}}} \tag{11}$$

After getting the voltage of RC, it can be found using Eq. (11)

$$R_C = \frac{V_{R_c}}{I_c} \tag{12}$$

Fifth step is calculating base resistance of transistor with DC analysis. Look at Fig. 2, $V_E = V_B = V_{th} + V_{R_S} + V_{R_V}$ and V_B equal to V_E. Looking at the base, input resistance can be denoted.

Depend on Fig. 5, base voltage and emitter voltage are equal. So, to formulate base resistance refer to ground Internal resistance of emitter and swamping resistor are series. Therefore, using Ohm Law base resistance can be written as

$$R_B = \frac{V_B}{I_B} = \frac{V_E}{I_B} = \frac{I_E(R_S + R_V)}{I_B} \tag{13}$$

where,

$$hfE = \frac{I_C}{I_B} \tag{14}$$

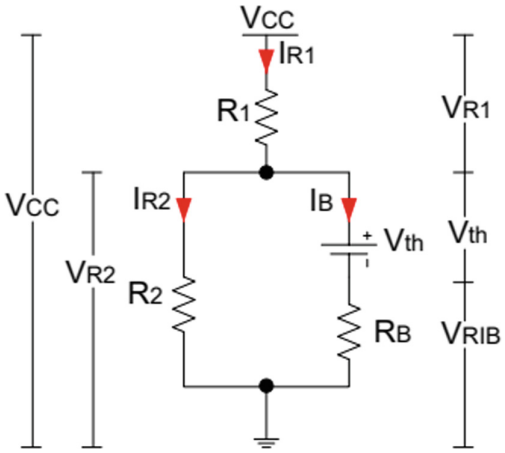

Fig. 6. Equivalent Circuit for Calculating Bias Resistor

So,

$$R_B = (R_S + r_e)hfE \tag{15}$$

Sixth step is calculating value of R_2. Maximum value of R_2 should be $\leq \frac{R_B}{10}$ to minimize through base of transistor. So, most of current from R_1 goes through R_2. Than the final step is calculating the value of R_1. Thevenin Theorem is not used because the beiger Thevenin resistance the bigger error on quiescent point [8].

Calculating the last component R_1, schematic approach should be drawn.

On Fig. 6, $V_{th} = V_{BE} = 0{,}7V$ for silicon transistor and $V_{R_2} = V_{th} + V_{RB}$. To obtain V_{R_1}, V_{RB} should be calculate first using Eq. (15)

$$V_{R_8} = (R_S + R_V)\, I_C \tag{16}$$

Substituting Eq. (13) and (14) to Eq. (16), voltage of R_2 could be

$$V_{R_2} = V_{th} + (I_c(R_s + R_V)) \tag{17}$$

After V_{R_2} obtained, current through R_2 is calculate using Ohm Law.

$$I_{R_2} = \frac{V_{R_2}}{R_2} \tag{18}$$

Than current through R_1 can be obtain with summing I_{R_2} and I_B. So, value of R_1 can be obtained with Eq. (18).

$$R_2 = \frac{V_{R_1}}{I_{R_1}} = \frac{V_{CC} - V_{R_2}}{I_{R_1} + I_B} \tag{19}$$

Value all components are obtained. DC load line can be drawn.

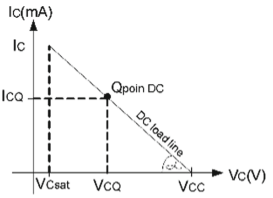

Fig. 7. DC Load Line Plotting.

2.3 DC and AC Load Line

On Fig. 7, collector voltage is close to V_{CC} when transistor in cutoff condition. Collector current was determined on the first step and minimum value of collector voltage, boundary between triode and saturation region, was calculated in the third step.

Quiescent voltage is considered in the middle between $V_{C_{sat}}$ and V_{CC} but in fact Quiescent point can be closed to $V_{C_{sat}}$ or V_{CC} depend on the gain. The important thing is Quiescent point is set to avoid clipping output wave form [9]. Depend on Fig. 7, I_{C_Q} can be obtained trigonometrical equation.

$$\tan\alpha = \frac{I_C}{V_{CC} - V_{C_{Sat}}} \tag{20}$$

And

$$\tan\alpha = \frac{I_C}{V_{CC} - V_{C_Q}} \tag{21}$$

So,

$$I_{C_Q} = \frac{I_C\left(V_{CC} - V_{C_Q}\right)}{V_{CC} - V_{C_{Sat}}} \tag{22}$$

To get Quiescent voltage, part of R2 can be replaced with potentiometer depicted on Fig. 8.

Value of $R_2 = R_{Q_{tune}} + R_{2_{new}}$ and $R_{Q_{tune}} > R_{2_{new}}$ is recommended to get significant variation of quiescent voltage. Making sure the signal output swing, AC load line is needed to plot. To get signal current through collector (I_c), Eq. (22) can be used.

$$I_c = I_{C_Q} + \frac{V_{C_Q}}{R_{Out}} \tag{23}$$

$R_{Out} = R_C$ when load resistance (R_{Load}) doesn't exist. If there is a load resistance, R_{Out} would be $R_C \| R_{Load}$. So as Voltage signal can be plot using Eq. (23).

$$V_c = V_{C_Q} + \left(I_{C_Q} R_{Out}\right) \tag{24}$$

After calculating I_c and V_c. AC load line is plotted as Fig. 9

On Fig. 9, AC load line is proper because its slope is steeper than DC load line. To make the two as close as possible, I_C should be raised.

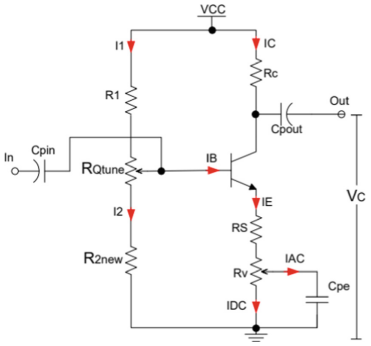

Fig. 8. Bias for Quiescent Voltage Tuning

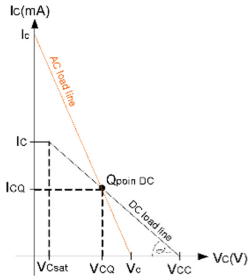

Fig. 9. AC and DC Load Line Plotting

2.4 Design Proper AC Load Line

Value of I_C should be in rage in transistor datasheet. Greater should be lower I_c, greater V_c and greater $V_{C_{Sat}}$. Due to greater $V_{C_{Sat}}$, voltage output swing will be decrease because increasing R_S and R_V. It led to $V_{C_{Sat}}$ increase. To minimize $V_{C_{Sat}}$ value of R_V should be decrease and R_S should be on minimum value.

Bipolar Junction Transistor type 2N3904 with Common Emitter topology is used for example of AC load line designing. Depend on the datasheet [10], hfE 200 can be flown by 1mA – 10mA through collector.

On Fig. 10. R_L depict input resistance on the next stage. For example, value but close to the reality is 6720Ω. Value of RV is 500 Ω. It was chosen because it is minimum value of potentiometer in the market. So, with four dependent variables (V_{CC}, hfE, R_L and R_V), I_C is varied by 2mA, 4mA, 6mA and 8mA. The result of load line calculation was written on Table 1.

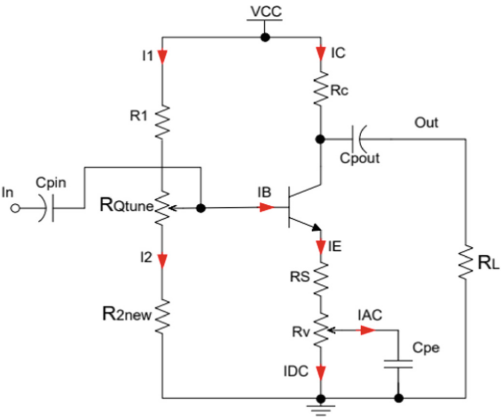

Fig. 10. Common Emitter Amplifier with Voltage Divider Bias, Swamping Resistor and Load

Table 1. Calculation Result.

I_C	V_{Csat}(V)	I_c(mA)	V_c(V)	V_{CQ}(V)	I_{CQ}(mA)
2mA	2,25	4,56	20,65	16,12	1
4mA	3,25	6,96	23,33	16,62	2
6mA	4,25	9,53	24,98	17,12	3
8mA	5,25	12,32	26,09	17,62	4

Result value on each row was depicted on Fig. 11, Fig. 12, Fig. 13 and Fig. 14.

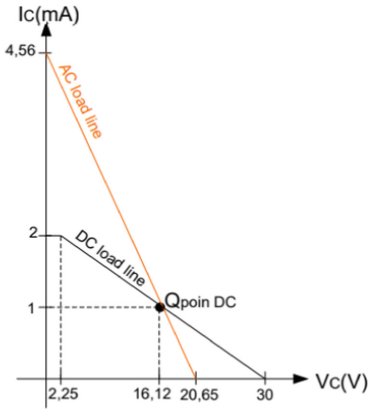

Fig. 11. DC and AC Load Line when $I_C = 2$ mA

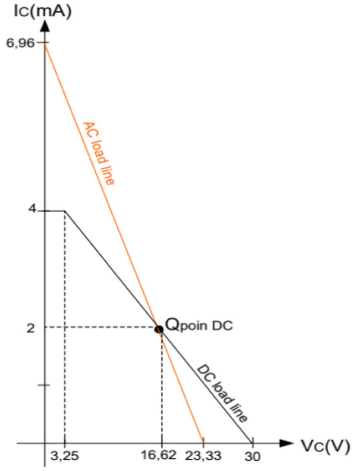

Fig. 12. DC and AC Load Line when $I_C = 4$ mA

Look at Fig. 11, Fig. 12, Fig. 13 and Fig. 14.

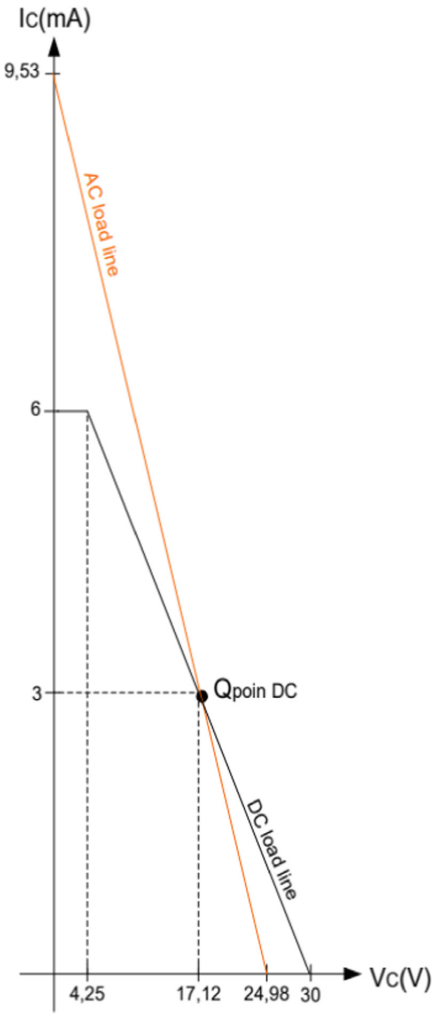

Fig. 13. DC and AC Load Line when $I_C = 6$ mA

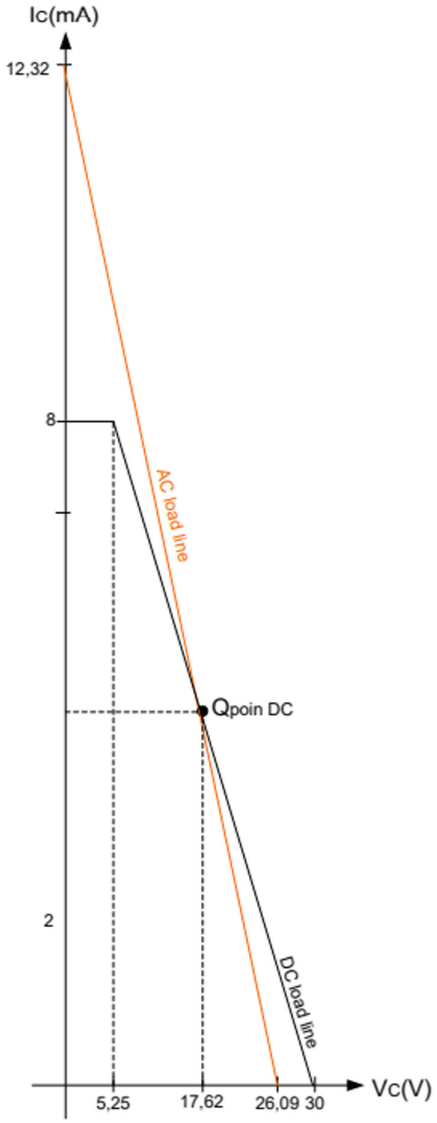

Fig. 14. DC and AC Load Line when $I_C = 8$ mA

3 Conclusion

Base on calculation and load line plotting. Determining higher IC makes higher collate ration. Higher I_C, DC and AC load line will be more collateral. But the power consumption goes higher as well. The advantage of higher collateral between AC and DC load line is minimum clipping output.

References

1. Pan, Z., Yang, C., Feng, R., Qi, M., Luo, Q., Zhu, M.: The Design of a Low Distortion Power Amplifier Based on Cascode. pp. 1–4 (2019).
2. Jeong, J. H., Kim, G. H., Min, B. R., Ahn, C. H., Cho, G. H.: A high efficiency class A amplifier accompanied by class D switching amplifier. In: PESC97. Record 28th Annual IEEE Power Electronics Specialists Conference, vol. 2, pp. 1210–1216 (1997).
3. Hou, Y., et al.: A 56–161 GHz Common-Emitter Amplifier with 16.5 dB Gain Based on InP DHBT Process. Electronics 10(14) (2021).
4. Stärke, P., Steinweg, L., Carta, C., Ellinger, F.: Common Emitter Low Noise Amplifier with 19 dB Gain for 140 GHz to 220 GHz in 130 nm SiGe. In: 2019 International Conference on Wireless and Mobile Computing, Networking and Communications (WiMob), pp. 1–4 (2019).
5. Dan-Abia, D.E., Obot, A., Udofia, K.M.: Design and Analysis of a Multistage Common Emitter Amplifier for Low Frequency Applications. Eur. J. Eng. Technol. Res. 4(10), pp. 87–92 (2019).
6. Kumar, A., Ganguli, S.: A new Hall-effect enabled voltage amplifier device based on magnetic and thermal properties of materials. J. Magn. Magn. Mater. 514, p. 167054 (2020).
7. Floyd, T.L.: Electronic Device Conventional Current Version. Pearson, Malaysia (2018).
8. Chen, X. et al.: Error Analysis of Approximate Calculation of Voltage Divider Biased Common-Emitter Amplifier. Circuits Syst. 8(10), p. 247 (2017).
9. Wardhana, A.W., Ramadhani, Y., Priswanto, P.: Design and Simulation of a Multistages Common-Emitter, Common-Collector, AC Voltage Amplifier. J. Nas. Tek. ELEKTRO (2022).
10. ON Semiconductor: General Purpose Transistors NPN Silicon 2N3903, 2N3904, https://pdf1.alldatasheet.com/datasheet-pdf/view/11470/ONSEMI/2N3904.html, last accessed on Aug. 11, 2022.