IC Circuits—Soul of Modern Society

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Abstract. Almost every technology people used from last century till today contains components of Integrated circuits. In order to present the significance of chips, this article is going to go through the fabrication of chips—from chip design, wafer growth, wafer fabrication to package and testing. Moreover, a generalization of the chip categories will be discussed and an evaluation of the importance of chips will be presented in this paper as well.

Keywords: Fabrication · Technology · Design · Packaging · Etching

1 Introduction

Integrated circuit constitutes the core of the modern technology. The famous Moore's law stated that the computational power of chips doubles per 18 months and over half a century of development, the Moore's law still holds. And over the last 60 years, the drastic progress in technologies not only provide convenience, but also link people around the world closely together. In order to demonstrate the importance of the IC chips, this article will go through the production of IC chips and the chip categories. Then, the article will evaluate the weight of chips in the modern society.

2 Production of IC Chips—International Cooperation

The main procedure of creating a single chip can be categorized into following 4 sections—design, production, package and testings. Each section is done by different companies. For example, companies like Intel and Qualcomm are specialized in designing chips and ASML is the company which makes equipments to manufacturing chips. Also, there are companies like SUMCO which specialize in making raw materials and companies which are responsible for final packaging and testing of products. However, nor many countries can support the entire industry-from design to testing. Countries around the world take part in different stages of the entire industry.

3 Design

Although IC circuits or chips look like little chocolate chunks, they in fact contain numerous tiny electronic circuits. As for circuits, we can design the layout of different

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circuits based upon each corresponding requirement. Traditionally, there are two major methods of chip designs—Down-Top and Top-Down.

In regard to Down-Top, the idea of drawing is based upon the systematic need. It utilizes the basic logic gates and constructs each independent functional mode. Then the modes will connect together and form an integrated system which will be undergo a series of final testing and analyzation. However, the Down-Top method is created for simple chip designs, so it cannot satisfy complicated chip designs. The other method is Top-Down. The Top-Down procedure starts with chip specification where all the parameters are determined upon the chips' requirements. Then the certain hardware developing languages like Verilog and VHDL are used to make logic designs. Moreover, the logic designs are converted into circuit designs in the form of gates. In the end, the circuit designs are converted into physical design which is the final layout. The Top-Down method has short designing period and higher success rate of constructing. However, it relies upon advanced EDA tools and environment, and it is also expensive.

Additionally, there are chip design methods based on artificial intelligence (AI). It starts with identification of chip functions which will produce the logic designs of chips. Then it produces the electronic designs of chips. In the end, the physical layout of chips is finalized. The entire process of AI designing doesn't involve any human works. What only needs is the simple function description. Moreover, the AI will self-study the current process of chip designs in order to produce the physical layout for chips. Since the machines or AI have faster computational speed, it can accelerate the process of chip designing [1].

4 Manufacture/Fabrication—From Raw Material to Wafer

4.1 Wafer Growth

A wafer starts as a bar of polycrystalline silicon, either molten or solid, depending upon which method is used. It is of high purity. The first step is to make a monocrystalline silicon bar. There are two major and different processes—Czochralski and float-zone processes.

As shown in the Fig. 1 below, poly-crystalline silicon and dopant are mixed together in the pot. Dopants depend on which types of monocrystalline silicon stick will be the product: P-type needs elements like boron, gallium, indium, etc. And n type needs elements like phosphorus, arsenic, antimony, etc. Then the mixture is heated up to the melting point of silicon and the mixture becomes molten. Moreover, the seed is lowering down close to the surface of mixture where the seed is heated. After that, the seed contacts the molten mixture and the seed begins rotating and is lifted up. Through the ascending duration, the silicon begins crystallization around the seed. Additionally, the ascending speed of seed will temporarily increase as an attempt to create a section, thinner than the diameter of seed. Later on, the silicon will continue to enlarge in diameter by lowering the rotating speed and adjusting the temperature. However, it is crucial to determine the diameter of the silicon rod because as soon as the diameter of silicon rod reaches its expectation value, the silicon rod is ascending in a faster speed. The diameter of the silicon rod can be determined by an improved stacked autoencoding method (in plain words, AI or machine learning) [2]. Overall, the silicon rod produced by Cz process has

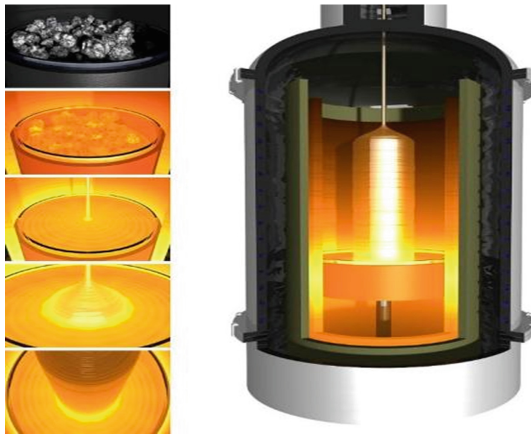

Fig. 1. Cz process [4]

higher concentration of oxygen. Although it is not harmful, it does can impact the overall performance of chips made by the silicon rods. A new technology called the OXYMAP technology can be used to monitor the oxygen concentration during the Cz process [3].

In float-zone process, the poly-crystalline silicon rod is heated in the furnace. Then, the crystalline seed contacts the heated area and the seed also melts. Moreover, the poly-crystalline rod will be lifted upward while the seed will fall down spirally until a mono-crystalline rod is formed.

Then, the monocrystalline silicon stick will be sliced, i.e. by diamond wire [5], into wafers of 1 mm thick. Next, the wafers will be chamfered as an attempt to remove all the unpleasant scars, glitches, cracks, etc. After chamfering, the wafers will have a smoother edge on its surface which also will have an increasingly stronger mechanical strength. Furthermore, the wafers will be grinded in order to remove the trenches and pollutions on the surface of wafer due to cutting. After that, the wafers will be etched via metal-assisted chemical etching so as to remove all the cuttings from the previous manufacturing. Moreover, the wafers also will be polished as an attempt to make its surface look more horizontal and cleaner. In the end, the final product of wafers will be scrutinized over its quality and the those which pass the ultimate examinations will be sold to customers.

4.2 Basic Technologies Involving in Fabrication of Chips from Wafers

4.2.1 Photolithography

The most crucial procedure in chip production is the Photolithography. It determines the minimum line width of the chips. An advanced Photolithographic technology can produce more chips from single silicon plate and thus lower the production cost. Also, it can improve the computational power of chips. The main procedures of the photolithography can be summarized into 3 following steps—photoresist coating, exposure and development.

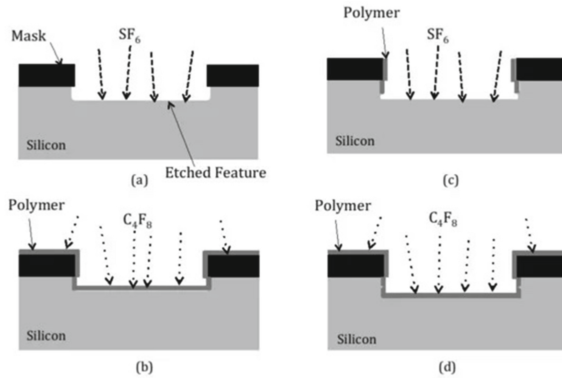

Fig. 2. Example of etching profile [9]

Photoresist coating means to glue a layer of photoresist onto the wafer. There are two types of photoresist—positive and negative photoresist. The photoresist is sensitive to light waves with specific wavelength. First, the photoresist is dropped onto the wafer. Then a motor will spin the wafer so that the photoresist can evenly spread across the wafer. In the end, the solvent is steamed away from the photoresist which will become hardened. However, the photoresist film has non-uniform thickness. So a SO (standard 0) sheet, larger than wafers, is coated with photoresist first, which will then bond with the wafer. As a result, a uniform layer of photoresist can be obtained on the wafer [6].

After that, the wafer undergoes exposure. The UV source is used to shine UV light onto the wafer. In addition to that, the UV LEDs, which are cheaper in both cost and repair bills, can be used in exposure procedure [7]. The positive photoresist will dis-compose under the UV light rays and become solvable, while the negative photoresist will polymerize. On the other hand, the negative photoresist becomes insoluble and only certain solvents can dissolve the negative photoresist.

In the end, the wafer undergoes development. The development solvent, made of mixture of organic solvent, is used to solve photoresists. During development, only certain photoresists which are positive. So part of surface area of wafer is exposed. The exposed area will later on be involved in etching. In the end, more corrosive solvent is used to strip photoresist off the wafer; also, chemical etching with reacted ion can also strip the photoresist off in an oxygen-rich environment. However, during stripping, bubble defect will occur as wafers contain a variety of different molecules which are used to implement wafer with different parameters. Under high temperature, these different molecules, for example, BF2, will disbond or release specific atoms which will react with the silicon atoms due to high temperature. So lowering temperature can reduce the bubble defect [8] (Fig. 2).

4.2.2 Film Growing and Striping

Another crucial technology is Film technology. Since the chips are multiple layers of circuits, it is important to deposit different layers of films, made from different materials with various conductivity, onto the wafer. The primary material used in film is silicon

dioxide which is a great insulator and can be grown easily under the condition of oxidation and heating. There are 3 major conditions used in growing Silicon Dioxide—Dry and wet oxidation and Deposit. The dry oxidation is a heating condition with pure and dry oxygen. The film of silicon dioxide needs to be very thin, so nitrogen gas can be used to control the growth of the film [10]. Although the growth rate of film is slow but the dry oxidation method can produce films with high quality. Wet oxidation is the oxidation under the condition of gaseous mixture of oxygen and water vapor. It is a fast motion but the films' quality decreases as the process continues. Multiple factors contribute to worsening quality, for example, the run out of water during oxidation process bears 20% of responsibility of decreasing thickness of film while the reduction of steam concentration impacts the thickness of film the most [11]. The deposit method is used on the non-silicon material. It utilizes the reaction between gaseous silicon mixture and gaseous oxidizer to produce insulate or protective layers between layers of conductors.

After growing the film, we also need to strip them. Stripping is mainly served to construct circuits onto the wafer. There are two methods of stripping—dry and wet stripping. The wet stripping uses diluted hydrofluoric acid to dissolve oxide film while the dry stripping uses RIE (reacted ion etching) or Plasma or chemical gas. In order to enhance the overall productivity of both dry and wet etching process, modular gas delivery system can be implemented [12].

Additionally, there are films made of other materials, for instance, metal films and insulator films. In order to grow these films, one of the methods is Deposition. It is to either create a film onto the surface of mono-silicon crystal or to create a film of poly-silicon crystal on the top of existing film of oxide or nitrite. Another method is metal sputtering or evaporation.

4.2.3 Doping

However, since all the chips are designed based upon different requirements, sometimes certain requirements need wafers to have different electrical properties. So in order to match the expected parameters, impurities are inserted into the wafers. Such method is called Doping. One of the Doping method is called diffusion. Wafers are initially placed on the wafer boat which will go through the entire furnace. Then depositions of dopants are created on the surface of wafers. After that, the dopants will expand across the wafers from area of higher concentration to area of lower concentration as the wafer boat moves across the process furnace.

Another method is Ion Implantation. It converts the dopants into ion gaseous molecules and the ion particles will be accelerated via a linear accelerator. Then, the ion beams will be deflected through pairs of deflection plates. In the end, dopants are inserted onto the surface of wafers at different angles. Since numerous nozzles are used to spray dopants onto wafers, excess amount of gas may be flowing into the process furnace and turbulence, caused by gas, will cause excessive amount of particles being generated on the wafers. So the flow of gas into the furnace can be improvised in order to resolve defects [13]. Moreover, the defects during the implantation process can be monitored by PMR (photo-modulated-reflectance) [14].

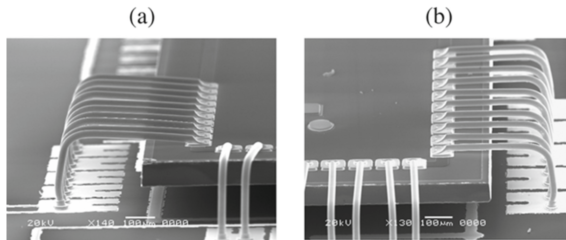

Fig. 3. Demonstration of packaging [16]

5 Testing and Packaging

In the end, the dies produced by the fable factories need to be packaged, followed by testing. Packaging is to further manufacture of dies into functional chips. Also, the chips will be granted external physical protection which will exclude the environmental influences, enhance the heat dissipation, connect the chips with the external circuits. The packaging can be separated in pre- and post- mold over the crafts. Also, it can be separated based the material used—metal, china and plastic packaging. In addition to that, packaging can also be distinguished upon the outfit of chips: SIP, DIP, PLCC, PQFP, etc. Moreover, the integrated circuits not only are consisted of single chips. So the System-in-Package (SIP) will combine all different electrical components together. During the SIP, wire bonding will fuse thin metal wires in between chips and chips or chips and base. Moreover, wire bonding can also be done at wafer level and it can allow shorter test cycle [15].

After packaging, it is the testing of the final products. So all the chips which have compromised functions or which fail to meet the requirement will be filtered out. There are a series of testing, such as DC and AC parameter test, function check, mixed signal module test, analog module and etc (Fig. 3).

6 Chip Categories

Chips can be divided into different categories based upon their gate length—28 nm, 14 nm and etc. The smaller the gate length, the more complicated the production will be.

Moreover, chips with smaller gate length have stronger computation power, have better energy cost efficiency and lower the production cost. So the chips' gate length become smaller and smaller throughout the history. Moreover, chips can also be separated upon the signals they process—Analog and digital chips. Furthermore, chips can be separated upon their functions—GPU, CPU, FPGA, DSP, ASIC and SOC.

7 Conclusions

Overall, the entire IC industry has a significant position in the modern society. According to data from Chinese boarder-control, China imported more than 400 billion bucks of IC

products which roughly are equal to more than 630 billion pieces in 2021. Moreover, we can see that the IC components have been widely used in everywhere. For example, our daily digital consumer products all contain numbers of chips, like mobile phones, PCs and televisions, etc. In addition to that, other products like household appliances, cars, etc. all need IC chips. The IC plays an important role in the modern society. Given its size, it has the most sophisticated structure and the technologies involving in production covers a variety range of different subjects. Also, the applications of chips involve nearly every digital product used in real life.

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