Modeling and Simulation of Multi Gate MOSFET with Reduced Short Channel Effects for High Power Applications

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Abstract. The Multigate (Double-gate) MOSFET has been proposed for high voltage and high-power applications with decreased short channel effects and drain current with gate overlap. This model takes in to account the short-channel effects (SCEs) in thin-layered MOSFETs with large drain regions by incorporating the drain resistance effect in the device. As a result, the device's SCEs are reduced. The gate contact overlapped region significantly affects the device operation for high-voltage FETs. These effects are modeled by self-consistent solutions of available multigate MOSFET device models with potential distribution. Multi-gate devices offer a significant benefit of enhanced SCE, as the gate controls the channel electrostatically from multiple sides and increased on state drive current which results in faster circuit speed. The demonstrated model can be further applied for size limitations in the modeling of multigate MOSFETs.

Keywords: multigate MOSFET · short channel effects · channel potential · drain resistance effect · overlap length

1 Introduction

Nowadays, low and high-voltage devices are incorporated on a single chip for specific applications where the low-power circuits control the high-voltage switching circuits [1]. Reducing the channel length became essential for integrating high-density circuits in a chip and prone to generating short channel effects. These effects are decreased by considering the ultra-thin layer of multigate MOSFET structures [5]. Despite the use of an ultra thin channel layer, reducing short channel effects remains critical [9]. The thin layers of the device can be prepared with numerical device simulations [10]. This

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paper models the short channel effects with ultra-thin layers, overlapped contact regions, and constant potential distributions. The potential distribution is considered at the drain, source, and in center of the channel. There is no degradation in the performance of the device due to being heavily doped at source/drain regions, and current density can increase with large conductivity [11].

The MOSFETs are required for high voltage and high power applications [13]. Accordingly, the MOSFET has been optimized to work at high voltages and is achieved at the edge of drain contact [18]. The high voltage operation is achieved due to the effect of high drain resistance caused by increasing drain contact length and decreasing the drain region's doping concentration. This work focuses on modeling short-channel effects and drain current of multigate (double-gate) MOSFET for high–voltage/power applications by targeting the 2 V to 3 V range as high voltage and 1 V to 1.3 V range as low voltage. Also, the device's performance is analyzed with different gate and drain voltages. The drain resistance effect and short channel effects are also studied in the proposed model and can be valid for both high and low voltages. In model development, the complete potential distribution present in the device is considered by including the effect of drain and gate overlap length effects.

2 Device Structure

The cross-sectional view of the multigate (double gate) MOSFET is shown in Fig. 1. The device structure is designed and analyzed using a 2D numerical TCAD tool where the device physics is included [19].

The DG-MOSFET has a lightly doped long drift region to work for the given high voltages in the device. The drift–diffusion model using the Poisson equation and carrier-continuity equation is utilized for the simulation analysis at 300 K. The drift-diffusion approximation helps in realizing transition for different bias conditions. In order to incorporate well quantum confinement effect in to the energy sub-bands for two dimensions, the diffusion and drift space mode method has been utilized. Additionaly, the model derivations have involved the use of the Newton-raphson method.

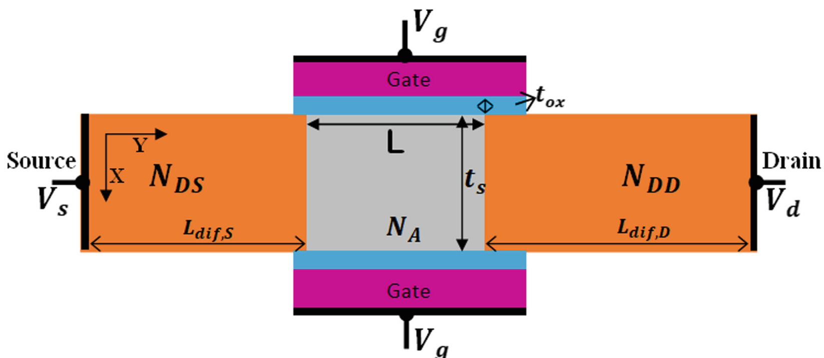

Fig. 1. Cross-sectional schematic view of considered multigate (double-gate) MOSFET

Table 1. The symbol definitions along with the parameter values used in the calculation and model development of the proposed device structure

Parameter	Definitions	Values
L	Channel Length	$25nm$
W	Channel width	$1\mu m$
N_A	Channel region dopingconcentration	$10^{15}cm^{-3}$
N_{DS}	Source region doping concentration	$10^{20}cm^{-3}$
N_{DD}	Drain region doping concentration	$10^{19}cm^{-3}$
t_{ox}	Oxide equivalent thickness	$1.5nm$
t_s	Silicon material thickness	$10nm$
$L_{diff,d}$	Drain region length	$75nm$
$L_{diff,s}$	Source region length	$75nm$
L_{over}	Channel overlap region length	$10nm$
DOS	Conduction-band density of state	3.24e17 $\mathrm{m}^{-2}\mathrm{V}^{-1}$
μ_0	Low field mobility	$900cm^2.V^{-1}s^{-1}$
v_{sat}	Velocity Saturation	$1 \times 10^7 cm/s$

The meshing of structure is selected by Deck Build Editor for exact simulation of all corners of the proposed device to step up the efficiency. Numerical-based simulations are performed by physical parameter models such as FLDMOB CONMOB and CVT, Fowler-Nordheim. The SRH and Auger recombination models are considered for minority-carrier recombination. The results obtained by models and methods are analyzed, and output data is extracted in the Tony-plot window. The definition of symbols, parameters, values used in the calculation, and model development are enumerated in Table 1.

3 Model Development

3.1 Short Channel Effects

Analytically modeled and numerically simulated V-I characteristics with different drain voltages of the considered device structure are shown in Fig. 2. The SCEs arise due to the deep large current flow in the center of the device being controlled by the electric field. The current density of the channel and between two gate regions with $V_{ds} = 50$ mV and $V_{gs} = -0.5$ V is shown in Fig. 3. It is observed that the current density is maximum at centre of the channel.

The presence of an inversion layer at the interface between the gate and channel can lead to a reduction in the deep current flow increasing V_{gs}. The charge distribution in the channel region is considered for modeling of short-channel device effects due to the flow of charge from source-channel-drain junctions in the channel region along the

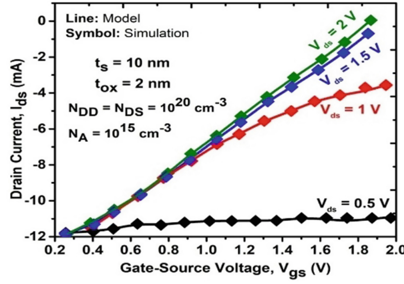

Fig. 2. V-I characteristics with different drain to source voltages

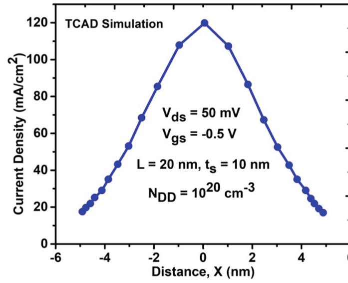

Fig. 3. Current density at the center of the channel

y-direction with cubic function [20].

$$\phi(y) = K_o \cdot (y + K_1)^3 + K_2 \tag{1}$$

The parameters K_0, K_1 and K_2 are the function of the charge present at source-channel-drain junctions and are described in Table 2. The other parameters used in model development with definitions are described in Table 2.

The potential gradient K_0 is obtained by solving Poisson's equation for proposed structure [21]. The minimum potential K_1 allows the maximum drain current along the y direction at a subthreshold state when $y_{\min} = K_1 y_{min} = K_1$. The potential distribution at channel, drain, and source junctions would overlap by decreasing the length of the channel, and its consequences would be the increase of minimum potential ($K_2 = \phi_{\min}$), as shown in Fig. 4.

The $\phi_{\min}$ will increase along with the long channel structure, and it is denoted as [20]

$$\Delta\phi_{\min}(V_{gs}, V_{ds}, L) = -2A_o(Y_{\min} - \frac{L_o - L}{2})^3 \tag{2}$$

Here, Y_{min} is denoted as the minimum potential position along the direction of the channel, which can be determined from the potential fields originating at the channel-source, channel-drain junctions and is written as

$$y_{\min} = -V_{di}/E_{source} + E_{Drain} \tag{3}$$

Table 2. The parameters and their expressions used in model development

Parameter	Definitions	Expression
K_0	Channel potential gradient	$sign(y).(V_{bi,source} - \phi_{\min})/(L_o/2)^3$
K_1	Minimum charge present at a position along the y-direction	$Y_{\min}$
K_2	Minimum potential	$\phi_{\min}$
$V_{bi,source}$	Built in potential at channel-source interface	$\beta^{-1} \cdot \ln(\frac{N_{ds} \cdot N_A}{n_i^2})$
$V_{bi,drain}$	Built in potential at channel-drain interface	$\beta^{-1} \cdot \ln(\frac{N_{dd} \cdot N_A}{n_i^2})$
E_{source}	Maximum electric field present at channel-source interface	$\frac{(V_{bi,source}+V_s-\phi_{\min})}{XJ_o}$
E_{drain}	Maximum electric field present at channel-drain interface	$\frac{(V_{bi,drain}+V_s-\phi_{\min})}{XJ_o}$
XJ_o	Scaling parameter for length	$\sqrt{(\varepsilon_s t_s t_{ox}/2\varepsilon_{ox})(1+\varepsilon_s t_s/4t_{ox})}$

V_{di} is potential difference at source channel drain junction edges.

E_{drain} and E_{source} are the electric fields originating at drain and source junction regions which are determined from the doping concentrations at the respective junction. The lateral distribution of potential influencing the device characteristics is modeled by considering the change in ϕ_{min} [22] as

$$V_G' = V_{gs} - V_{FB} + \Delta\phi_{\min} \tag{4}$$

Here, V_G' is utilized to determine surface-potential (ϕ_s) at the gate to channel interface, which is calculated by Gauss law and the self-consistent solution of the Poisson's equation is written as

$$\phi_s(y) = V_G' + \frac{Q_{si}(y)}{C_{ox}} \tag{5}$$

Here, Q_{si} is the charge present in the channel, C_{ox} is the gate oxide capacitance. The function $\varnothing_S(y)$ $\phi_s(y)$ is iteratively solved by the Newton-Raphson method, which includes analytical initial accurate value to improve the speed of calculations. Only the drain-side and source-side channel regions are solved in place of the complete channel's Poisson equation solution by taking quasi-Fermi distribution in the channel region with approximations of drift-diffusion.

The gate capacitance with respect to applied gate voltage characteristics is analyzed to estimate the short channel device effects and is shown in Fig. 5. The short channel effects are raised by induced deep leakage current in the channel, and related charges appear in the total gate capacitance over the threshold region.

The short channel effect impacts parameters such as threshold voltage roll off, threshold voltage reduction, and subthreshold swing, which are shown in Fig. 6 with higher

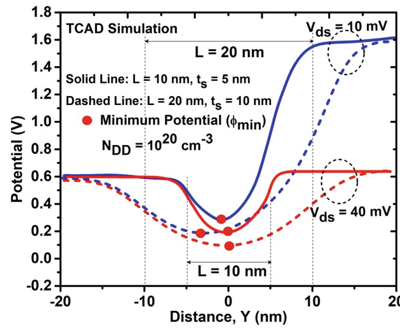

Fig. 4. TCAD numerical simulation results of the distribution of potential in the center of the channel for different channel lengths and thicknesses at $V_{ds} = 10$ mV and 40 mV

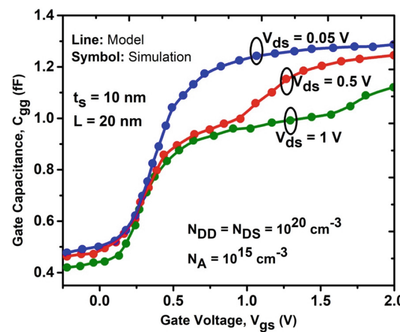

Fig. 5. The gate capacitance in respect of applied gate voltage characteristics for different applied drain voltages with L = 20 nm and $t_s = 10$ nm

drain side doping of 10^{20} cm^{-3}. From these results, it is observed that the reduction of short-channel effects is improved.

3.2 Effect of Depletion Region and Drain Resistance

The two effects that are dominant when low doping at the drain region are: (1) the extension of depletion region through the operation of the short channel device's sub-threshold swing (2) The effect of drain side resistance region through applied high drain and gate voltages. These two effects are included in the development of DG-MOSFET [23]. The effect of drain region resistance increases due to the distribution of potential expansion into the deep drain region with low doping concentration [18]. The gate region extends towards the drain side at the gate edge due to the drift region and the current flow in the channel. The potential generated at the gate region edge towards the deep drain side causes increasing drain resistance with small N_{DD}. The local point V_{DP} surrounded by the overlapped gate region refers to the gate control endpoint, and it is calculated by the current flow in the channel and drift region current. The flow of current in the

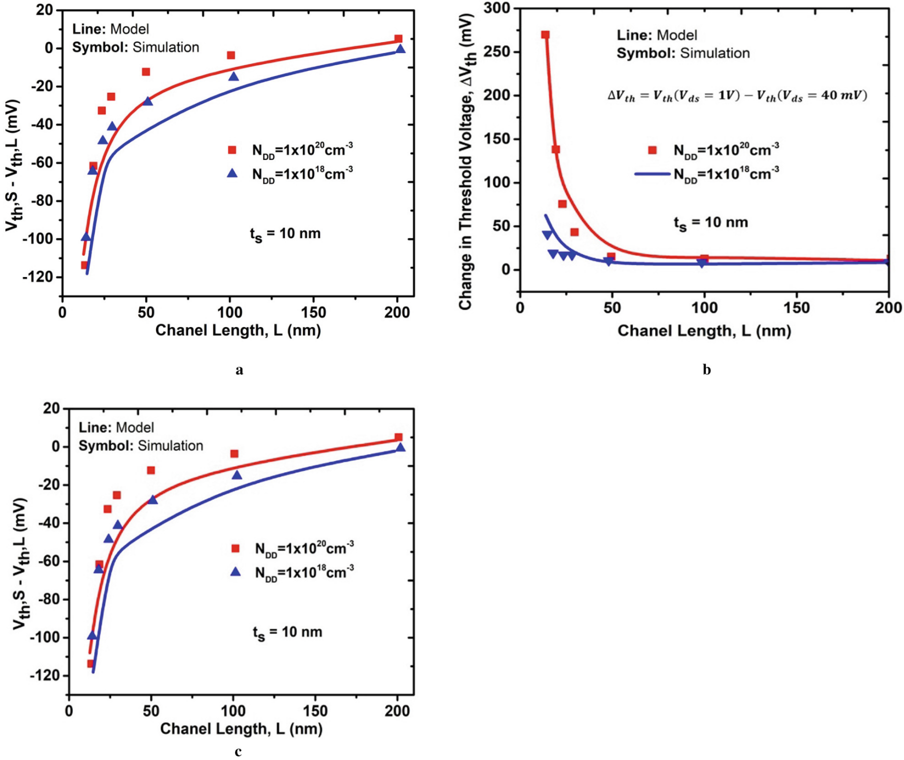

Fig. 6. The short channel effect parameters with respect to channel length variation (**a**). Threshold-voltage roll-off (**b**). Threshold voltage reduction, and (**c**). Subthreshold swing

channel region is expressed as

$$I_{ds} = 2\frac{W}{L} \cdot \frac{\mu_{eff}}{\beta} \times \left[(Q_{nL} - Q_{nO}) - \frac{\beta}{2} \cdot (Q_{nL} - Q_{nO}).(\phi_{SL} - Q_{SO}) \right] \tag{6}$$

The flow of current in the drift drain region (I_{DPP}) is given as [24]

$$I_{ddp} = W \cdot X_{OV} \cdot W_q \cdot N_{DD} \cdot \mu_{drift} \cdot \frac{V_{ddp}}{L_{drift}} \tag{7}$$

$$V_{ddp} = V_{ds} - V_{dp} \tag{8}$$

Here, X_{OV} X_{OV} and W are the current flow under the extended depth of overlap region and width. The V_{ddp} can be determined by the difference in the concentration of drift drain, a channel region, and drift channel length. The depletion region extended due to the operation of a short channel device in the subthreshold region. The V_{di} can be calculated by the drop of potential at the drain region of the depletion region [19] and is shown in Fig. 7.

$$V_{di} = V_{dp} + V_{bidrain} - V_{bisource} - E_{drain} \cdot w_{dep_D}/2 \tag{9}$$

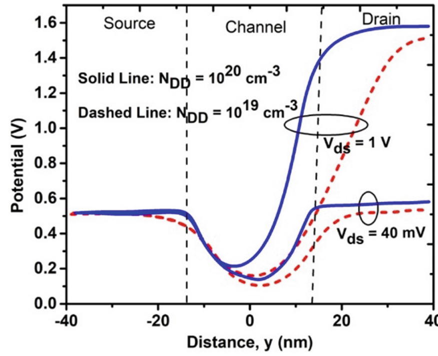

Fig. 7. The potential distribution for various drain side doping concentrations and drain voltages at the middle of the channel (x = 0)

The $E_{drain} \cdot w_{dep_D}/2$ is the potential drop generated additionally due to the small charge density at the drain side of the device.

The modeled and simulated V_{gs}-I_{ds} characteristics are shown in Fig. 8a for V_{ds} = 40 mV and Fig. 8b for V_{ds} = 1V with various channel lengths and drain side doping concentrations. It is observed that the degradation of sub-threshold swing enhanced with both high and low drain voltages for N_{DD} reduction. Also, the effect of drain resistance is drastically improved with decreasing channel length.

Upon validation with 2D numerical simulation at higher voltages, it is observed that the proposed device structure exhibited favorable agreement between simulation results and the model. The modeled and simulated V_{gs}-I_{ds} characteristics for different drain voltages with $L = 20nm$, $t_s = 10nm$, *and* $N_{DD=}10^{18}cm^{-3}$ is shown in Fig. 10(a). Figure 10(b) shows the transconductance characteristics of DG-MOSFET for different values of V_{ds}. The transconductance has no dependency on V_{gs}, which is called quasi-saturation behavior. An abrupt change in g_m has been observed with an increase in the applied voltage V_{ds}.

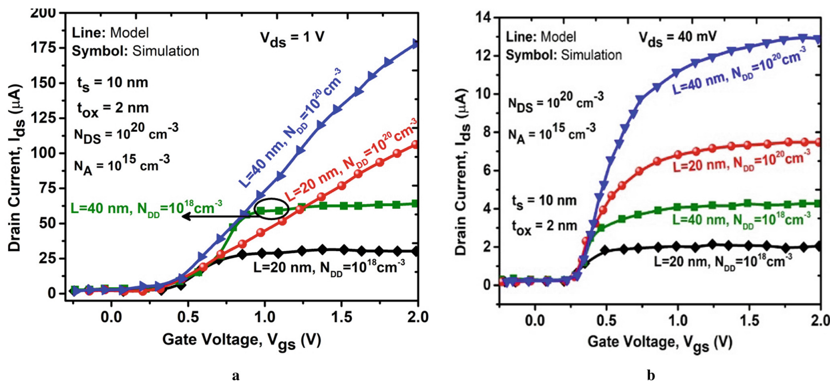

Fig. 8. The modeled and simulated V_{gs}-I_{ds} characteristics at (**a**). V_{ds} = 40 mV and (**b**). V_{ds} = 1 V for various channel lengths and drain side doping concentrations

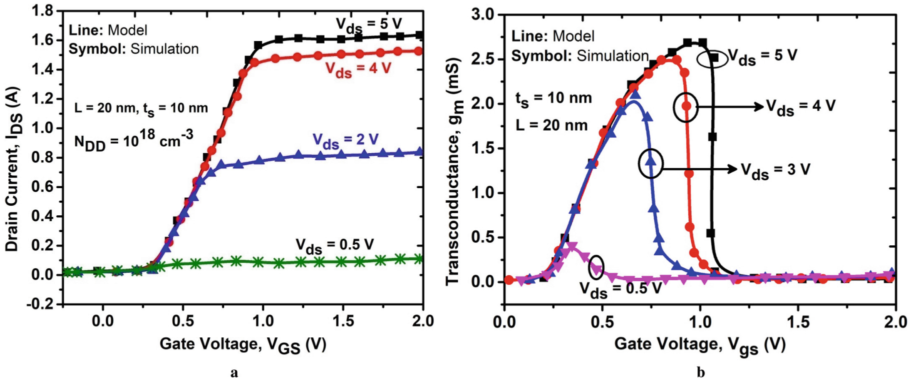

Fig. 9. The modeled and simulated (**a**). V_{gs}-I_{ds} characteristics with different drain voltages with $L = 20nm$, $t_s = 10nm$, and $N_{DD} = 10^{18}cm^{-3}$ and (**b**). Transconductance characteristics with different drain voltages

4 Conclusion

An analytical model with surface potential is developed for high-voltage applications to address the SCEs and drain current of double gate MOSFET. The analytical modeling incorporates various biasing conditions using drift-diffusion approximations. The developed analytical model includes the effects of the high resistive drain region and the impact of the short channel device by considering the potential distribution along the channel. From the results, it is noted that device effects with short channel are reduced explicitly with reducing the small amount of resistive region at the drain side and consequences to affect the distribution of potential in the overlapped drain region. The increasing overlap length can reduce the effects of short-channel devices. The developed analytical model results are justified with numerical simulation results and found in good agreement, and this model can be applied for even changing the device dimensions in the modeling of multigate MOSFETs.

References

1. F. Á. Herrera et al., "Advanced short-channel-effect modeling with applicability to device optimization—Potentials and scaling," IEEE Trans. Electron Devices, vol. 66, no. 9, pp. 3726–3733, Sep. 2019.
2. A. Litty, S. Ortolland, D. Golanski, C. Dutto, A. Dartigues, and S. Cristoloveanu, "Towards high-voltage MOSFETs in ultrathin FDSOI," Int. J. High Speed Electron. Syst., vol. 25, nos. 1–2, p. 1640005, 2016.
3. M. Bawedin, C. Renaux, and D. Flandre, "LDMOS in SOI technology with very-thin silicon film," Solid-State Electron., vol. 48, no. 12, pp. 2263–2270, Dec. 2004.
4. D. Hisamoto et al., "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," IEEE Trans. Electron Devices, vol. 47, no. 12, pp. 2320–2325, Dec. 2000.
5. B. J. Baliga, Fundamentals of Power Semiconductor Devices. Boston, MA, USA: Springer, 2008.

6. M. Bijit Choudhuri, K. Mummaneni, “A new pocket-doped NCFET for low power applications: Impact of ferroelectric and oxide thickness on its performance,"Micro and Nanostructures, vol. 169, 2022, 207360, ISSN 2773-0123, https://doi.org/10.1016/j.micrna.2022.207360.
7. K. Vanlalawmpuia, Suman Kr Mitra, Brinda Bhowmick, “An analytical drain current model of Germanium source vertical tunnel field effect transistor,” Micro and Nanostructures, vol. 165, 2022, 207197, ISSN 2773-0123, https://doi.org/10.1016/j.micrna.2022.207197.
8. I. Ferain, C. A. Colinge, and J.-P. Colinge, “Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors,” Nature, vol. 479, no. 7373, pp. 310–316, Nov. 2011.
9. Neeraj Kumar Niranjan, Paramita Sarkar, Brinda Bhowmick, Madhuchhanda Choudhury, Krishna Lal Baishnab, “Modeling and simulation of 2-D SixGe(1-x) source dual-gate pocket NTFET,” Micro and Nanostructures, vol. 167, 2022, 207237, ISSN 2773-0123, https://doi.org/10.1016/j.micrna.2022.207237.
10. N. Pandey, H.-H Lin, A. Nandi, and Y. Taur, “Modeling of short channel effects in DG MOSFETs: Green’s function method versus scale length model,” IEEE Trans. Electron Devices, vol. 65, no. 8, pp. 3112–3119, Aug. 2018.
11. K. K. Young, “Short-channel effect in fully depleted SOI MOSFETs,” IEEE Trans. Electron Devices, vol. 36, no. 2, pp. 399–402, Feb. 1989.
12. A. Cerdeira, B. Iñiguez, and M. Estrada, “Compact model for short channel symmetric doped double-gate MOSFETs,” Solid-State Electron., vol. 52, no. 7, pp. 1064–1070, Jul. 2008.
13. Verma, Y.K., Gupta, S.K. Center Potential Based Analysis of Si and III-V Gate all around Field Effect Transistors (GAA-FETs). Silicon 13, 1787–1803, 2021.
14. M. Shrivastava, H. Gossner, and V. R. Rao, “A Novel drainextended FinFET device for high-voltage high-speed applications,” IEEE Electron Device Lett., vol. 33, no. 10, pp. 1432–1434, Oct. 2012.
15. A. Litty, S. Ortolland, D. Golanski, and S. Cristoloveanu, “Optimization of a high-voltage MOSFET in ultra-thin 14nm FDSOI technology,” in Proc. IEEE 27th Int. Symp. Power Semicond. Devices IC’s (ISPSD), Hong Kong, 2015, pp. 73–76.
16. R. T. Doria, R. D. Trevisoli, and M. A. Pavanello, “Impact of the series resistance in the I-V characteristics of nMOS junctionless nanowire transistors,” ECS Trans., vol. 39, no. 1, pp. 231–238, 2011.
17. A Baidya, TR Lenka, S Baishya, Linear distortion analysis of 3D double gate Junctionless transistor with high-K dielectrics and gate metals, Silicon, 13 (9), 3113–3120, 2021.
18. ATLAS User’s Manual, Silvaco Inc., Santa Clara, CA, USA, Apr. 2020.
19. G. Amarnath, V. Sharmila, Y. Sreenivasulu, et al. AlInN/GaN HEMT on Silicon Substrate with GD-Field-Plate: Modelling and Simulation of Electric-Field and Breakdown-Voltage Characteristics, Silicon, 2022.
20. G. Amarnath, R. Swain, TR. Lenka, modeling and simulation of 2DEG density and intrinsic capacitances in AlInN/GaN MOSHEMT. Int J Numer Model. 31:e2268, 2018.
21. P. Jacob, R. Xie, M. G. Sung, L. Liebmann, R. T. P. Lee, and B. Taylor, “Scaling challenges for advanced CMOS devices,” Int. J. High Speed Electron. Syst., vol. 26, nos. 1–2, Art. no. 1740001, Mar. 2017.
22. A Gupta, M. Shrivastava, M. S. Baghini, D. K. Sharma, H. Gossner and V. R. Rao, “Part I: High-voltage MOS device design for improved static and RF performance,” IEEE Trans. Electron Devices, vol. 62,no. 10, pp. 3168–3175, Oct. 2015.
23. F. Á. Herrera et al., “Leading-edge thin-layer MOSFET potential modeling toward short-channel effect suppression and device optimization,” IEEE J. Electron Devices Soc., vol. 7, pp. 1293–1301, 2019.

24. P. Kachhawa and N. Chaturvedi, "Simulation of β - Ga2O3 based MOSFETs for Depletion and Enhancement Mode Operation," In Review, preprint, May 2021. doi: https://doi.org/10.21203/rs.3.rs-232838/v111/21.

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