Study and Performance Comparison of Coupled Ring Oscillator

Shirisha Pendyala[1](✉), Mohd. Ziauddin Jahangir[1], and Paidimarry Chandra Sekhar[2]

[1] Chaitanya Bharathi Institute of Technology, Hyderabad, India
[2] Osmania University College of Engineering, Hyderabad, India

Abstract. This work represents the study of the effect of aspect ratio on coupled ring oscillators. The two different coupled ring oscillators i.e.., 3 × 2, 3 × 3 are designed in 90nm CMOS process. The frequency, phase noise and power consumption are measured for different aspect ratios also a comparative study of the above parameters i.e.., frequency, phase noise, power consumption for different coupled ring oscillators are presented.

Keywords: ring oscillator · coupled ring oscillator · low phase noise · effect of aspect ratio

1 Introduction

Ring oscillators are an easiest way for implementing VCO's, VCO's are widely used in PLL's. Which are very important circuits for IC applications. Therefore, ring oscillators enjoy wide demand in IC market. However, one of the major issues that is encountered with ring oscillator is its high phase noise making it least preferred choice in applications like wireless communications.

In recent decade research has been focused on the reduction of phase noise of ring oscillator one of the proposed solutions can be found in the article of Abdul-Latif et al. [1] which describes about developing coupled ring oscillators for reduction of phase noise. Similar work can also be found in reference [2, 3].

Hence, in this work it is proposed to study the performance, specifically the frequency and phase noise of coupled ring oscillators implemented with long channel and variable weight transistors.

It was found that certain weight combinations could yield better phase noise while some other combinations may degrade. Further about this is discussed in sections below. The phase noise of ring oscillator is given by (1) and the frequency of oscillations is given by (2). Where, I_D represents the drain current of short channel devices.

$$L_1\Big/_{f^2}(\Delta f) = 10log_{10}\left[\frac{N\Gamma^2_{rms},\overline{i^2_{n,max}}}{8\pi^2 q^2_{max}(\Delta f)^2}\right] \tag{1}$$

B. Raj et al. (Eds.): ICETE 2023, AER 223, pp. 936–943, 2023.
https://doi.org/10.2991/978-94-6463-252-1_94

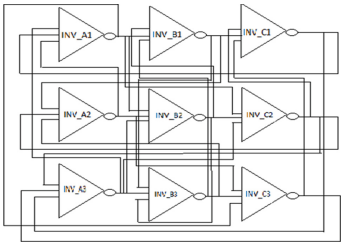

Fig. 1. 3 × 3 coupled ring oscillator.

$$fosc = \frac{I_D}{V_{DD}NC_{tot}} \tag{2}$$

The paper is organized as follows, first we describe the structure of ring oscillators implemented in this article and in the subsequent sections this performance is studied and compared.

2 Coupled Ring Oscillator

Coupled oscillators are a combination of two or more oscillators that are connected to each other in some way. When these oscillators are coupled, they can exhibit resonance, which means that they respond strongly to a particular frequency of excitation one example of a coupled oscillator is a pair of pendulum clocks that are mounted on the same wall i.e., if the coupling between the two clocks is strong enough then they eventually synchronize their swings and start to oscillate in phase with each other. Coupled oscillators can provide lower phase noise while operating at higher frequencies.

2.1 Coupled Ring Oscillator-3 × 3

The structure of 3 × 3 coupled ring oscillator is shown in Fig. 1. Each row consists a 3-stage ring oscillator. Three such stages are cascaded below. Each inverter of three stage ring oscillator contains three inputs, one to connect it in ring oscillator configuration and the other two inputs to provide coupling to subsequent ring oscillators. The three-input inverter is as shown in Fig. 2. Inv1 is the first input that is connected in ring oscillator inv2 and inv3 are two inputs used for coupling. Transistors M1, M2 form the first part of the inverter, M3 and M4 form second part of inverter M5 and M6 form the third part of inverter. Drains of all the inverters are connected to a single output.

2.2 Coupled Ring Oscillator-3 × 2

Similarly, a 3 × 2 coupled ring oscillator is developed as shown in Fig. 3, using two input inverters.

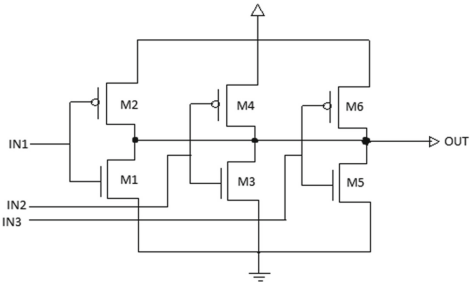

Fig. 2. Circuit of 3-Input inverter for 3 × 3 coupled oscillator.

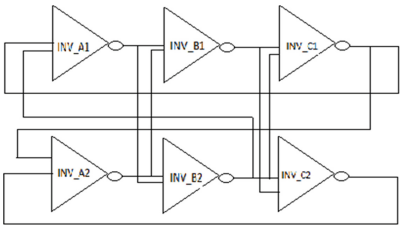

Fig. 3. 3 × 2 coupled ring oscillator.

3 Results and Observations

The oscillator described in Sect. 2 are designed and simulated using CMOS 90nm process in cadence virtuoso. The obtained results are described below.

3.1 Coupled Ring Oscillator 3 × 3

Figure 4 shows the phase noise plot of 3 × 3 ring oscillator for W1 = 600, W3 = 400, W5 = 200 the phase noise obtained is -95dbc/Hz at 1 MHz while operating at a frequency of 2.5 GHz.

The effect of the variation of aspect ratio of different transistors of 3 × 3 coupled ring oscillator is described in Table 1. Maximum frequency is obtained for W1 = 600, W3 = 400, W5 = 200 as shown in Fig. 5 and minimum phase noise is shown in Fig. 6.

3.2 Coupled Ring Oscillator 3 × 2

A 3 × 2 coupled ring oscillator is implemented in cadence virtuoso as shown in Fig. 7.

The effect of the variation of aspect ratio of different transistors of 3 × 2 coupled ring oscillator is described in Table 2. Maximum frequency is obtained for W1 = 600, W3 = 400, W5 = 200 is shown in Fig. 8 and minimum phase noise as shown in Fig. 9.

3.3 Comparison of Power of 3 × 3 and 3 × 2 Coupled Ring Oscillator

The power consumption of both the oscillators are described in Sect. 2 is as shown in the Table 3.

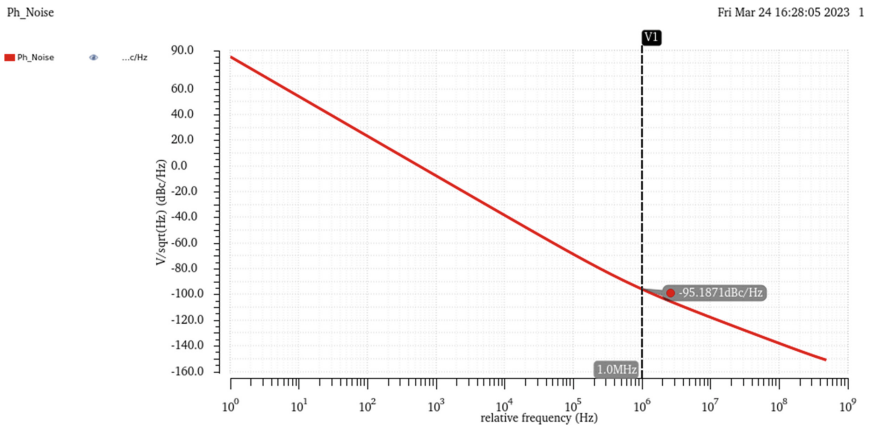

Fig. 4. Phase noise of 3 × 3 coupled ring oscillator simulated in cadence virtuoso.

Table 1. Effect of width of inverter transistor on the frequency and phase noise of 3 × 3 coupled ring oscillator.

Width (n)	Frequency (GHz)	Phase noise (db./Hz)
W1 = 600 W3 = 400 W5 = 200	2.5	-95.18
W1 = 400 W3 = 200 W5 = 600	2.438	-92.96
W1 = 200 W3 = 600 W5 = 400	2.518	Not defined
W1 = 600 W3 = 200 W5 = 400	2.465	-93.08
W1 = 400 W3 = 600 W5 = 200	2.439	-92.96

* All $W_{PMOS} = 2 \times W_{NMOS}$, L = 300n constant for all W1 = M1, W3 = M3, W5 = M5

The power for 3 × 3, 3 × 2 coupled ring oscillator was calculated using cadence virtuoso and are presented in the Table 3 it can be seen that the power consumption increases exponentially with the increase in number of coupled oscillators.

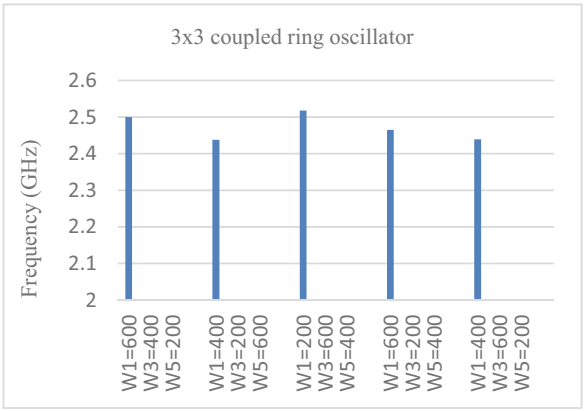

Fig. 5. Effect of frequency of 3 × 3 coupled ring oscillator for different widths.

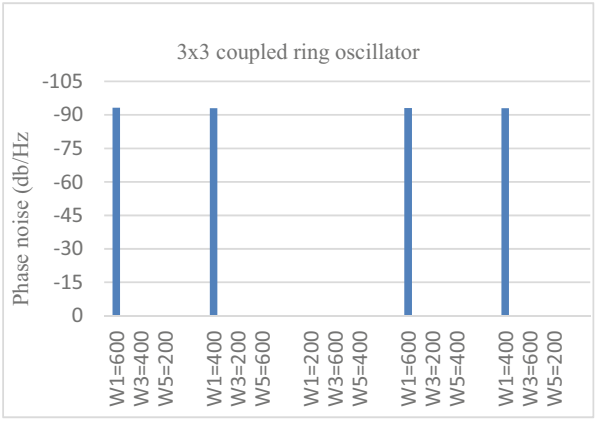

Fig. 6. Effect of phase noise of 3 × 3 coupled ring oscillator for different widths.

4 Conclusion

3 × 3 and 3 × 2 coupled ring oscillator is designed and simulated in 90nm CMOS process. The effect of aspect ratio on frequency and phase noise is studied and power consumptions are compared.

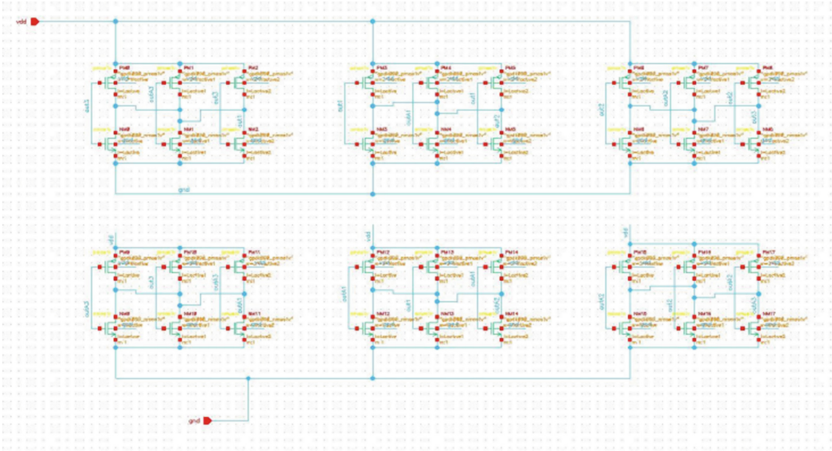

Fig. 7. The 3 × 2 coupled ring oscillator schematic in cadence virtuoso.

Table 2. Effect of width of inverter transistor on the frequency and phase noise of 3 × 2 coupled ring oscillator.

Width (n)	Frequency (GHz)	Phase noise (db/Hz)
W1 = 200 W3 = 600 W5 = 400	2.52	-91.6
W1 = 600 W3 = 200 W5 = 400	2.515	-91.66
W1 = 600 W3 = 400 W5 = 200	2.542	-91.61
W1 = 400 W3 = 200 W5 = 600	2.534	-91.06
W1 = 200 W3 = 400 W5 = 600	2.531	-91.61
W1 = 400 W3 = 600 W5 = 200	2.531	-91.6

* All $W_{PMOS} = 2 \times W_{NMOS}$, L = 300n constant for all W1 = M1, W3 = M3, W5 = M5

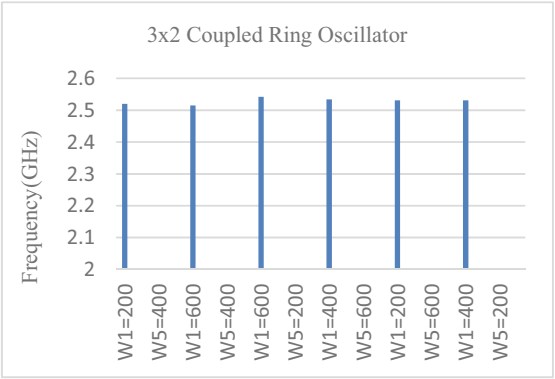

Fig. 8. Effect of frequency of 3 × 2 coupled ring oscillator for different widths.

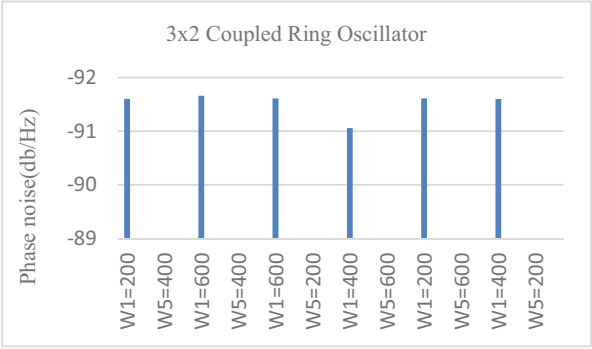

Fig. 9. Effect of phase noise of 3 × 2 coupled ring oscillator for different widths.

Table 3. Power consumption of coupled ring oscillator.

Oscillators	Power consumption
3 × 3 coupled ring oscillator	1.247 mwatts
3 × 2 coupled ring oscillator	366.1 uwatts

References

1. M. M. Abdul-Latif and E. Sánchez-Sinencio, "A 3.16 – 12.8 GHz low phase noise N-Push/M-push cyclic coupled ring oscillator," 2011 IEEE Radio Frequency Integrated Circuits Symposium, Baltimore, MD, USA, 2011, pp. 1–4, doi: https://doi.org/10.1109/RFIC.2011.5940679.
2. A. Elk holy, S. Saxena, R. K. Nandwana, A. Elshazly and P. K. Hanumolu, "A 2.0–5.5 GHz Wide Bandwidth Ring-Based Digital Fractional-N PLL With Extended Range Multi-Modulus Divider," in IEEE Journal of Solid-State Circuits, vol. 51, no. 8, pp. 1771–1784, Aug. 2016, doi: https://doi.org/10.1109/JSSC.2016.2557807.

3. B. Fahs, W. Y. Ali-Ahmad and P. Gamand, "A Two-Stage Ring Oscillator in 0.13-μm CMOS for UWB Impulse Radio," in IEEE Transactions on Microwave Theory and Techniques, vol. 57, no. 5, pp. 1074–1082, May 2009, doi: https://doi.org/10.1109/TMTT.2009.2017246.