Thermoelectric Cooler Failure Prevention Caused Due to CTE Mismatch by FEA Based Solder Layer Material Selection

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Abstract. Thermoelectric coolers (TEC) work on the principle of Peltier effect and are widely used in semiconductor industry to cool the components placed inside packages. The present work examines the effect of coefficient of thermal expansion (CTE) on the strength of solder joints of TEC. Due to difference in the CTE's of TEC materials, uneven expansion and contraction of solder layers occurs leading to high stress levels in n-p semiconductors. Two solder layers are used in TEC to attach ceramic plate to heat sink at hot and cold sides. Finite element analysis (FEA) is performed for different solder materials to investigate the failure of n-p semiconductors. This allows selecting the most appropriate material to improve the design of TEC and thus prevent failure. To prevent dependency on single source and supplier, three different materials are analyzed namely Indium (In99.9), Indium Bismuth (In-50Bi) and Tin Bismuth (Sn42Bi58). Based on performance criteria, two of them are shortlisted with an aim to improve the TEC design. Solder junctions between ceramic plate and heatsink are important to connect both the parts. CTE mismatch between solder layers causes high stress in n-p semiconductor, leading to TEC failure. FEA analysis performed under thermal shock load over 0–125 C helps in selecting the better solder material to reduce the testing time with improved TEC design.

Keywords: Peltier effect · CTE · TEC · Solder material · Thermal shock

1 Introduction

Thermoelectric cooler is solid-state heat pump used to transfer heat from one side to another. TEC uses n and p type semiconductors which is made up of bismuth telluride (Bi2Te3) material. Semiconductors are soldered between two ceramic plates electrically in series and thermally in parallel. Thermoelectric cooler used in semiconductors industry to dissipate the heat from the high temperature source to low temperature sink. Strength evaluation is very important part of the product and due to involvement of different materials in TEC construction, it becomes more complex to analyze the TEC assembly. TEC installed in various semiconductors packages in which temperature ranges are extreme. In the present work single stage TEC is considered with the thermal shock load

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from 0 °C to 125 °C. TEC consist of five different layers or blocks of material. The first one is the TEC mount, on which complete assembly is mounted followed by mounting of heat sink, solder layer, ceramic plate, connector pads and n-p semiconductors. All these layers are soldered with each other. For different material layers the coefficient of thermal expansion is also different, due to this CTE mismatch occurs which often results in high stresses, leads to the failure of product. It becomes important to select the solder material such that the connected parts don't experience high stresses during actual working. Effective solder materials such as Indium, Indium-Bismuth and Tin-Bismuth materials are analyzed with the help of commercially available FEA software Abaqus, to predict the suitable solder material, which can sustain the thermal shock load of 0 °C to 125 °C. Pure Indium (99.9) and Indium based solders shows the characteristics of low melting point, softness, and ductility [1]. Due to excellent ductility Indium is good choice to join the materials exhibits different CTE's. Indium Bismuth solder alloy material is also common solder material. Addition of Bismuth makes the material brittle but increases the strength of the alloy. Different material combinations of Indium Bismuth alloys are tested, and stress-strain data revealed that the addition of bismuth makes the alloy brittle [2]. In-Bi alloy shows anisotropic CTE properties and have different values for parallel ($\alpha\|$) and perpendicular directions ($\alpha\perp$) [3]. In-Bi alloys with low melting temperatures are also suitable for the bendable substrates of polypropylene (PP) and poly-(methyl methacrylate) (PMMA) [4]. It has also been found that by increasing the Indium content in Indium-Bismuth alloys, helps to reduce the melting temperature of the alloy [5]. Indium based solders observed failures due to stress overload or unidirectional creep [1]. Therefore, other than Indium based solders Tin-Bismuth solders are also considered for the soldering application. Tin-Bismuth solder alloy has high strength compared to Indium based solder alloys, but ductility will be less as compared to indium-based solder alloys [6]. Rapid decrease of Tin-Bismuth alloys young's modulus over 80^{O}C is observed [7]. Tin-Bismuth solder alloy having very good crystal structure, microstructure, and low melting point [8]. Different works carried out to predict the cooling of thermoelectric cooler [10] based on FEA simulation. Practical assessment of thermoelectric cooler used in trucks and its FEA simulation is carried out to check the performance of the device [11]. Design optimization also carried out for TEC module related to n-p semiconductors and its soldering [9]. In the previous works coefficient of performance was studied and the optimization, but the solder material selection based on CTE is not taken into consideration. In the present work importance of solder material CTE is taken into consideration as well as its effects on TEC is considered. New product development requires continuous improvement and FEA based software's provide a reliable solution to improve the product. TEC is a complex structure and requires accuracy before proceeding to change in any material related area. TEC solder reliability is an important criterion because TEC solder failure results in complete electronic package failure. FEA based solution leads to know the suitable material for the TEC solders. Three different materials are considered, and the detailed finite element modelling is carried out to predict the solder behavior. Indium based, and Tin Bismuth solder layers are modelled and evaluated for the thermal shock load of 0 °C to 125 °C.

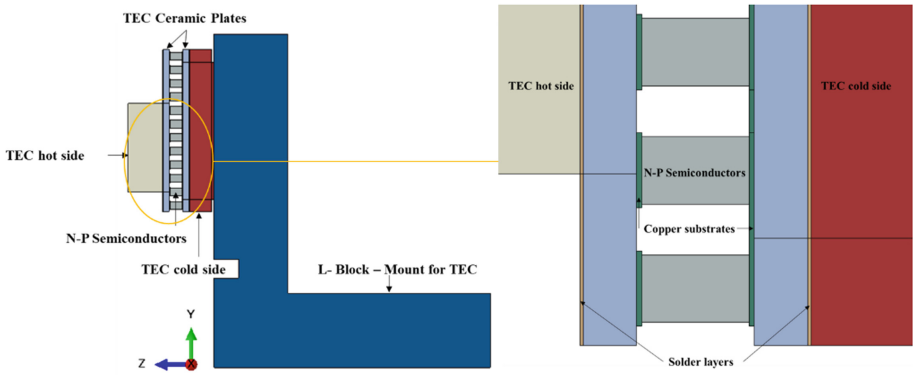

Fig. 1. TEC CAD data used for FEA analysis with enlarged view of solder layers

2 FEA Analysis Procedure

2.1 CAD Model

To evaluate the suitable solder material for TEC, FE model setup is prepared in Abaqus CAE software as shown in Fig. 1 TEC is mounted on the L shaped TEC mount and mount is screwed to the adjacent components. To simplify the solution and to save the computational time only the TEC and TEC mount is taken into consideration. A brief introduction of the TEC parts is given in the Fig. 1.

2.2 Material Used for FEA Analysis

For most of the materials only linear elastic material properties are considered. For solder layers, three different solder materials are used for performing FEA simulation. For detailed solder layer modelling stress-strain curves (elastic-plastic material data) are required to get more realistic results, as shown in Fig. 2. Simulations are performed with materials listed in Table 1. Solder material properties are listed in Table 2.

3 Loads and Boundary Condition

Temperature shock load of 0 °C to 125 °C applied on the complete assembly as shown in Fig. 3. Corner vertices of L block are fixed in all degrees of freedom as shown in Fig. 4.

4 FE Analysis Results and Discussion

After performing the FEA simulation, results on n-p semiconductors are listed in Table 3. It has been observed that n-p semiconductors are sensitive to the solder layers, although there is no direct physical contact between the solder layers and n-p semiconductors.

By using Indium as solder layer material, stress observed over n-p semiconductors are below the 40 MPa which is the allowable stress limit of the material. The stress

Table 1. Material properties used for FEA analysis

Part	Material	Young's Modulus (MPa)	Poisson's Ratio	Coefficient of thermal expansion (mm/mm per K)
L block Copper Substrates	Oxygen Free high conductivity Copper (OFHC)	117000	0.343	1.70E-05
TEC hot side	Copper Tungsten (W90Cu10)	340000	0.280	6.50E-06
Ceramic plate	Aluminium Oxide (Al2O3)	300000	0.210	8.10E-06
n-p semiconductors	Bismuth Telluride (Bi2Te3)	50000	0.220	1.29E-05
TEC cold side	Copper Molybdenum (Cu30Mo70)	210000	0.290	8.00E-06

Table 2. Solder material properties used for FEA analysis

Part	Material	Young's Modulus (MPa)	Poisson's Ratio	Coefficient of thermal expansion (mm/mm per K)
Solder Layers	Indium (In99.9)	12740	0.450	2.48E-05
	Indium Bismuth (In-50Bi)	12598.2	0.320	$\alpha\parallel$ = -8E-05, $\alpha\perp$ = 6E-05
	Tin Bismuth (Sn42-Bi58)	39000	0.350	1.67E-05

and strain distribution for Indium material solder layer and the n-p semiconductor stress distribution is shown in Fig. 5.

When compared to Indium, Indium-Bismuth alloy has better yield strength. Therefore, the iteration performed with In-Bi material solder layer and the stress results for solder layer and n-p semiconductors are shown in Fig. 6. It has been observed that with better yield strength the solder layer stress is below the allowable yield stress limit of 53 MPa. But the stress induced on n-p semiconductors are above the allowable stress limit of 40 MPa.

Iteration performed with Tin-Bismuth alloy material. Tin-Bismuth alloy has modulus of elasticity approximately 2.5 times that of In and In-Bi alloy. Yield strength of Sn-Bi alloy is 3 times the yield strength of In-Bi alloy and the CTE is lower than both In and In-Bi material. FEA results for Sn-Bi material are shown in Fig. 7.

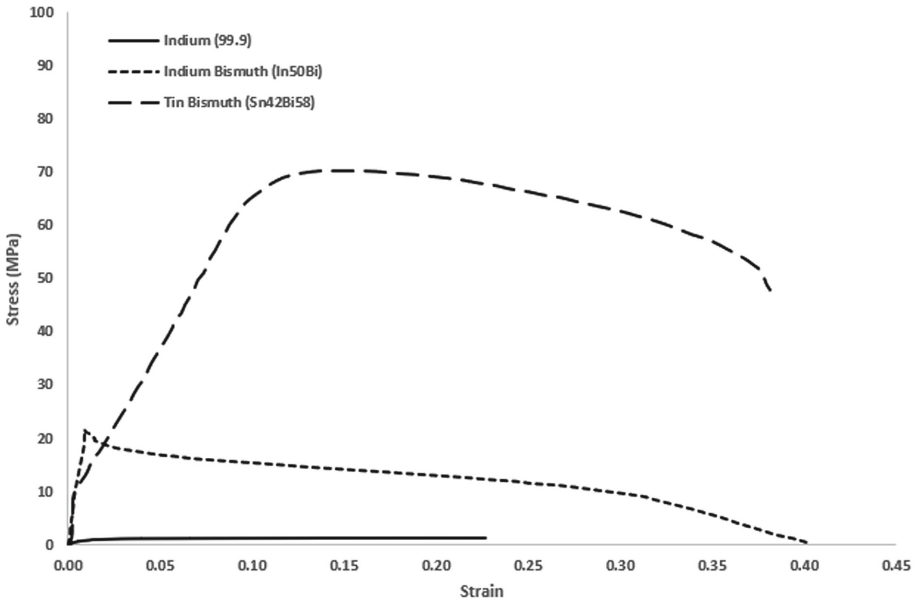

Fig. 2. Solder material stress -strain data used for FEA analysis

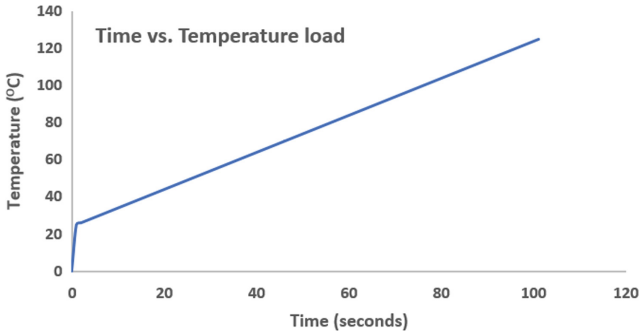

Fig. 3. Temperature shock load used for FEA analysis

FEA results for In-Bi and Sn-Bi solder layer material shows low stress on solder layers and high stress on n-p semiconductor and therefore the materials are not suitable for the solder layer application.

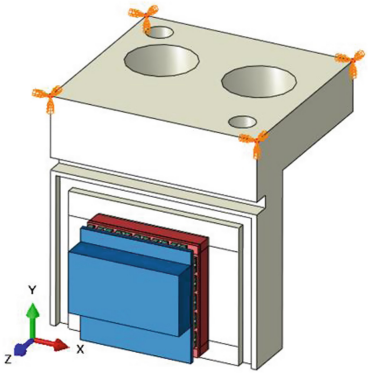

Fig. 4. Fixed boundary condition for FEA analysis

Table 3. FEA simulation stress results on n-p semiconductors

Solder material	Stress induced on n-p semiconductors (MPa)	Stress above yield stress limit of 40 MPa	TEC (Safe / Not safe)
Indium (In99.9)	36	No	Safe
Indium Bismuth (In-50Bi)	53	Yes	Not safe
Tin Bismuth (Sn42-Bi58)	50	Yes	Not safe

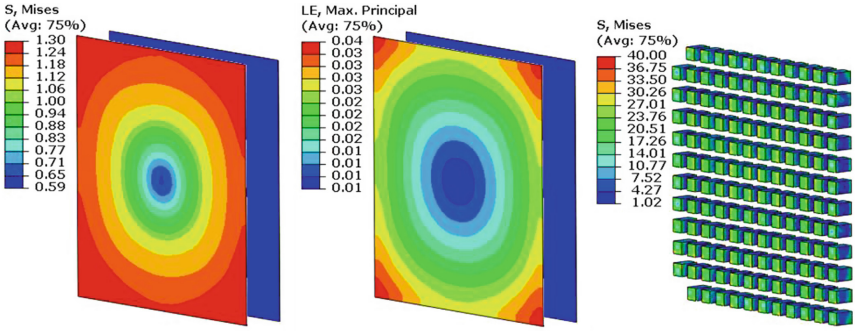

Fig. 5. Indium layer solder material stress -strain and stress on n-p semiconductors

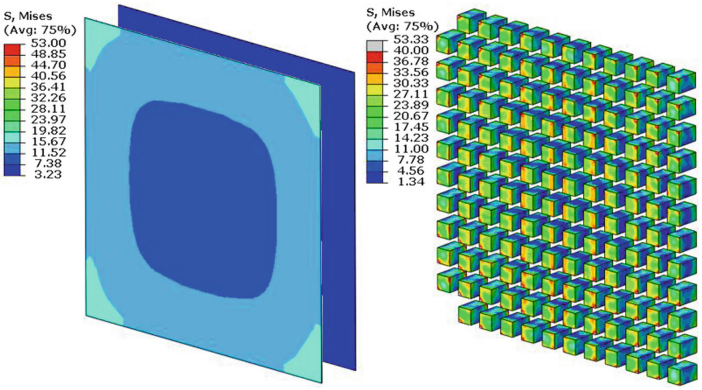

Fig. 6. Indium-Bismuth solder material stress and stress on n-p semiconductors

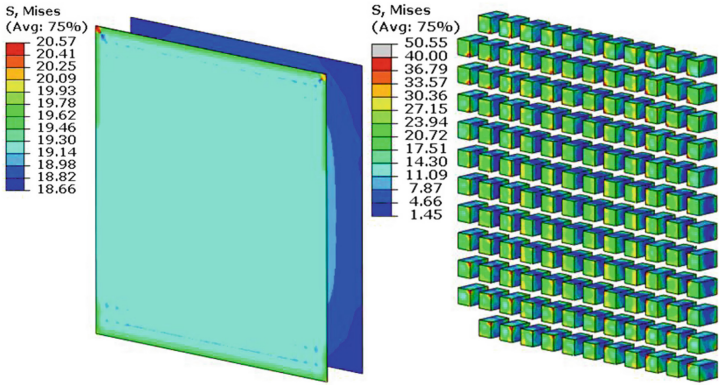

Fig. 7. Tin-Bismuth solder material stress and stress on n-p semiconductors

5 Conclusion

By performing FEA analysis for different solder layer materials, it has been observed that the solder layer plays an important role in the safety of TEC n-p semiconductors. Solder layers strength is not the only selection criteria, but the solder material selected such that the solder expansion would not exert high stress on semiconductors. Based on performed FEA iterations it has been observed that the Indium material is best suited for the solder layer requirement. Therefore, despite of low elongation and low strength than InBi and SnBi alloys, Indium material fulfills the solder material requirement. Therefore, the amount of expansion indium solder provide is enough to withstand the applied thermal shock load.

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