Power Optimized Carry Select Adder Using Reversible Logic Gates

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Abstract. Reversible logic is playing an important role for low power computations. In today's trend it is essential to optimize the power for portable devices which can be achieved through reversible logic computation. The low power computations can be performed using Reversible Logic Gates (RLG) which forms the fundamental blocks of the digital logic circuits. One of the important metric's in the integrated circuit design is Power dissipation. The Digital circuits constructed using irreversible conventional logic gates dissipates more power when compared to the circuits with Reversible Logic Gates. Adders are the fundamental components which performs the basic addition operation in many complex calculations. Among various adders available Carry select Adder being the fastest adders used to perform the basic arithmetic Addition operation in many data processing processors. Thus it is essential to design a power efficient Carry select Adder(CSA) in power constraint and high speed design applications. In this paper both conventional and reversible CSA is modelled using Verilog HDL and it is synthesized by using XILINX VIVADO EDA tool.

Keywords: Reversible gate, Reversible, Carry select Adder, Adder, HDL VERILOG.

1 Introduction

In Electronic Design Automation Industry Reversible logic computation is playing a prominent role to design a low power, energy constraint, loss less information for an efficient design. This prevents energy loss which occurs due to the bit loss during calculations. There is probability of information loss during computations due to which there is a dissipation of heat which causes the damage to the system. There is an increase in the above discussed factor which is not inevitable in designing an effective electronic circuit as the power is the most important considering factor for the portable devices. According to the Launder's principle [1-2], KTln2 heat is dissipated for a single bit loss.

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The major challenges in designing the electronic devices are the power efficient, miniature size and improving the speed without any performance degradation has to be considered. Scaling of a device is necessary to design Very large scale integrated circuits so as to incorporate a large number of transistors to increase the computational speed of a device to build more complex circuits to increase the functionality of the design without any performance degradation. But scaling of a device consists of both advantages as well as disadvantages when necessary techniques are used for scaling.

2 Reversible Logic

The reversible computation is achieved using reversible gates that comprises of quantum gates. All quantum gates are reversible gates. In a Reversible logic[3] gate, a unique output is produced for every input which result in no information is loss during computations. Reversible gates are used in reversible computing which forms the basic blocks for combinational circuits[5] consumes low power. The quantum gates are reversible gates. A reversible gate if it has the following specifications: The gate should have equal number of inputs and outputs. Feedback is not allowed in reversible computing. Fan out is not allowed. The Design parameters used to design the reversible gates are: One or more inputs are made constant to get the necessary output known as constant input. The total count of the 1*1 size 2*2 size quantum gates used to construct the reversible logic gate is known as its quantum cost. If any of the output which is not required in further computation is known as the garbage output. Quantum gates are reversible gates which consist of elementary quantum gates. NOT gate, CNOT gate, SWAP gate, controlled v-gate and controlled v+ gate are the basic quantum gates. The BUS gate[1] performs all the basic, universal(NAND &NOR)and special (XOR)logical operation. A RLG is decomposed into quantum circuit.

3 The Proposed Framework For CARRY SELECT ADDER

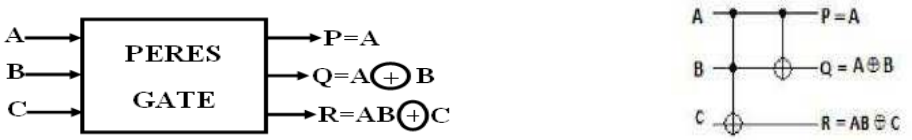
The proposed BUS (basic, universal, special) gate has three inputs and three outputs. It comprises of 3 Peres gates and 3 Feymann gates. The design metrics of the BUS RLG are the Quantum cost is 15, constant input and the garbage output is one. If the input is constant i.e., c=1, NAND and NOR gates are performed. If c=0, AND and OR operation is performed. If b= 1 XOR operation is performed.

(a) (b)

Fig. 1 (a). Block Diagram **(b)**. Quantum Circuit**.**

3.1 PERES GATE

It is a 3*3 reversible gate consists of three inputs and three outputs as shown in Fig. 3. Its Quantum cost is 4.



(a) (b)

Fig. 2 (a). Block Diagram **(b)**. Quantum Circuit.

3.2 FEYMANN GATE

A 2*2 reversible gate which consists of two inputs and outputs shown in Fig. 5. The quantum cost is 1.

(a) (b)

Fig. 3 (a). Block Diagram **(b)**. Quantum Circuit

Carry Select Adder

As the prominence for high performance processor is growing, there is an increasing necessity to improve the data path unit performance [8]. Addition is the basic and frequently used arithmetic operation in most of the complex calculations and the

performance of the VLSI processor is mostly affected by the speed of the adder[4]. Thus a high performance and power constraint adder plays a prominent role in the hardware circuits[6].

Operation of Carry Select Adder is explained with both conventional logic gates as well as the proposed reversible BUS gate. The proposed RCSA is synthesized using Xilinx Vivado EDA tool.

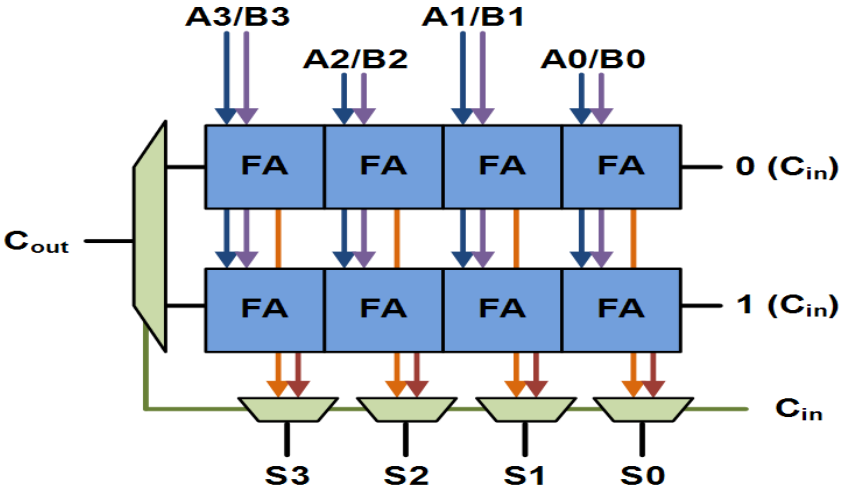


Fig. 4. Block Diagram of Carry Select Adder

A Carry select Adder typically has two main components:

Carry Select Blocks: Each block handles a group of bits and computes two possible sum values and carry-out values. one assuming the carry-in as 0, and the other carry-in as 1.

Multiplexers: After computing both the results, a multiplexer selects the correct result based on the actual carry input [10].

A Conventional Carry select Adder is built using irreversible logic gates which dissipates energy in the form of heat due to information loss according to the launder's principle.

A Reversible Carry select Adder is implemented with the proposed BUS gate. Reversible logic gates consume much less power than conventional gates, especially when designed to minimize switching activity[9]. Ideally reversible logic, exhibits no energy dissipation associated with logical operations. In practical designs, power consumption isless because reversible gates generate much less heat and reduce unnecessary switching.A Reversible

CSA offers significant power-saving advantages, making it ideal for low-power, energy-constrained applications like mobile devices, IoT and DSP systems[7].

4 Experimental Results And Analysis

The implemented design is simulated and synthesized and various reports namely power, utilization, implementation and timing of the conventional and reversible carry select adder is shown below. From the obtained simulation reports it is evident that the reversible carry select adder consumes less power compared to conventional carry select adder.

Fig. 5. Waveform of Conventional Carry Select Adder

The Fig. 5 represents the waveforms of conventional CSA with inputs a is equal to 8,b is equal to 2 with cin 1 gives the result sum is equal to 11 with cout 0.

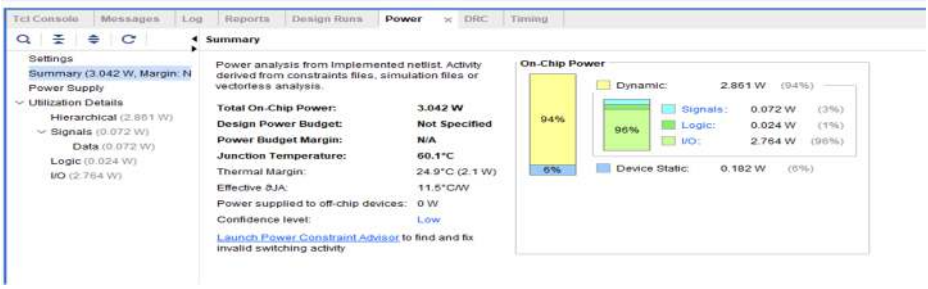


Fig. 6. Power report of Conventional Carry Select Adder

Fig. 9. denotes the total on chip power of a conventional carry select adder is 3.042 W.

Fig. 7. Utilization report of Conventional CSA

The Fig.7 denotes the utilization report of a conventional carry select adder more than reversible carry select adder.

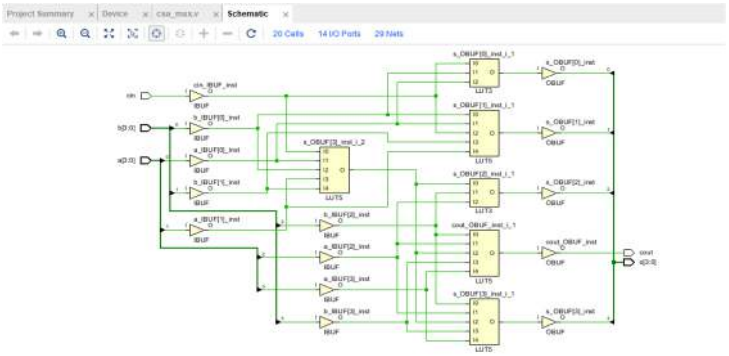


Fig. 8. Schematic view of Conventional Carry Select Adder

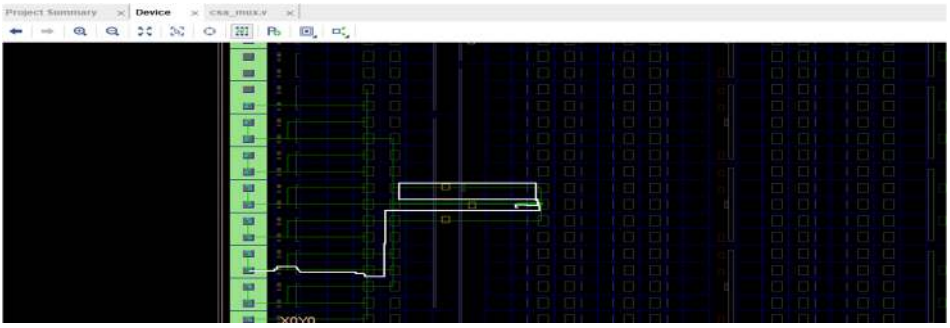


Fig. 9 Implementation view of the Conventional Carry Select Adder

ports | Design Runs | Power | DRC | Timing | Utilization

Unconstrained Paths - NONE - NONE - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	De
Path 1	∞	4	3	3	a[1]	cout	8.172	4.253	3.919	∞	input port clock	
Path 2	∞	4	3	3	a[1]	s[3]	7.800	4.028	3.772	∞	input port clock	
Path 3	∞	4	3	3	a[1]	s[2]	7.737	3.986	3.751	∞	input port clock	
Path 4	∞	3	2	3	a[0]	s[0]	7.143	3.627	3.516	∞	input port clock	
Path 5	∞	3	2	2	a[1]	s[1]	6.943	3.674	3.269	∞	input port clock	

Fig. 10. Timing report of Conventional Carry Select Adder

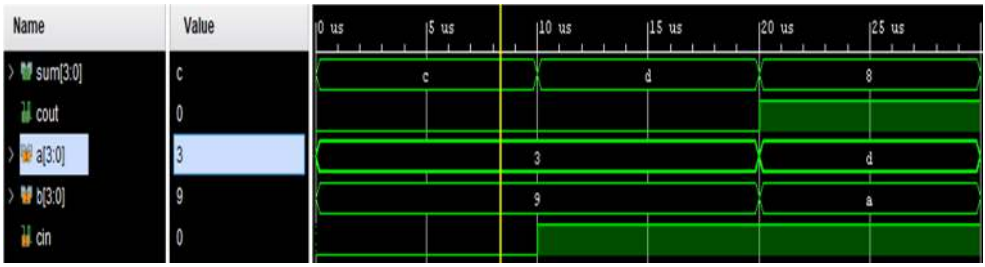


Fig. 11. Waveform of Reversible CSA

The Fig.11 represents the simulation report of reversible carry select adder with inputs a is equal to 3, b is equal to 9 with cin 0 gives the result sum is equal to 12 with cout 0.

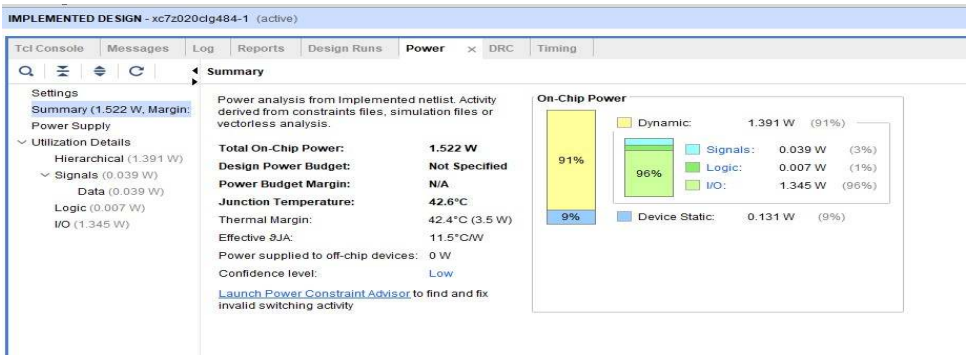


Fig. 12. Power report of Reversible Carry Select Adder

The Fig. 12. denotes the total on chip power of reversible carry select adder is 1.522W which is the summation of dynamic and static power.

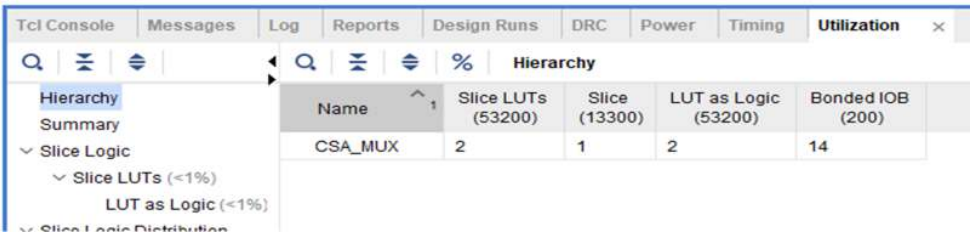


Fig. 13. Utilization report of Reversible Carry Select Adder

The Fig.16 denotes the utilization report of a reversible carry select adder less than conventional carry select adder.

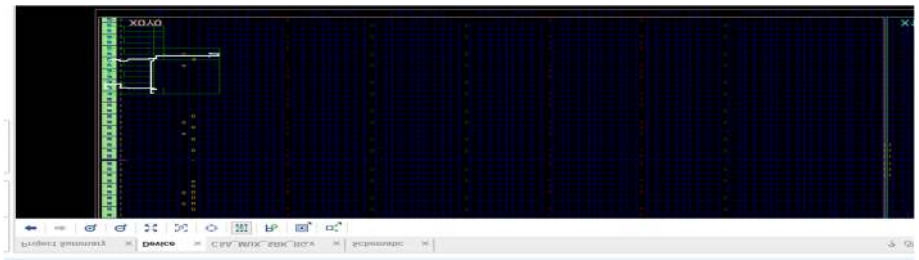
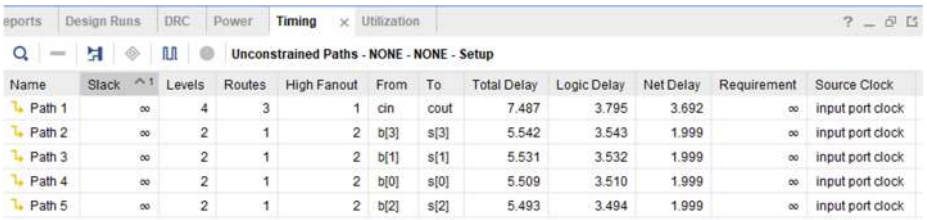


Fig. 14. Implementation of Reversible Carry Select Adder

In Fig.14 Implementation of reversible carry select adder is represented.



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	4	3	1	cin	cout	7.487	3.795	3.692	∞	input port clock
Path 2	∞	2	1	2	b[3]	s[3]	5.542	3.543	1.999	∞	input port clock
Path 3	∞	2	1	2	b[1]	s[1]	5.531	3.532	1.999	∞	input port clock
Path 4	∞	2	1	2	b[0]	s[0]	5.509	3.510	1.999	∞	input port clock
Path 5	∞	2	1	2	b[2]	s[2]	5.493	3.494	1.999	∞	input port clock

Fig. 15. Timing report of Reversible carry select adder

The Fig.15 is the Timing report of a reversible carry select adder.

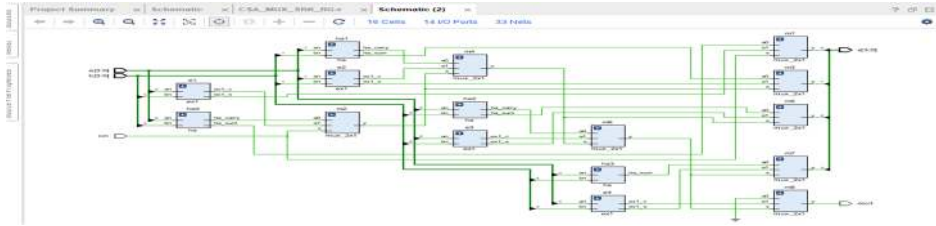


Fig. 16. Schematic view of Reversible carry select adder

Table.1 Comparison between conventional and reversible CSA

TYPE	POWER(W)	DELAY(ns)
Conventional CSA	3.042	8.172
Reversible CSA	1.522	7.487

5 Conclusion

From the results, we can say that the reversible gates can be replaced with conventional logic gates to design digital logic circuits. There is a power saving of 49.96% reversible CSA compared to that of the conventional CSA. The delay is also calculated for conventional CSA and Reversible CSA which is 0.685ns less for Reversible CSA. The number of slice LUTs are represented which is not same for both. The above CSA can be extended to implement 8, 16, 32 bits also. Thus the reversible gates are analyzed and implemented which helps in building the various arithmetic circuits and can be implemented for low power computation techniques in various fields.

Disclosure of Interests. The authors have no competing interests to declare that are relevant to the content of this article.

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