Performance Analysis of Differential and Single Ended SRAM Cells in Low Power Smart System Applications

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Abstract. Smart systems, including IoT devices and biometric authentication platforms performance, depend on internal memory architecture for its high-speed, low-power operation and reliable data storage. As modern CMOS technology advances, minimizing leakage current and ensuring data retention have become critical challenges. This research investigates and compares the delay, power dissipation, and noise margin of 6T (differential mode) and 8T (single-ended) SRAM cells. While 6T SRAM remains the industry standard for general-purpose memory, 8T SRAM demonstrates superior read stability and reduced leakage, making it suitable for low-power applications. Comparative analysis reveals that the 8T SRAM offers a higher read noise margin than the 6T cell. Read delay of 8T and 6T 2.3ns and 23.4ps respectively. The write delay for the 6T cell is 481ps, compared to 1.8ns for the 7T cell. Simulations were conducted using 90nm CMOS technology across a supply voltage range of 300mV to 1Volt. In this work, we consider two methods for calculating stability: the Butterfly Curve and the N-Curve method. This study highlights the potential of SRAM Memory designs in shaping future technologies like IoT, AI accelerators, and low-power smart systems by optimizing critical parameters such as power consumption, security, and silicon area.

Keywords: SRAM, Low Power Design, Internet of Things, System on Chip, Delay, Static Noise Margin, Security.

1 Introduction

Static random-access memory is a primary building block of modern digital systems, and its importance will continue to rise with the increasing number of intelligent systems. Designing and developing portable gadgets for future applications, like smart systems, wearable technology, and the Internet of Things (IoT), has attracted much focus. These kinds of applications require semiconductor memory with low power consumption [1]. Memory requires up to a large section of a SoC, which impacts overall system performance [2]. The SRAM cache memory is more suitable for SoC applications because of its high speed and low power dissipation. Therefore, portable devices and biomedical equipment employ SRAM. Since the cache memory occupies more than half of the processor's chip area, leakage power is the primary cause of processor power dissipation [3]. CMOS devices have scaled down in recent years to achieve higher speed and lower power. The transistor size and supply voltage are two critical factors influencing this process. Reducing the supply voltage helps lower power dissipation. However, optimal performance also requires a reduction in the threshold voltage. Unfortunately, as the threshold voltage drops, the sub threshold

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leakage current rises. This causes more static power to be lost, which is mainly due to the leakage current [4]. Additionally, the scaling of supply voltage has negatively impacted efficiency and other design parameters. To address these challenges, researchers have proposed various design solutions that aim to minimize power consumption, enhance read stability and write ability, and improve overall efficiency. This paper presents an in-depth evaluation of standard 6T, 7T, and 8T SRAM cells. Among the several SRAM designs, 6T and 8T are most often used. Each has certain advantages, suitable for particular applications. The 6T SRAM cell is well-known for its simple structure and lower space, while the 8T cell is preferred for improved read stability with low power. The primary difference between them is the number of bit lines used. The 6T cell uses a double-bit line, while the 7T and 8T cells use only one bit line. 8T SRAM cells provide improved read stability using the read decoupling technique [5].

2 SRAM Cell

The design of the SRAM Memory cell allows it to achieve good write ability while maintaining a stable read operation. The standard 6T SRAM cell fulfills these requirements by suitable transistor sizing. According to the Bit cell ratio (β) and pull up ratio (PR) sizing takes place. In this paper, the simulation is done with β=1.33 and PR =0.6. The separation of read and write operations in single ended SRAM cells further enhances stability by reducing disturbance during read operation.

2.1 Differential Type (6T) SRAM Memory Cell

Fig. 1. shows a conventional 6T. It has two cross-coupled inverters, which are used to store data, and two access transistors, which connect the Q and QB nodes to the bit lines during the read and write operation. Due to its direct connection, an SRAM cell experiences lower read stability. The read stability and write margin are the major challenges at a lower supply voltage. The word line (WL) activates the access transistors during the write operation, and the bit lines on the Q and QB nodes apply data [6].

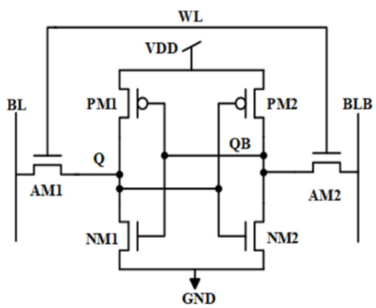


Fig.1. Differential Type 6T SRAM Memory Cell

2.2 Single Ended 8T SRAM Memory Cell

The 8T SRAM Memory Cell decouples the read operation by adding two more transistors for an individual read path. Since the read current does not directly impact the storage node, this design enhances read stability and lowers the possibility of data flipping. Liang et al. [7]. As shown in Fig. 2. popular read buffer 8T cell, the write operation of this cell is comparable to 6T, as they share a similar write mechanism cell. This similarity allows the cell to achieve good writing ability without introducing delay. The read operation in 8T cell performed by the activating RWL line in place of word line (WL). Whenever read disturbances are absent; a much higher SNM is produced by two cross-coupled inverters.

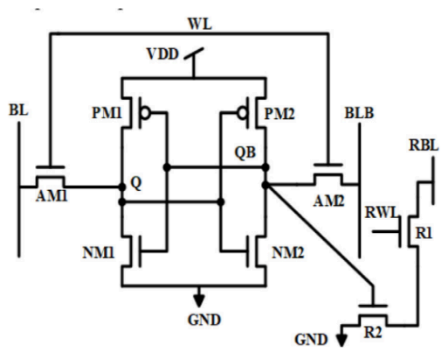


Fig. 2. Single Ended 8T SRAM Memory Cell

2.3 Single Ended 7T SRAM Memory Cell

Fig. 3. illustrates the 7T SRAM Memory cell. A standard 6T memory comprises two nodes, (Q and QB) for storing data. Control signals are utilized to execute read and write operations. In a write operation, the signal WWL controls the gate while the WBL is applied to the drain/source of a transistor (M7). During the read operation, the RBL signal is connected to the drain/source of a transistor (M5) while the RWL Signal regulates the transistor gate. To ensure that the stored data is not disrupted during the read operation, the read access transistors (M5 and M6), are designed to be isolated from the node Q to prevent data flipping at the node [8].

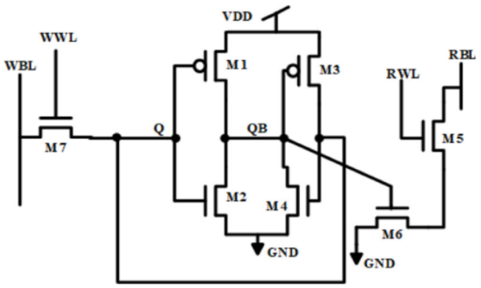


Fig. 3. Single Ended 7T SRAM Memory Cell

3 Simulation Results

The performance parameters of the 6T, 7T, & 8T SRAM cells are compared in this section with a focus on parameters like stability, delay, power consumption, and leakage. This analysis evaluates stability, reliability, SNM, and power consumption during different conditions.

3.1 Read Delay and Power Consumption

The difference between the word line and bit line (BL or BLB) at 50%of the supply voltage is used for calculating the SRAM cell delay. The delay has an impact on the circuit's speed. The SRAM cell's speed will drop if the delay is increased. Table 1 summarizes the power and read delay simulation results at low voltage (300mV).

Table 1. Read Delay and Power Consumption at 300 mV

SRAM Cell	Read Delay (pS)	Read Power (nW)
6T	*23.2*	1.6
7T	*81.1*	2.7
8T	*54.4*	2.7

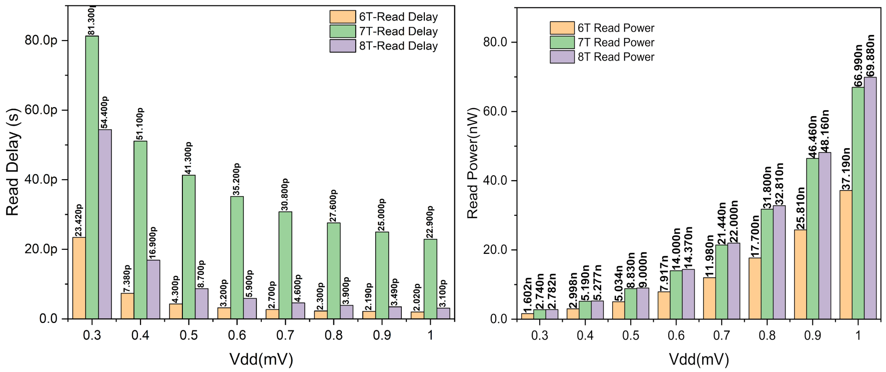


Fig. 4. Read Delay and Power Consumption

This result shows that the 7T Cell Exhibits a higher read delay compared to the other cells, likely due to its more Complex Circuit design and additional components involved in its operation. Lower delay provides high stability. While this higher delay may be undesirable, it is frequently accompanied by greater stability, making the 7T cell an acceptable choice for applications where reliability takes priority over speed. The read power of 8T and 7T Cell is higher than 6T cell primarily due to their additional transistor and circuit. These extra components increase the dynamic power consumption during read operation.

3.2 Write Delay and Power Consumption:

The delay of an SRAM cell is an important performance parameter that refers to how long it takes the cell to complete a write operation. The Write Delay is the time required to overwrite the data in the cell by changing the bit lines to the desired values. In Table 2 summarizes the power and write delay data.

Table 2. Write Delay and Power Consumption at 300mV

SRAM Cell	Write Delay(ps)	Write Power (nW)
6T	*482ps*	5.6
7T	*1.5ns*	3
8T	*482ps*	6.1

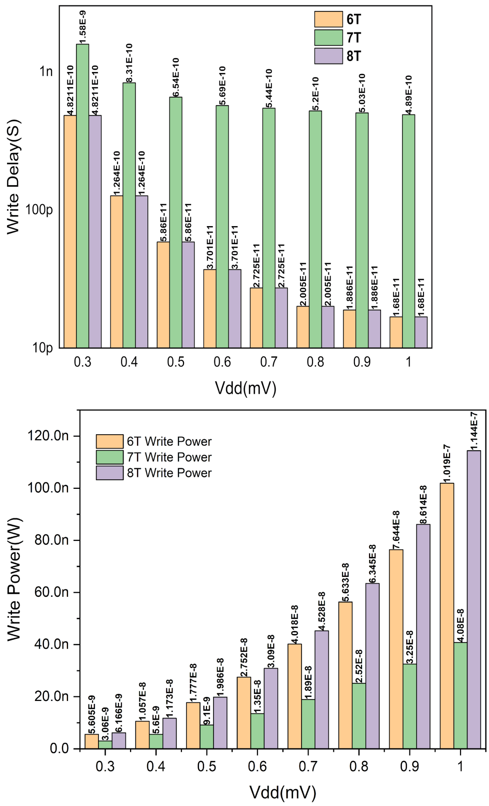


Fig. 5. Write Delay and Power Consumption

This result indicates that the standard 6T and 8T SRAM cells have a lower write delay compared to the 7T SRAM cell because they use a single bit line for the write operation, which simplifies the process and reduces delay. The write delay of 6T and 8T SRAM is nearly identical since their write operation is similar. On the other hand, the write power of the 6T SRAM cell is higher than that of the 7T SRAM cell due to increased switching activity and higher power dissipation. For low-power applications, such as IoT and embedded systems, where energy efficiency is crucial, the 7T SRAM cell is a better choice due to its lower write power consumption, making it suitable for systems with Low power.

3.3 Leakage Power

When the SRAM is not in use or has no switching condition, current leakage causes power loss or dissipation. In low power and high performance applications, leakage power must be managed. Table 3 shows the leakage power dissipation of 6T, 7T & 8T and observed that 7T SRAM cell is lowest leakage power. The reduced leakage can considerably improve power efficiency, mainly in standby mode, where leakage current is a major contributor to power loss. This makes the 7T SRAM cell more suitable for low-power applications, such as IoT devices, wearable electronics, and embedded systems, where energy conservation is important. By minimizing leakage, the 7T SRAM cell helps extend battery life and enhances the overall efficiency of power-constrained systems.

Table 3. Leakage power of all consider cells

SRAM Cell	Leakage power (nW)
6T	*1.5*
7T	*0.7*
8T	*2.3*

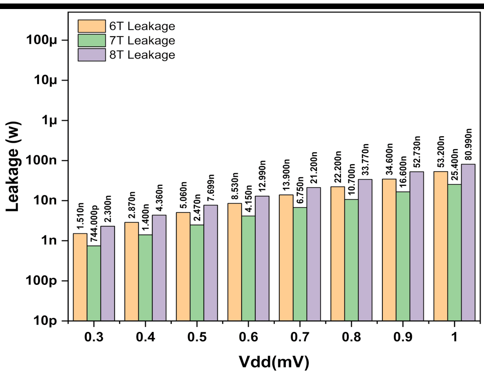


Fig.6. Leakage Power

3.4 Noise Margin

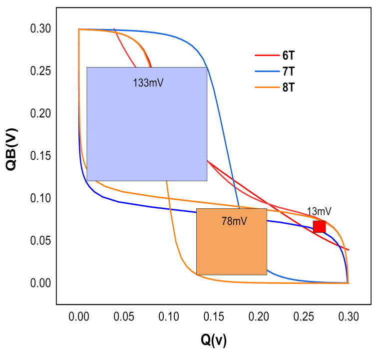
To calculate the noise margin, there are two methods: one is the butterfly method, and the second one is the N-curve method. In this section, we analyze SRAM cell stability with the help of both methods.

Butter-fly method: The noise margin of an SRAM Memory cell is an important parameter that measures the cell's tolerance to noise as well as its ability to retain data under a various operating conditions. It is usually evaluated during read and writes operations and expressed in terms of voltage levels. Static noise margin is measures the maximum noise voltage that can be tolerated by the SRAM memory cell without flipping its stored data. RSNM and WSNM measure the noise tolerance during read and write operations, respectively. In Table 4 summarizes the write and read noise margins.

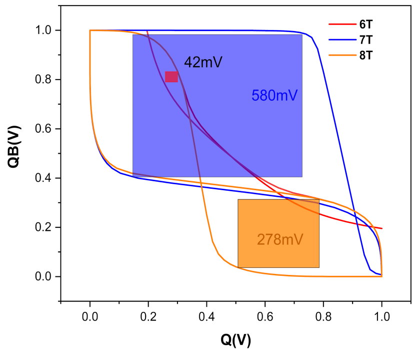
Table 4. Noise Margin.

SRAM Cell	RSNM (mV)		WSNM (mV)	
	1V	300mV	1V	300mV
6T	*42*	13	421	132
7T	*580*	133	270	71
8T	*278*	78	421	132

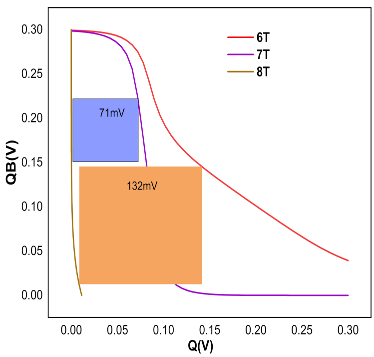
This result shows that the RSNM of 7T cell is much higher than that of the other cells, which shows improved stability during read operations. Leading to a higher RSNM ensures that the cell can better resist disturbances during a read operation. Due to architectural differences, the higher WSNM of the 6T and 8T cells reflects their better performance in write operations.



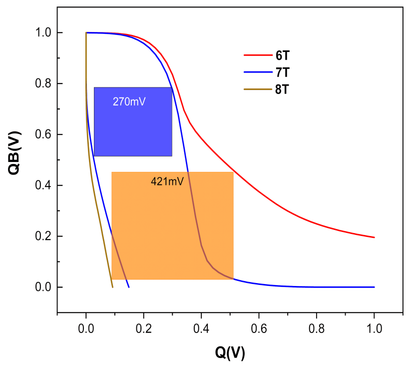
(a) RSNM at 300mV



(b) RSNM at 1V



(c) WSNM at 300mV



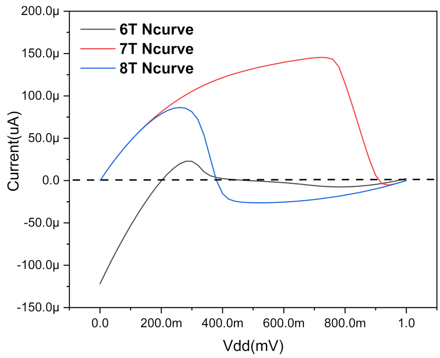
(d) WSNM at 1V

Fig.7 Noise Margin using Butter fly curve

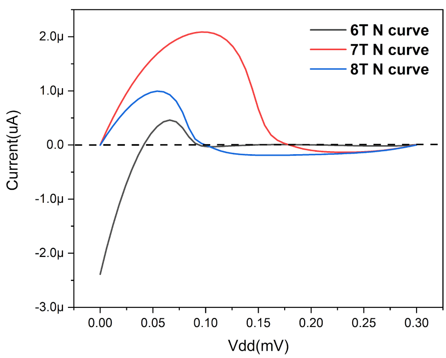
N-Curve method: The stability of the SRAM cell is examined using the noise curve, especially with respect to writing ability and data retention. SNM is unable to provide any data of cell current during the read and write states; overcome this problem using the Noise Curve method. Figure 7 shows the current-voltage characteristics at 1 volt and 300mV, which determine how well the SRAM cell can write to or retain its data.

Table 5. N-Curve for stability.

SRAM Cell	6T		7T		8T	
Parameters	1V	300mV	1V	300mV	1V	300mV
SVNM(mV)	285	71	900	175.75	380	102
SINM (uA)	22.8	0.4	127	1.9	86.45	0.75
WTV(mV)	485	123	102	123.69	618.46	201



(a) N-curve



(b) N-curve

Fig.8.N-Curve at (a) 1Volt and (b) 300mV

The n-curve analysis shows that the 7T SRAM Memory Cell provide the excellent performance in terms of write margin and stability, as reflected by the highest peak current. The 6T cell has minimum Peak current, demonstrating relatively least write margin and stability, which makes it less suitable for low power application. The 8T cell offers moderate improvement.

4 Conclusion:

This study provides a comparative analysis of 6T, 7T, and 8T SRAM cells, evaluating critical performance parameters write and read power dissipation, write and read delays, Static Noise Margin (SNM) during write and read. Simulations performed using the Cadence Virtuoso tool at 90nm GPDK technology, and observed that the 7T SRAM cell better performed in terms of read delay and write power dissipation as compared to 6T SRAM cell, while also demonstrating significantly lower leakage current compared to the 6T and 8T cells. This reduction in leakage current enhances overall power efficiency, making the 7T cell a compelling choice for low-power applications. The 8T SRAM cell, however, exhibits an improved WSNM over the 7T cell, ensuring better write stability, though the 7T cell maintains superior RSNM compared to the 6T cell, indicating enhanced read stability. These results underscore the suitability of 7T SRAM cells for applications that demand efficient write operations, robust read stability, and low power consumption. Moreover, the insights from this work highlight areas for innovation in future memory designs, particularly in optimizing stability and minimizing power dissipation.

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