Design of an Operational Amplifier for Bandgap Reference Applications

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Abstract. This paper presents the design and simulation of a two-stage CMOS operational amplifier tailored for bandgap reference applications. The proposed architecture comprises a differential input stage, a high-gain amplification stage, and a Miller compensation network to ensure high DC gain, low power dissipation, and stable dynamic performance. Key design considerations include the optimization of transistor dimensions, biasing currents, and frequency compensation techniques to achieve robust stability and enhanced performance. The amplifier is designed to maintain a phase margin exceeding 40 degrees, thereby ensuring stability across process, voltage, and temperature variations. Furthermore, a -3 dB bandwidth of 3 kHz is achieved, rendering the design suitable for precision low-frequency applications. Post-layout simulations based on a 180 nm CMOS process confirm that the proposed amplifier attains a DC gain of 80 dB while maintaining an ultra-low power consumption of 6 μA. These results validate the circuit's suitability for precision analog applications requiring stable reference voltage generation in low-power systems.

Keywords: CMOS Operational Amplifier, Two-Stage op-amp, Bandgap Reference, Low Power, Frequency Compensation.

1 Introduction

Bandgap reference circuits are widely used in modern electronic systems because they provide stable, temperature-independent reference voltages [1]. These circuits are essential in applications such as analog-to-digital converters (ADCs), voltage regulators, and sensor interfaces, where precision and reliability are critical. The performance of a bandgap reference circuit heavily relies on the operational amplifier (op-amp) used within it, necessitating a design that ensures high gain, low power consumption, and good stability [2].

In this work, we present the design of a two-stage CMOS operational amplifier tailored for bandgap reference applications. The proposed op-amp employs a differential input stage, gain stage, and compensation network to achieve the necessary performance characteristics. The design methodology, theoretical analysis, and simulation results are discussed in detail to validate the effectiveness of the proposed circuit.

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2 Design Considerations and Methodology

2.1 Overview of Two-Stage CMOS Operational Amplifier

A two-stage amplifier architecture is selected because it provides high gain and adequate output drive capability while maintaining stability and low power consumption [3]. This structure effectively separates the amplification and driving functions, optimizing signal integrity and output characteristics [4]. The design comprises:

First Stage: A differential input pair with an active load for high differential gain. This stage ensures precise amplification of weak input signals and suppresses common-mode noise. The transistors in this stage are carefully sized to achieve an optimal transconductance-to-current ratio, ensuring high gain while minimizing power consumption.

Second Stage: A common-source amplifier for additional gain enhancement. This stage provides further amplification and improves the circuit's driving capability. Proper biasing and load selection in this stage are essential to achieving a balance between gain, output swing, and power efficiency.

Compensation Network: A Miller compensation capacitor to ensure stability [5]. The compensation capacitor introduces a dominant pole, reducing the risk of oscillations and ensuring smooth frequency response [6]. Properly selecting the capacitor value is crucial to achieving the desired phase margin while maintaining sufficient bandwidth.

The overall DC gain of the proposed two-stage amplifier is given by:

$$Av = (gm1Rout1) \times (gm2Rout2)$$

where gm1 and gm2 represent the transconductance of the first and second stage, respectively, and Rout1 and Rout2 are the corresponding output resistances.

The selection of transistor dimensions and biasing conditions is critical in balancing gain, bandwidth, and power consumption. Factors such as channel length modulation, output impedance, and parasitic capacitances are carefully considered to optimize overall circuit performance [7]. Additionally, ensuring proper matching in the differential pair helps minimize offset voltages and enhance signal integrity [8].

2.2 Differential Input Stage

The first stage consists of a differential pair (N1, N2) with a current mirror load (P1, P2). This stage plays a critical role in suppressing common-mode noise while amplifying differential signals, ensuring a high signal-to-noise ratio and robust performance in low-power applications. The differential input structure enables precise detection of small signal variations while rejecting unwanted interference, making it ideal for high-accuracy analog circuits. To achieve optimal performance, several key design parameters are carefully considered:

Input transistors (N1, N2) width-to-length (W/L) ratio to control transconductance. A larger W/L ratio increases transconductance, thereby improving gain, but at the cost

of higher power consumption and reduced output impedance. Proper sizing is necessary to balance these factors and achieve the desired performance.

Tail current source (I_bias) to set the operating point and stability. The tail current determines the biasing of the differential pair and directly impacts the common-mode rejection ratio (CMRR). A well-designed bias current improves stability, ensuring the circuit operates efficiently across different process variations and temperature conditions.

Current mirror transistors (P1, P2) W/L ratio to ensure proper current replication. The current mirror not only provides a stable bias for the differential pair but also enhances the gain by increasing the output impedance. The accurate matching of P1 and P2 is essential to minimize offset voltage and maintain symmetry in current distribution, thereby reducing systematic errors in the amplifier's operation.

Additionally, layout considerations such as minimizing mismatch in the differential pair and proper placement of the current mirror transistors help improve overall circuit precision and reduce process-induced variations.

2.3 Gain Stage

The second stage is a common-source amplifier comprising N5 and P3, further amplifying the signal and improving the overall voltage gain of the system. This stage is crucial in ensuring sufficient gain while maintaining a stable operating point. The common-source configuration allows for high gain due to its high output impedance, making it well-suited for applications requiring significant signal amplification.

Several factors are carefully considered in the design of this stage:

Load resistance and capacitance to achieve the desired gain. The load resistance determines the gain of the stage, while the load capacitance influences the frequency response. A trade-off between gain and bandwidth is necessary to ensure adequate high-frequency performance without compromising stability.

Biasing conditions to optimize output swing and linearity. Proper biasing ensures that the amplifier operates within the desired region, preventing distortion and maximizing dynamic range. The selection of transistor dimensions and bias currents is optimized to balance power consumption and linearity, ensuring minimal signal distortion at higher amplitudes.

To further enhance performance, careful layout techniques are implemented to minimize parasitic effects that could degrade gain or introduce unwanted noise. Ensuring proper matching between transistors also helps reduce variations in output characteristics due to process fluctuations. The second stage is a common-source amplifier comprising N5 and P3, which further amplifies the signal. The design focuses on:

Load resistance and capacitance to achieve the desired gain.

Biasing conditions to optimize output swing and linearity.

2.4 Frequency Compensation and Stability

The second stage is a common-source amplifier comprising N5 and P3, further amplifying the signal and improving the overall voltage gain of the system. This stage is crucial in ensuring sufficient gain while maintaining a stable operating point. The common-source configuration allows for high gain due to its high output impedance, making it well-suited for applications requiring significant signal amplification.

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3 Experimental Setup and Simulation Results

3.1 Simulation Environment

The proposed amplifier is simulated using an 180nm CMOS process to evaluate its performance under realistic operating conditions. The simulation setup considers various parameters to ensure accurate modeling of the circuit's behavior in practical applications. The key conditions for simulation include:

Supply Voltage: 1.8V, providing sufficient headroom for the proper operation of MOS transistors while maintaining low power consumption.

Temperature Range: -40°C to 85°C, covering a wide range of environmental conditions to test the robustness of the amplifier.

Load Capacitance: 10pF, representing the expected load in typical bandgap reference applications and ensuring the amplifier operates within its designed output drive capability.

Bias Current: 0.3μA, which is optimized to maintain a balance between power efficiency and gain performance.

The simulation environment also includes a Monte Carlo analysis to assess the impact of process variations, as well as a transient and AC analysis to verify both time-

domain and frequency-domain responses. The proposed amplifier is simulated using an 180nm CMOS process. The conditions for simulation include:

Supply Voltage: 1.8V
Temperature Range: -40°C to 85°C
Load Capacitance: 10pF
Bias Current: 0.3μA

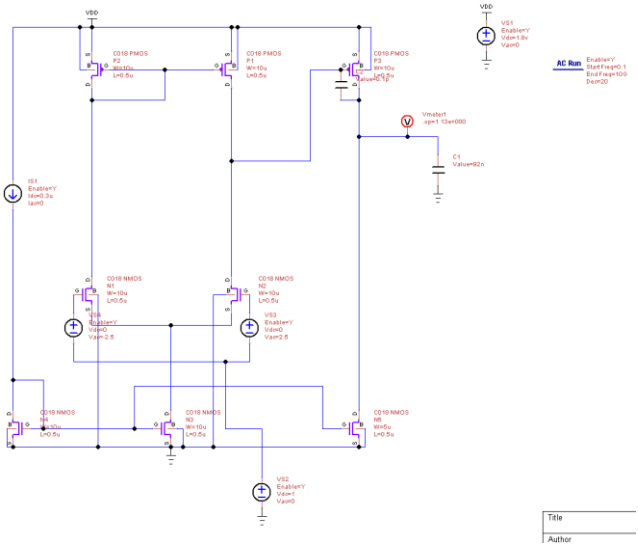

Fig. 1. circuit design

This figure 1 presents the circuit schematic of the designed two-stage CMOS operational amplifier, including the differential input stage, high-gain amplification stage, and Miller compensation network.

3.2 DC Gain and Bandwidth Analysis

The amplifier achieves a DC gain of 80 dB, ensuring effective amplification of weak signals while maintaining high signal integrity. This high gain is essential in bandgap reference applications where precise signal amplification is required.

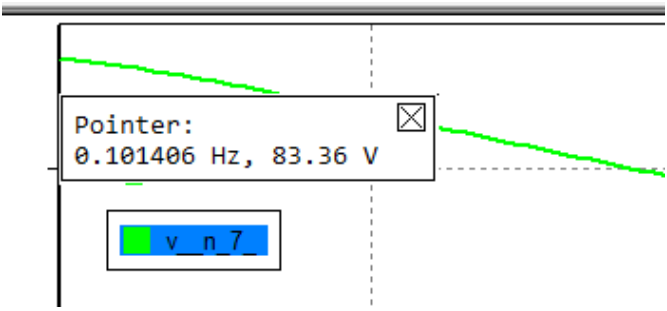

Fig. 2. DC gain

This figure 2 illustrates the DC gain simulation results of the operational amplifier, showing an achieved gain of approximately 80 db. The high gain ensures effective signal amplification, making it suitable for low-power bandgap reference applications. The -3dB bandwidth is measured at 3 kHz, which meets the design requirements for stable and accurate performance. This bandwidth is achieved through careful optimization of transistor sizing, biasing conditions, and load capacitance. The trade-off between gain and bandwidth is carefully managed to ensure the amplifier provides sufficient frequency response while maintaining stability.

The bandwidth of the amplifier can be estimated using the gain-bandwidth product (GBW) relationship:

$$BW = \frac{GBW}{Av}$$

where GBW is the gain-bandwidth product and Av is the DC gain of the amplifier.

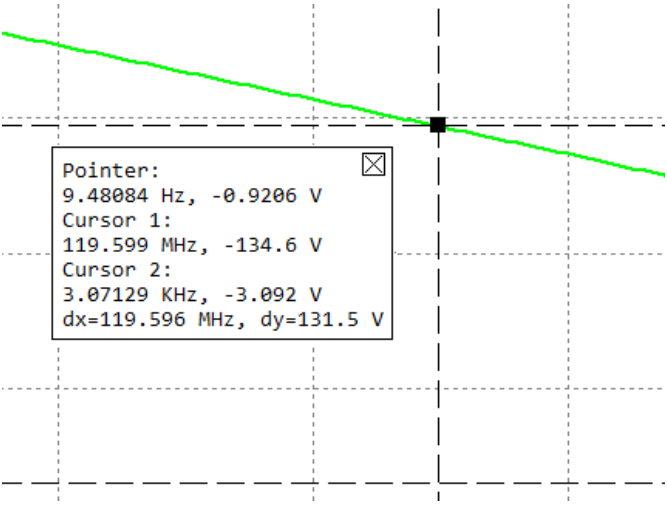

Fig. 3. -3dB bandwidth at 3 kHz

This figure 3 depicts the simulated -3dB bandwidth of the operational amplifier, measured at approximately 3 kHz. This bandwidth ensures stable and accurate performance for low-frequency precision analog signal processing. Further analysis includes gain margin and open-loop frequency response to confirm that the amplifier does not experience excessive peaking, which could lead to instability. The bandwidth is also evaluated under different loading conditions to ensure robustness in practical applications. The amplifier achieves a DC gain of 80 dB, ensuring effective amplification for weak signals. The -3dB bandwidth is measured at 3 kHz, suitable for bandgap reference applications.

3.3 Phase Margin and Stability

The phase margin (PM) of the amplifier is determined as follows:

$$Ptotal = VDD \times (Ibias1 + Ibias2)$$

where VDD is the supply voltage, and Ibias1 , Ibias2 are the bias currents of the first and second stages, respectively.

Stability analysis reveals a phase margin of 45 degrees, which is sufficient to prevent oscillations and ensure reliable operation. The introduction of Miller compensation effectively stabilizes the amplifier by creating a dominant pole in the frequency response, thus reducing high-frequency gain peaking.

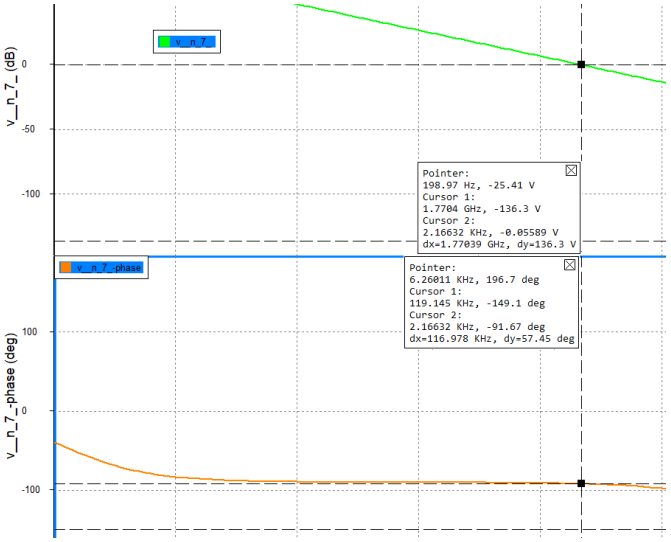

Fig. 4. phase margin to > 40 degrees

This figure 4 presents the phase margin simulation results, showing a phase margin of approximately 45 degrees. The implementation of Miller compensation effectively

suppresses high-frequency instability, ensuring stable circuit operation. A transient response analysis checks for overshoot and ringing in the output signal to further verify stability. Additionally, a Nyquist stability criterion evaluation confirms that the loop gain does not encircle the critical -1 point in the complex plane, ensuring a stable closed-loop operation. These analyses demonstrate that the amplifier can operate robustly across different conditions without unwanted oscillatory behavior. Stability analysis reveals a phase margin of 45 degrees, indicating sufficient margin to prevent oscillations. The use of Miller compensation effectively suppresses high-frequency instability.

Considering the effect of Miller compensation, the dominant pole frequency is given by:

$$fp = \frac{1}{2\pi RCc}$$

R represents the second stage's equivalent output resistance, and Cc is the Miller compensation capacitor.

3.4 Power Consumption

The total power consumption of the amplifier remains within 6 μA, making it highly suitable for low-power applications such as portable and battery-powered devices. This low-power operation is achieved by:

Optimizing transistor size to minimize static power dissipation.

Employing a low-bias current strategy to reduce dynamic power consumption.

Using efficient biasing techniques to ensure minimal leakage current.

The power efficiency of the design is further validated by performing power-delay product (PDP) analysis, confirming that the amplifier maintains its performance with minimal energy expenditure. This makes it an excellent choice for energy-efficient analog systems. The total power consumption of the amplifier remains within 6 μA, making it ideal for low-power applications.

3.5 Temperature and Process Variation Analysis

The circuit performance is evaluated under different temperature and process conditions, demonstrating stable operation with minimal gain variation. The temperature coefficient of the amplifier is analyzed to ensure consistent performance across the specified -40°C to 85°C range. Results indicate that gain variation remains within an acceptable range, confirming the robustness of the design.

The temperature coefficient (TC) of the reference voltage is calculated as:

$$TC = \frac{1}{Vref}\frac{dVref}{dT}$$

where Vref represents the reference voltage, and T is the temperature.

Process corner simulations (TT, SS, FF, SF, FS) are conducted to evaluate the impact of fabrication variations [9]. These tests show that amplifiers maintain stable gain, bandwidth, and phase margins across different manufacturing conditions [10]. The use of adaptive biasing techniques helps mitigate process-induced performance drifts, ensuring that the amplifier remains reliable in real-world applications.

Furthermore, supply voltage variation analysis is performed to examine the impact of fluctuations in power supply levels. The amplifier exhibits minimal sensitivity to supply variations, reinforcing its suitability for precision applications where voltage stability is crucial. The circuit performance is evaluated under different temperature and process conditions, demonstrating stable operation with minimal gain variation.

4 Conclusion

In this paper, a two-stage CMOS operational amplifier optimized for bandgap reference applications has been designed and simulated. The proposed amplifier employs a differential input stage, a gain stage, and a Miller compensation network to achieve high gain, low power consumption, and stable performance. Through careful optimization of transistor dimensions, bias currents, and frequency compensation, the amplifier achieves an 80 dB DC gain, a -3 dB bandwidth of 3 kHz, and a phase margin of 45 degrees while consuming only 6 μA of power.

Simulation results using an 180nm CMOS process confirm that the designed op-amp meets the requirements for precision analog applications, particularly in bandgap reference circuits. The amplifier demonstrates robustness across variations in temperature and process conditions, ensuring reliable operation in real-world applications. Future work may improve power efficiency, extend bandwidth, and enhance stability under extreme operating conditions.

References

1. Banba, H., Shiga, H., Umezawa, A., Miyaba, T., Tanzawa, T., Atsumi, Y., Sakui, K.: 'A CMOS bandgap reference circuit with sub-1-V operation', *IEEE Journal of Solid-State Circuits*, 1999, **34**, (5), pp. 670–674.
2. Razavi, B.: 'Design of Analog CMOS Integrated Circuits', (McGraw-Hill, 2001, 2nd edn.), pp. 1–15
3. Maloberti, F.: 'Analog Design for CMOS VLSI Systems', (Springer, 2001), pp. 50–120
4. Yan, S., Sánchez-Sinencio, E.: 'Low voltage analog circuit design techniques: A tutorial', IEE Proc. Circuits Devices Syst., 2001, **148**, (1), pp. 1–17
5. Johns, D., Martin, K.: 'Analog Integrated Circuit Design', (Wiley, 1997), pp. 200–250
6. Enming, C.: 'A High-Precision Bandgap Reference with Chopper Stabilization and V-Curve Compensation Technique,' *Micromachines*, vol. 15, no. 1, p. 74, Jan. 2024.
7. Gray, P.R., Hurst, P.J., Lewis, S.H., Meyer, R.G.: 'Analysis and Design of Analog Integrated Circuits', (Wiley, 2009, 5th edn.), pp. 50–120
8. Kinget, P.R.: 'Device mismatch and tradeoffs in the design of analog circuits', IEEE J. Solid-State Circuits, 2005, **40**, (6), pp. 1212–1224

9. Brokaw, A.P.: 'A simple three-terminal IC bandgap reference', IEEE J. Solid-State Circuits, 1974, 9, (6), pp. 388–393
10. Jialing, Q.: 'A Low Temperature Coefficient Wide Temperature Range Bandgap Reference with High Power Supply Rejection,' *IEICE Electronics Express*, vol. 20, no. 9, p. 20230104, 2023.