FPGA-Based Hardware Acceleration Technology and Its Application in Image Processing

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Abstract. With the expansion of image processing application scenarios and the diversification of image processing demands across different fields, Field-Programmable Gate Array (FPGA)-based hardware acceleration technology has become an effective solution to overcome the limitations of traditional software implementations. This paper reviews the latest research progress on FPGA applications in image processing, covering multiple application areas such as convolution computing, real-time medical image processing, machine vision inspection, microarray image analysis, and robotic welding. By leveraging parallel computing, pipelining optimization, and hardware acceleration strategies, FPGA-based implementations achieve an optimal balance between processing efficiency, power consumption, and computational performance. This enables FPGA to be widely applied across different domains and makes it the optimal solution for specific application scenarios. Research shows that FPGA architectures can effectively accelerate convolution operations and enable high-speed multi-channel image acquisition and processing, which ultimately enhances medical image quality. Additionally, integrating FPGA into heterogeneous computing environments and System-on-Chip (SoC) designs enhances system scalability and adaptability, meeting diverse application needs. This paper highlights the critical role of FPGA technology in real-time, efficient, and low-power image processing applications and provides in-depth insights into its future applications and challenges.

Keywords: Field Programmable Gate Arrays, Image Processing, Hardware Design Languages.

1 Introduction

Nowadays, image processing technology has been widely applied in various fields and plays a crucial role in areas such as medical diagnosis, autonomous driving, and intelligent security. The core tasks of image processing vary depending on the application field and mainly include image enhancement, object recognition, edge detection, and deep learning inference. Although software algorithms depending on Central Processing Units (CPUs) offer high flexibility, they face significant limits, such as delays in handling large-scale and real-time tasks with high complexity. The lack of

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real-time performance, high consumption of power and high cost of computation all together prevent CPU from being deployed in a lot of application scenarios.

To overcome the limitations of traditional software implementations, Field-Programmable Gate Array **(**FPGA**)**-based hardware acceleration technology has emerged as a widely adopted approach in the field of image processing in recent years. By strategies such as parallel computing, pipeline optimization and computational task decomposition, FPGA-based hardware acceleration significantly improves computational efficiency, enabling low-power and high-performance image processing.

With the diversification of image processing demands, hardware acceleration technologies, especially FPGA, have become the mainstream solution, providing high-efficiency, low-power, and real-time computational capabilities for image processing. The application of FPGA enables image processing to be applied in a wider range of scenarios. Therefore, conducting systematic research on FPGA-based hardware acceleration for image processing is not only of great theoretical value but also has a profound impact on application domains.

The purpose of this review is to provide a comprehensive overview of FPGA-based hardware acceleration technology and its application in image processing. Through summarizing recent research results of this field, this review seeks for future directions, possible challenges and further applications of FPGA-based hardware acceleration technology.

2 FPGA-Based Hardware Acceleration Technology

2.1 Hardware Parallel Structure for Convolution Computing in Image Processing

This paper proposes a hardware architecture for image convolution computing to enhance the speed of convolution computation in hardware acceleration solutions. The design of hardware architecture is primarily based on two parallel computing methods, optimizing image convolution computation by exploring filter parallelism (in the filtering stage) and operation parallelism (in the Multiply-Accumulate (MAC) computation stage), while also adopting structured and defragmented data processing techniques. Furthermore, this design offers flexibility, which makes it adaptable to different types of convolution filters.

Table 1. Processing time and required resources [1]

Method	Conv. Mask time	Resources	Filtering time	Resources	MAC Filter time	Resources
Sequential	47ms	3 Register and 9 Shift memory elements	1.080ms	3 MAC Blocks	1.080ms	18 memory elements

Filter Parallelism	47ms	3 Register memory elements	Shift and 9	0.540ms	6 MAC Blocks	0.540ms	18 memory elements
Operation Parallelism	47ms	3 Register memory elements	Shift and 9	0.360ms	9 MAC Blocks	0.360ms	18 memory elements

According to the performance analysis results in Table 1, FPGA-based hardware acceleration utilizing this architecture significantly reduces computation time in both the filtering and MAC computation stages compared to sequential computing, thereby improving the overall efficiency of image convolution computing.

In addition to reducing computation time, this hardware architecture offers higher hardware efficiency, greater scalability, and more convenient resource optimization. These advantages make FPGA-based hardware acceleration under this architecture applicable for a larger number of scenarios that require image processing compared to traditional software-based implementations [1].

2.2 Hardware Up-gradation Plugin for Accelerating the Image Convolution Processing

This paper proposes an acceleration method by implementing parallel image convolution computing on an FPGA device integrated into the Arty Z7 board. This FPGA device serves as a Hardware Upgradation Plugin (HUP), which is combined with existing CPU- and Graphics Processing Unit (GPU)-based systems to form a heterogeneous computing system. The FPGA device adopts a parallel convolution architecture based on multiple convolution modules.

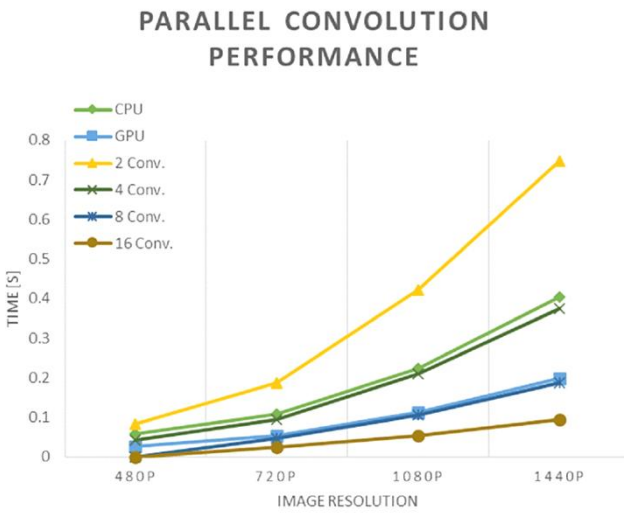

Fig. 1. Performance test results for different hardware solutions [2].

As shown in Fig. 1, the research compares the calculation time of FPGAs with different numbers of convolution modules, CPUs and GPUs. Experimental results show that when the number of convolution modules within HUP reaches a certain threshold, its execution time becomes significantly superior to that of CPUs and GPUs. This indicates that in a heterogeneous computing system, computationally intensive tasks can be allocated to HUP to achieve higher overall efficiency.

The paper also highlights the advantages of this architecture, including hardware efficiency, scalability, and resource optimization. The findings, supported by experimental results, demonstrate that FPGA-based hardware acceleration is an effective solution for optimizing image processing tasks in heterogeneous computing environments. Additionally, the study suggests that there is room for improvement in data read/write performance, recommending further enhancements in the interface between HUP and the original system [2].

2.3 Implementation of Real-Time System for Medical Image Processing using Verilog Hardware Description Language

To meet the high-speed and real-time demands of medical image processing, implementing image processing algorithms in hardware has become essential. In response to this need, this paper proposes an innovative approach by designing a configurable medical image processing system on FPGA using Verilog Hardware Description Language (HDL).

The system adopts a pipelined architecture and utilizes configurable filters to enhance medical images. Users can dynamically adjust the filter sequence and parameters to improve image quality while ensuring real-time performance. When

implemented on Xilinx Virtex-6 FPGA ML605, it achieves a processing frequency of 219.443 MHz with a latency of 18.2280 ns.

Experimental results demonstrate that, compared to implementations based on Digital Signal Processors (DSPs) and software-based approaches, the FPGA-based solution significantly enhance image processing efficiency. The most notable advantage of this system is that it eliminates the need for a dedicated image processing processor. By directly implementing the image acquisition → preprocessing → image use workflow on the FPGA, the system fundamentally avoids data flow bottlenecks. This research proves the efficiency of FPGA-based Digital Image Processing (DIP) systems, paving the way for further research into the hardware implementation of more complex image processing algorithms in the future [3].

2.4 FPGA-Based Multi-Channel Image Acquisition and Processing System

With the integration of information technology and manufacturing, machine vision-based inspection technology has been widely applied in industrial production, especially in large-scale repetitive manufacturing. However, traditional single-camera vision inspection struggles to meet the demands of complex scenarios, such as the precise adhesive detection required in automotive welding. To address the challenges of multi-camera adhesive video inspection, this study proposes a system leveraging the advantages of FPGA to design a multi-channel parallel image acquisition, processing, and transmission solution.

FPGA serves as the core component of the system and acts as the primary control unit. It manages image acquisition, data storage, preprocessing, and transmission functions. It also provides hardware-level parallel computing capabilities, enabling multi-channel data synchronization and significantly enhancing image processing efficiency.

Moreover, the system fully utilizes FPGA's parallel image processing and pipelining capabilities to conduct comprehensive preprocessing of the detected images. It also implements key image processing algorithms such as graIscale conversion, Gaussian filtering, Sobel edge detection, and image stitching. This demonstrates the extensive application potential of FPGA in the field of machine vision inspection [4].

2.5 Design of High-Speed Image Processing System for Weak-Dim Target Based on FPGA

In the field of optoelectronic detection, the detection and tracking of weak targets present a critical technical challenge, especially in long-range detection scenarios. Due to the low signal-to-noise ratio and the small pixel coverage of targets, imaging systems require long exposure times to enhance target signals while maintaining a high frame rate to improve measurement accuracy. However, traditional imaging systems often struggle to balance the requirements of long exposure times and high frame rates.

This paper introduces a high-performance embedded image processing system utilizing FPGA, enabling parallelization of image acquisition and processing. The system adopts a ping-pong storage architecture and leverages FPGA to optimize image

storage and computational processes, successfully addressing the trade-off between long exposure times and high frame rates in detector imaging.

Experimental results demonstrate that the system achieves a frame rate of 50Hz with an exposure time close to 20ms, capable of detecting and tracking targets with a brightness exceeding that of a 3rd magnitude star. Additionally, this design approach is highly versatile and can be applied to other scenarios requiring long-range and weak-target detection [5].

2.6 Design of Sobel Operator Based Image Edge Detection Algorithm on FPGA

The Sobel operator is a technique for edge detection that effectively identifies edge pixels of an image based on the calculation of gradient. However, in real-time image processing scenarios, large amounts of pixel data must be processed within strict time constraints. Therefore, reconfigurable devices that utilize parallel computing technology, such as FPGAs, have become an efficient solution. This paper proposes an FPGA-based Sobel edge detection algorithm, designed using the Xilinx ISE Design Suite-14 and implemented in VHDL, while MATLAB is used for image data conversion and processing.

The detection system was ultimately implemented and tested on Xilinx FPGA series, including Spartan-3, Spartan-6, and Virtex-5, which differ in their processing power and resource efficiency. The results demonstrate that the system can correctly output processed edge detection images while meeting real-time processing requirements and outperforming traditional processors in terms of hardware resource utilization and computational efficiency. Additionally, compared to Spartan-3 and Spartan-6, the Virtex-5 FPGA offers superior performance and resource efficiency due to its DSP48E units, which support efficient multiplication and addition operations [6].

2.7 FPGA technology and parallel computing towards automatic microarray image processing

Microarray technology is an essential tool for gene expression analysis, enabling researchers to understand gene regulatory mechanisms, biochemical pathways, and cellular functions. However, existing software implementations for microarray image processing suffer from long computation times, significant user intervention, and high hardware costs. Therefore, this study proposes an FPGA-based hardware architecture to achieve automated, high-speed processing of microarray images while reducing computational costs.

Microarray image processing typically includes image enhancement, image addressing, and image segmentation steps. In this study, the Xilinx Virtex5 ML505 FPGA board was used to design three core processing units: one for microarray image enhancement, another for computing image projection information for automatic spot position estimation, and the last for image segmentation, including edge detection and background suppression.

Experimental results demonstrate that the FPGA system significantly decreases the processing time for microarray image processing. Although these results of processing time are still longer than those of traditional software platforms, the FPGA-based parallel architecture still has optimization potential. By further increasing the number of processing units to handle multiple microarray spots simultaneously, the overall efficiency can not only be improved but also surpass the performance of traditional software-based implementations [7].

2.8 Efficient Hardware Implementation of 2D Convolution on FPGA for Image Processing Application

Image processing algorithms are naturally localized and operated in a two-dimensional (2D) space, making 2D convolution a fundamental operation in image processing applications. Hence, this paper aims to introduce an efficient FPGA-based hardware architecture for 2D convolution. This architecture reduces the number of different modules, thereby saving hardware resources and minimizing the usage of Lookup Tables (LUTs).

The study employs Verilog for the simulation of 2D convolution and validates the implementation on the Xilinx Spartan 3E FPGA. Compared to existing 2D convolution hardware architectures, the proposed method achieves lower resource utilization and shorter latency in FPGA implementation. For a 16×16 image resolution, the propagation delay is 4.040 ns, and as the image resolution increases, the architecture effectively reduces computational time [8]. The proposed 2D convolution hardware architecture is modular and scalable, making it suitable for high-resolution image processing tasks. Future research can explore FPGA implementations with higher processing capabilities and integrations to meet higher computational demands [8].

2.9 Robotic Welding Path Identification Using FPGA-Based Image Processing

In robotic welding technology, due to the significant variations in weld seam paths and welding gaps, traditional fixed control systems find it challenging to ensure welding quality. To address these issues, the author introduces a weld path detection system on System-on-Chip (SoC) hardware, which extracts the weld path using image processing techniques and provides real-time feedback.

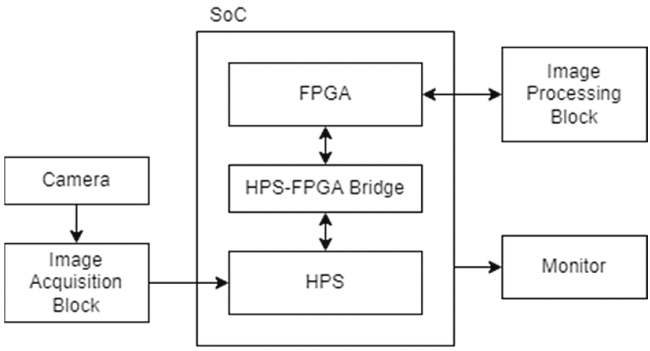

Fig. 2. System block diagram [9].

As shown in Fig. 2, the SoC hardware integrates an Hard Processor System (HPS) and an FPGA. The HPS unit is responsible for image acquisition and preprocessing, whereas the FPGA unit focuses on detailed image processing and outputs weld path data. The image processing includes Median Filter denoising and Canny edge detection, ultimately calculating and outputting the weld gap width. Experimental results show that the weld path data obtained through the camera can be directly used for robotic welding control. The hybrid structure of HPS and FPGA offers modularity, making it adaptable to various hardware conditions, which helps reduce the economic cost of machine vision in welding robots [9].

2.10 FPGA Implementation of SAR Imaging Processing System

Synthetic Aperture Radar (SAR) is a radar technology capable of imaging targets under all weather conditions, often used in military reconnaissance and environmental monitoring. This study proposes a Miniature Synthetic Aperture Radar (MiniSAR) signal processing system on FPGA. To achieve high efficiency of SAR signal processing, the system adopts an FPGA hardware architecture and incorporates the following optimizations: Signal Processing Module: The improved Polar Format Algorithm (PFA) method replaces traditional two-dimensional interpolation with Fast Fourier Transform (FFT) operations, enhancing computational accuracy while reducing computational complexity. Additionally, time-division multiplexing of Intellectual Property (IP) cores is employed to optimize hardware resource utilization.

Time-division multiplexing of Intellectual Property (IP) cores is employed to optimize hardware resource utilization. The FPGA-implemented Phase Gradient Autofocus (PGA) module automatically estimates and compensates for phase errors, improving SAR image focusing quality. The Geometric Correction Module performs image resampling on the FPGA to reduce geometric distortions introduced by PFA. For data transmission, the system utilizes Ethernet IP cores provided by Xilinx and employs the User Datagram Protocol/Internet Protocol (UDP/IP) protocol to achieve high-speed communication between the host computer and the FPGA. To address the extensive row and column operations in SAR data processing, the Matrix Transposition Module utilizes DDR3 for data storage and implements a direct segmentation storage method

to enhance matrix transposition efficiency. Operating at an FPGA frequency of 200 MHz, the system processes a 4K×2K pixel SAR image in just 2.1 seconds, compared to MATLAB's 91 seconds, showcasing the FPGA-based solution's high-speed performance and stability [10].

3 Conclusion

This review provides an in-depth analysis of FPGA applications in image processing. It highlights its advantages in computational efficiency, power consumption, and real-time performance. By leveraging parallel computing, pipeline optimization, and hardware acceleration strategies, FPGA effectively overcomes the limitations of traditional software-based implementations. It has demonstrated remarkable potential across various domains, including convolution computing, medical image processing, machine vision, microarray analysis, robotic welding, and SAR imaging. Furthermore, the integration of FPGA with heterogeneous computing environments and SoC architectures enhances system scalability and interoperability, making FPGA a highly adaptable solution for diverse application needs.

Despite its advantages, FPGA still faces several challenges, including high development complexity, suboptimal hardware resource utilization, and data transmission bottlenecks. Current FPGA development primarily relies on low-level hardware description languages such as Verilog and Very-High-Speed Integrated Circuit Hardware Description Language (VHDL), which require extensive knowledge of circuit design, posing a steep learning curve compared to software-based solutions. Moreover, while FPGA offers efficiency gains in specific image processing tasks, its cost-effectiveness and performance trade-offs compared to GPU acceleration require further investigation, particularly in terms of scalability and economic viability.

Looking ahead, with the continuous advancement of technology, the development of FPGA in image processing is likely to focus on the following key directions. Advancing high-level design tools: Transitioning FPGA programming toward higher abstraction levels by developing more intuitive and user-friendly programming environments. This will lower the barrier to entry and enable broader adoption in image processing applications. Enhancing computational scalability: Leveraging FPGA's multi-core architecture and hardware parallelism to handle increasingly complex image processing tasks with greater efficiency.

Expanding application domains: FPGA holds immense potential in emerging fields such as edge computing, autonomous driving, smart surveillance, and industrial inspection. Exploring tailored FPGA solutions in these areas will allow it to maximize its unique advantages in low-power, high-performance computing. Optimizing synergy with other acceleration technologies: Rather than being viewed as a standalone solution, FPGA should be integrated into hybrid computing architectures, working alongside CPUs, GPUs, and AI accelerators to enhance the overall processing speed of the system.

In summary, while FPGA has already achieved significant breakthroughs in image processing, its future success will depend on overcoming development challenges,

optimizing hardware-software co-design, and exploring novel application scenarios. Instead of focusing solely on hardware acceleration, future research should emphasize a more holistic approach-balancing performance, ease of use, and cost-effectiveness-to fully unleash FPGA's potential in next-generation image processing systems.

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