Research and Design of Low Power Amplifier for Brain Computer Interface

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Abstract. Brain-computer interface (BCI) technology realizes human-computer interaction through direct analysis of neural signals, and has strong application potential in the field of medical rehabilitation and intelligent equipment. However, the high power consumption characteristics of traditional front-end amplifiers limit the stability of BCI systems under long-term implantation. In this paper, two design methods of low power amplifier are proposed: inverter common source common gate transresistance amplifier based on active common leakage feedback mechanism, and current multiplexing chopper amplifier. The former realizes high gain and wide bandwidth under low power consumption through dynamic adjustment of active device bias and topology collaborative optimization. The latter combines dynamic bias optimization and chopper modulation with vertically stacked complementary inverter technology to significantly reduce noise and improve signal integrity. Simulation results show that the proposed design is superior to the traditional architecture in terms of gain, bandwidth and noise performance, while greatly reducing static power consumption. This paper provides an effective solution for the miniaturization and low power consumption of BCI system, verifies the feasibility of multi-objective collaborative optimization technology in bioelectrical signal processing, and lays a technical foundation for the future development of implantable medical devices and high-performance brain-computer interfaces.

Keywords: Low Power Amplifier, Brain-Computer Interface (BCI), Transimpedance Amplifier (TIA), Active Feedback Mechanism, Power Consumption Optimization

1 Introduction

The core of brain-computer interface (BCI) technology is to realize human-computer interaction by receiving and decoding neural electrical signals, which has important value in limb function reconstruction, communication of patients with consciousness disorders and neuroscience research. The long-term implantability of existing BCI systems is faced with a serious challenge that the bioelectrical signal is weak and susceptible to noise interference, and it needs to rely on high-performance front-end amplifiers for signal conditioning, but the high power consumption of traditional amplifiers is easy to cause local tissue thermal damage, and is limited by the limited

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energy supply capacity of implantable devices. In addition, the existing design has a significant bottleneck in the collaborative optimization of low power consumption, high gain, wide bandwidth and other performance indicators, which restricts the practical and miniaturization process of BCI system. How to break through the tradeoff between power consumption and performance has become a key scientific problem to be solved in this field.

In this paper, the low-power design of BCI front-end amplifier is taken as the starting point, and a new circuit architecture and optimization method are explored to achieve multi-objective collaborative optimization of power consumption, gain, noise and other performance parameters. The research focuses on the innovative design of the amplifier core module, improving the energy efficiency ratio through topological reconstruction and dynamic control mechanism, and providing theoretical support and technical solutions for the long-term stable operation of the implantable BCI system.

The thesis is divided into four chapters. The first chapter is the introduction, which describes the application background of BCI technology and the research significance of low power amplifier. The second chapter systematically analyzes the signal characteristics and amplifier design requirements of BCI system, and clarifies the core performance index. In Chapter 3, two low power amplifier architectures are proposed, and the optimization path is discussed from the perspective of dynamic feedback mechanism and current reuse technology, and their performance is verified by simulation. Chapter 4 summarizes the research results, compares the differences of existing technologies, and looks forward to its potential application in the field of neural engineering.

2 Methodology

2.1 Basic overview of BCI

A BCI is a communication system in which messages or commands that an individual sends to the external world do not pass through the brain's normal output pathways of peripheral nerves and muscles [1]. This technique was first developed by Dr Fetz in 1969 by regulating the firing rate of individual neurons in the anterior central cortex of macaques[2]，revealing the possibility of using external forces to control brain activity. In 1973, Vidal explicitly proposed the concept of brain-computer interface for the first time [3].

After years of development, BCI technology has shown broad application prospects.

2.2 Importance of low-power amplifier in brain-computer interface technology

A typical BCI system consists of a closed-loop system consisting of front-end neural signal acquisition, feature extraction algorithm and feedback device, in which the acquisition of bioelectrical signal is the main requirement for the reliable operation of the whole system. LNA is a component of the Analog Front End (AFE). It works by amplifying and refining signals captured by sensors, which are typically responsible for

recording physiological data such as an electrocardiogram (ECG) or electroencephalogram (EEG) [4].

Developing an lna for biomedical use requires consideration of several factors, including low power consumption, significant gain, minimal noise, and optimal linearity [5].

The low power consumption is required because the brain-computer interface needs to implant tissue, and the fragility of the tissue structure makes it possible to damage the heat generated during mechanical work, and because the energy required is provided by wireless or rechargeable batteries, it requires less power consumption to ensure a longer battery life [6].

2.3 Design of core low-power amplifier and methods for reducing power consumption

2.3.1 Inverter common source common gate TIA design based on active common leakage feedback.

The power consumption breakthrough is achieved by dynamic adjustment of active device and collaborative optimization of topology. As shown in Figure 1.

The inverter CCG core consists of complementary transistor pairs to form the inverter amplifier stage, which is cascaded with the CCG pair. The high output impedance of the CCG structure is used to suppress the Miller capacitor and push the main pole to the high frequency. The active common-drain feedback network replaces the traditional transistor pair, and realizes the negative feedback by dynamically adjusting the drain voltage to eliminate the DC bias path, thus reducing the static power consumption [7].

The inverter pair (Mp2&Mn2) is used as the input stage to receive the differential signal directly and realize the initial voltage amplification. The common source common gate pair (Mp & Mn) is used as a constant-on-cascaded transistor to limit the transient current peak of the inverter pair (Mp2&Mn2), reduce the switching noise energy, and improve the circuit stability by dynamically suppressing the switching current fluctuation. In the common drain active feedback network (Mp1&Mn1), Mn1 is the main amplifier tube and its drain outputs the signal. Mp1 is equivalent to a dynamic load resistance and optimizes linearity through a negative feedback mechanism. The constant current source Ib provides static bias current, which can be replaced by a current mirror [8][9][10] structure to eliminate additional bias circuit power consumption and reduce device area.

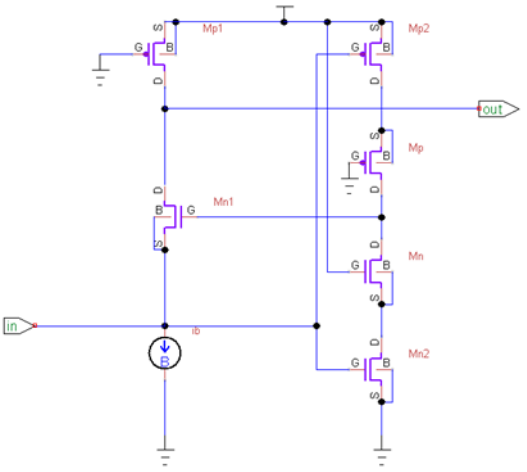

Fig. 1. Inverter cascode with active common-drain feedback mechanism

The proposed TIA enhancement schematic is shown below:
Through simulation (simulation parameters are shown in Table 1), we verified the performance of the amplifier. The frequency response of the amplifier in the -3db bandwidth is 9.2 Ghz, and the transresistance gain is 53.2 dB ohms. The power consumption of the circuit is 3.2 mW. This design reduces power while ensuring good gain and bandwidth.

Table 1. Simulation parameter table

VLSI Technology (Channel Length)	180 nm
Channel length to width ratio	Mp1 = 18 Mn1 = 6 Mp2 = Mn2 = 2.25
Capacitance	450 pF
Supply voltage	1.8 V

Table 2 summarizes the performance of the proposed TIA enhanced circuit compared to previous similar circuits.

Table 2. Comparison of the performance of the proposed TIA-enhanced circuit with previous similar circuits

Topology /technique	**Technology (nm)**	**Supply voltage (V)**	**Gain (dB-ohm)**	**Bandwidth (Ghz)**	**Power (micro Watts)**	**Figure of Merit (FoM)**
Regulated Gate Cascode [11]	180	1.8	56	8.27	35	13.23
Inverter Cascode [12]	40	1.2	69.2	7	19.25	25.16

Inverter with Active Feedback [13]	40	1.1	47	8	2.03	185.22
Inverter Cascode with Active Feedback (this work)	180	1.8	53.2	9.2	3.2	152.95

To evaluate performance, a normalized performance optimum value is defined here for quantifying circuit energy efficiency, expressed as:

$$FOM = \frac{\text{Gain(dB)}\times\text{Bandwidth（GHz）}}{Power\ dissipation\ （mW）} \quad （1）$$

This formula shows that the reduction of power consumption will directly increase the FOM value while maintaining the gain and bandwidth performance. Simulation data show that the improved circuit based on the 180 nm CMOS process has a significantly better FOM than the traditional architecture (see Table 2). This result verifies the effectiveness of the proposed structure in multi-objective collaborative optimization such as gain, bandwidth and power consumption, especially through the technology to achieve a breakthrough reduction in power consumption.

2.3.2 Chopper amplifier with cascade amplifier.

Aiming at the amplitude characteristics of electroencephalogram (EEG) microvolt level, this design achieves a breakthrough in transconductance efficiency through vertically stacked complementary inverter, The overall structure consists of three choppers, a cascade amplifier, a negative feedback loop, and a DC servo loop, and two pseudo-resistance stabilized input common mode levels are connected at the input end of the amplifier [14].

Its low power consumption mechanism is as follows:

Current multiplexing structure technology (its structure is shown in Figure 2)

By vertically stacking the NMOS and PMOS input pairs, a single bias current flows through four complementary inverters, enabling quadruple current multiplexing. As shown in Figure 2, the input pair M1a-M4a shares the tail current source Iss with M1b-M4b, ensuring that each transistor operates in the saturation region by optimizing the bias voltage (Vb1-Vb7) distribution. The design makes the total transconductance Gm meet:

$Gm \approx 4gm$

This current multiplexing structure can significantly reduce static power consumption and improve the gain of the circuit without adding additional current. At the same time, due to the reduction of current and power consumption, there can be more margin in the first stage of tube core selection, so as to further optimize the noise performance of the chip.

Dynamic bias optimization

The inverter cascade structure faces several technical problems in practical application. First, the architecture results in a significant increase in the system supply

voltage, increasing the circuit power consumption. Secondly, due to the existence of multiple independent input ports, how to establish an efficient low-noise input coupling mechanism has become a key problem, which needs to ensure the integrity of the signal and realize the economy of the cost. Third, the multi-output structure requires the development of low-loss small-signal current integration technology, which poses a dual challenge to system energy efficiency and manufacturing costs. It is worth noting that the optimization process of the above technical solution must strictly ensure the core performance indicators of the circuit, including the common mode rejection ratio (CMRR), power supply rejection ratio (PSRR) and the working stability under environmental factors such as process deviation, power supply voltage fluctuation, temperature change (PVT), and avoid the deterioration of key parameters caused by the improvement of the architecture. In order to minimize the voltage margin consumed by the cascade amplifier, a bias circuit is used to bias each of the four stacked input pairs of the cascade amplifier. The current is copied using a current mirror to generate a voltage through a gate-drain short-circuited MOS tube, which is then connected to their gate-ends by a pseudo-resistor.

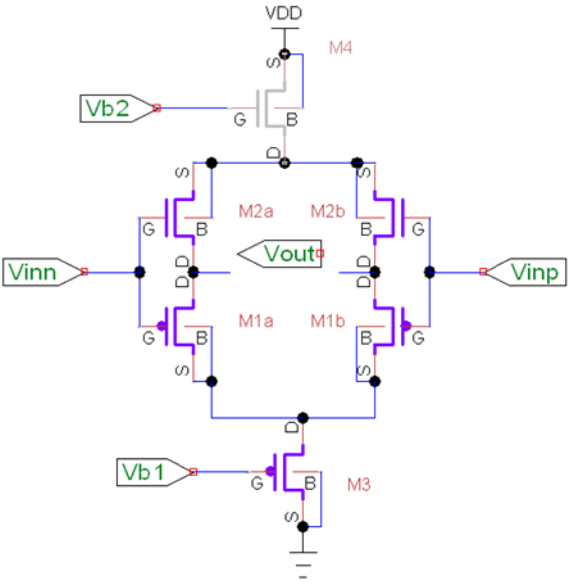

Fig. 2. Inverter current multiplexing structure

In order to minimize the voltage margin consumed by the cascade amplifier, a bias circuit is used here to bias each of the four stacked input pairs of the cascade amplifier. The pseudo-resistance is used to construct feedback, which increases the circuit stability.

Chopper modulation

In order to prevent the clock feed-through effect and offset the partial channel charge injection more effectively, a chopper is used instead of a single tube ground switch. The chopper uses complementary CMOS switches, four of which are designed to effectively prevent clock feed-through effects and offset partial channel charge injection. In order to avoid the production of large switching parasitic capacitance, MOS tubes with smaller switching sizes are usually used.

The performance of the amplifier is verified by simulation. When the frequency is in the range of 2.08kHz to 875.07kHz, the gain of the amplifier is greater than 70dB. When the whole PAC simulation is carried out, the closed-loop gain of the amplifier is 39.98dB and the 3dB bandwidth is 1.5kHz, which can meet the needs of low frequency bioelectrical signal processing. Dc servo circuit (DSL) effectively inhibits electrode misadjustment. 5mV input misadjustment attenuates to 2.1mV after 4 seconds, and the suppression ratio is 252.4 times. The common mode rejection ratio (CMRR) exceeds 104dB in the low frequency band, showing excellent anti-interference ability. In addition, after the cascade of rotating filters, the equivalent input noise in the 0.5-100Hz band is reduced to 0.9μVrms, with a noise efficiency factor (NEF) of 4.24. As a result, the cascade amplifier consumes a maximum current of 3.6μA in the temperature range of approximately -40° to 120°, achieving low power consumption.

3 Conclusion

The practical application of brain-computer interface (BCI) technology depends on the high efficiency and reliability of the front-end signal acquisition system, and the low-power amplifier as its core module directly affects the long-term implantability and stability of the system. Aiming at the trade-off between power consumption, gain and noise performance of traditional amplifiers, this paper proposes two innovative low power amplifier design schemes, which provide theoretical basis and technical path for performance optimization of BCI system.

Firstly, the active common-leakage feedback based inverter common source common gate transresistance amplifier (TIA) can effectively suppress the redundancy loss of static power by dynamically adjusting the active device bias and cooperating with topology optimization. The design uses the cooperative work of complementary transistor pairs and dynamic feedback network, which can significantly reduce the power density of the circuit while ensuring wide bandwidth and high gain. The simulation results show that the optimal value of performance (FoM) is significantly improved compared with the traditional scheme, which verifies the effectiveness of dynamic feedback mechanism in power optimization. Secondly, the chopper amplifier with vertically stacked complementary inverters and current multiplexing structure realizes the cooperative goal of low noise and high energy efficiency through quadruple current multiplexing technology and dynamic bias optimization. The introduction of chopper modulation technology further inhibits the clock feed-through effect and offset voltage, improves the signal integrity, and the integration of pseudo-resistance feedback network enhances the environmental anti-jamming ability of the circuit.

Compared with traditional architectures, the two schemes proposed in this paper show significant advantages in power consumption, noise and gain. Its core innovation

is to break through the limitation of single performance optimization in traditional design, and balance the contradictory needs of low power consumption and high precision through multi-objective collaborative design method. In addition, the dynamic control mechanism and topology reconstruction strategy adopted provide a scalable technical framework for the miniaturization and low power consumption of implantable medical electronic devices in the future.

Future studies can further explore the effect of process size reduction on circuit performance, optimize the real-time control algorithm for dynamic bias, and verify its robustness in complex biological environments through live experiments. The research results of this paper not only provide a new design idea for the development of BCI technology, but also lay an important foundation for the low power consumption and integration of bioelectrical signal processing chips, and have broad clinical application and industrialization prospects.

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