Research on High-Gain Operational Amplifier Architecyures: A Comparative Study of Cascode, Two-Stage, and Three-Stage Designs

Zijun Ni

Cangzhou Jiaotong College, Rail and Transit college, Tianjin, China
NIZIJUN040407@outlook.com

Abstract. This study investigates advanced operational amplifier (op-amp) architectures for gain enhancement, focusing on cascode, two-stage, and three-stage configurations in high-performance circuits. The cascode op-amp combines the high gain of common-source amplifiers with the wide bandwidth and low output impedance of common-gate amplifiers, making it particularly suitable for high-frequency applications. Two-stage op-amps employ folded-cascode structures to achieve an optimal trade-off between gain and output swing, meeting the requirements for higher amplification. Three-stage op-amps further improve signal amplification by enhancing gain, stability, and output drive capability, enabling adaptation to diverse load conditions. Through a comprehensive analysis of each architecture's advantages and limitations, this research provides valuable theoretical insights and practical optimization strategies for designing high-gain op-amps. The findings contribute to the development of more efficient, stable, and versatile electronic systems, offering guidance for engineers in selecting and refining op-amp designs for specific applications. This work underscores the importance of architectural innovation in advancing analog circuit performance.

Keywords: High-Gain op-amp, Cascode Structure, Gain-Boosting Techniques, Signal Amplification

1 Introduction

Operational amplifiers (op-amps) are one of the most critical components in analog real-time signal processing systems[1]. As integrated circuit technology continues to advance, high-performance op-amps are increasingly used in analog signal processing, sensor interfaces, data conversion, and other fields. Many configurations of current mirror are discussed and used for many applications. Especially cascode current mirror which is one of the main building blocks of analog and mixed-signal integrated circuits[2]. The cascode structure, two-stage, and three-stage op-amp architectures have become focal points of recent research, aiming to achieve higher gain, better common-mode rejection ratio (CMRR), and improved output drive capability.

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Invented in 1979 and subsequently refined in 1990, the CMOS active-cascode gain-enhancement technique finds wide applications in analog integrated circuits[3], play a significant role in the study of high-gain op-amps.because of the increasing demand to the low power systems ,designing of the low power circuits is taken great consideration[4], For example, the folded-cascode structure effectively reduces power consumption while increasing gain and bandwidth, making it widely applicable in low-voltage, low-power applications. Additionally, optimization techniques such as current mirror loads, source followers, and gain-boosting stages can further enhance the op-amp's gain and linearity. Therefore, selecting the appropriate op-amp architecture and optimizing design parameters using gain-boosting techniques are crucial for achieving high-performance analog circuits.

This paper is divided into five chapters. Chapter 1 introduces the research background, significance, and the importance of high-gain op-amps in analog signal processing, along with current research trends. Chapter 2 analyzes the basic principles and circuit characteristics of cascode op-amps, focusing on their high-gain properties and advantages in high-frequency applications. Chapter 3 discusses the architecture and optimization of two-stage op-amps, examining the impact of folded-cascode structures and gain-boosting techniques on performance. Chapter 4 explores the working principles of three-stage op-amps and their optimization strategies for drive capability, stability, and frequency response. Finally, Chapter 5 concludes the paper by summarizing the research and outlining future directions for high-gain op-amps in analog integrated circuits.

2 Gain-Boosting Circuits

2.1 Cascode Operational Amplifier Circuit

2.1.1 Basic Structure.

The common source and common gate amplifier is a high-performance single-stage amplifier structure that significantly improves gain, output impedance and frequency characteristics by stacking transistors, and is widely used in analogue IC design. common-source level (chemistry) ， The input transistor (M1 or Q1) operates in a common-source (common-emitter) configuration and is responsible for transconductance amplification ， Signal input from gate (base), output from drain (collector) ， common gate level (electronics) ， Stacked transistors (M2 or Q2) operating in common gate (common base) configuration as current buffers ， The gate (base) is connected to the fixed bias voltage and the source (emitter) is connected to the output of the CS stage. NMOS Common Source + NMOS Common Gate ， Shielding effect of the common gate stage (shielding the CS stage drain from early effects), resulting in a significant increase in output impedance ， The common gate stage reduces the Miller effect of the CS stage and extends the bandwidth. The cascode current mirror and the regulated cascode current mirror are used to increase output impedance and improved active feedback current mirror and a three stage feedback current mirror are proposed to improve the accuracy[5]. The cascode op-amp combines the common-source and common-gate amplifier structures, leveraging the advantages of both. The common-source amplifier provides high gain, while the common-gate structure offers wide bandwidth and low output impedance, ensuring excellent performance in high-frequency applications.As shown in Figure 1,Folded Cascode Operational Amplifier.

The telescopic cascode structure is a common high-gain amplifier circuit that increases the input signal through the common-source stage but limits the output voltage swing. In contrast, the folded-cascode structure improves the output swing but may not meet the power consumption and gain requirements of high-performance circuits[6].

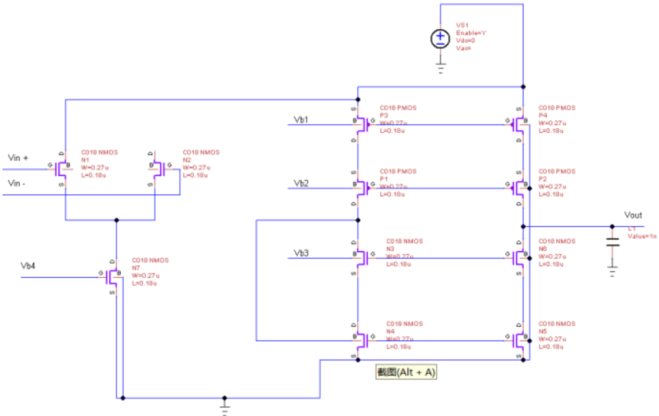

Fig. 1. Folded Cascode Operational Amplifier

2.1.2 Differential Amplifier.

In the differential amplifier architecture, a cascode operational amplifier can suppress common-mode noise, and the common-gate section is insensitive to common-mode noise because the input impedance of the common-gate is extremely low, and the gain of the noise signal is also relatively low, thereby enhancing the ability to suppress common-mode noise.The differential amplifier consists of a subtractive attenuator followed by an output gain stage, with the operational amplifier section employing an identical structure[7].As shown in Figure 2,Two-Stage Operational Amplifier。Common source and common gate amplifiers are one of the core modules of high-performance analogue circuits through clever transistor stacking that achieves a quantum leap in gain, impedance and frequency characteristics from a single-stage amplifier.

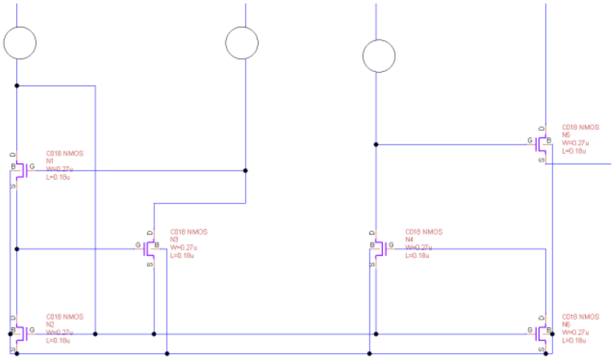

Fig. 2. Two-Stage Operational Amplifier

In a cascode operational amplifier, the common-source amplifier section is primarily responsible for providing high gain, while the common-gate section serves to suppress noise and stabilize the gain. Through this distribution of gain, the entire system is capable of delivering high gain without excessively amplifying noise signals. The gain of the common-source section increases with the input signal, but the common-gate section aids in maintaining the stability of the system's gain and the suppression of noise throughout this process.Fully differential folded-cascode (FC) amplifier is being used in many low-voltage and high bandwidth applications and does not suffer from “mirror pole” limitations. This structure is utilized in many cases[8].

2.2 Two-Stage Operational Amplifier

2.2.1 Basic Principles.

Two-stage operational amplifiers are core modules for analogue integrated circuit design, offering high gain, good stability and wide applicability. ， First stage (differential input stage) 。Provides high differential gain, high input impedance and common mode rejection ratio ， differential pairing tube ， Active loads (e.g. current mirrors) to maximise gain. Outputs: single-ended or differential (converted to single-ended output by current mirror). Level 2 (gain level) ， Function: Provides additional voltage gain and drives the output. Common source (CS) or common emitter (CE) amplifiers (for high gain) ， Active loads (e.g. current sources or resistors) ， Achieved by two-stage high-gain cascade ， Current mirrors convert differential currents to single-ended outputs Two-stage op amps are the cornerstone of analogue design, balancing gain, stability and versatility. Its performance depends on optimisation of bias design, compensation capacitance and transistor size. Modern improved architectures (e.g. folded common-source, common-gate, sleeved op-amps) are based on this foundation. The two-stage amplifier using the cascode structure employs a low-voltage current mirror to achieve high gain. The first stage uses a PMOS input folded-cascode structure with gain-boosting techniques to increase output impedance and gain.

The second stage adopts a simple common-source structure to provide maximum output swing[9].

The design of a two-stage op-amp requires two stages to serve different purposes. The first stage provides high gain, while the second stage ensures output swing and stability. Compared to the telescopic cascode structure, the folded-cascode structure offers a larger output swing and can be used as a unity-gain buffer[10].

2.3 Three-Stage Operational Amplifier

2.3.1 Basic Principles.

Three-stage operational amplifiers add an additional gain stage to the traditional two-stage structure (differential input stage + gain stage) to address design challenges under the demands of high gain, high bandwidth, and high driving capability, Differential input stage (first stage): provides high common mode rejection ratio (CMRR) and low noise, Intermediate gain stage (second stage): provides the main voltage gain, Output buffer stage (third stage): provides low output impedance for enhanced drive capability, Differential input stage (first stage), Structure: PMOS/NMOS differential pair + active load (current mirror), Converts differential input signals to single-ended signals, Provides high common mode rejection ratio, Determines input noise and distortion voltage, Intermediate gain stage (second stage): Architecture: Common Source Amplifier (NMOS/PMOS) + Current Source Load, Provides mains voltage gain, level shift, Determines the gain bandwidth product of the op amp, Improved output impedance with Cascode structure, Miller Compensation for stability, Output buffer stage (third stage), Structure: Class-AB push-pull output stage, Provides low output impedance, Enhancement of driving capabilities, Increase in swing rate, Reduced crossover distortion with Floating Bias, Feedforward compensation for improved stability.The input stage features a rail-to-rail differential pair with active load current mirrors, providing high common-mode rejection ratio (CMRR) and low input-referred noise characteristics，The differential amplification stage employs a folded cascode topology with gain boosting techniques to enhance the overall open-loop gain while maintaining adequate phase margin,The output stage utilizes a class-AB push-pull configuration with adaptive biasing, delivering robust output current drive capability up to ±50mA with minimal crossover distortion,The bias generation circuit incorporates a bandgap reference and start-up circuitry to establish stable operating points for all amplifier stages. Advantages of three-stage op-amp: ultra-high gain (>100dB), strong driving ability, low distortion, Three-stage op-amps offer irreplaceable advantages in scenarios requiring ultra-high precision and strong drive through reasonable gain allocation and compensation strategies.

2.3.2 First-Stage Amplification.

The first stage of high-gain CMOS operational amplifier circuits typically consists of differential pair transistors (NMOS or PMOS), active loads, biasing circuitry, and current mirrors where applicable. As shown in Figure 3,This CMOS-based op-amp architecture typically consists of four key functional modules: The input stage employs a differential pair configuration for high-precision signal reception and initial processing. The intermediate stage serves as the differential amplification stage, utilizing cascode or current mirror load circuits to provide the primary gain amplification. The output stage adopts a push-pull or class-AB amplifier structure to ensure sufficient output drive capability and voltage swing. The bias circuit delivers precise and stable operating points to each stage while incorporating self-biasing or bandgap reference techniques to enhance power supply rejection ratio (PSRR) and temperature stability.,

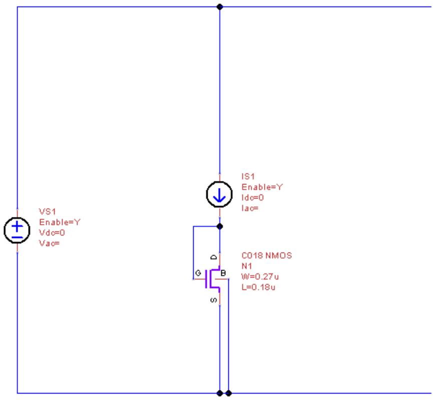

Fig. 3. First Stage

2.3.3 Second-Stage Amplification.

In a three-stage operational amplifier architecture, the second stage (intermediate gain stage) is the central hub connecting the input stage to the output stage. Main gain contributor stage: Provides more than 60% of the voltage gain of the full amplifier (40-60dB typical), converting the first stage differential output to a large amplitude single-ended signal. High-impedance node design: using a common-source amplifier structure (e.g. NMOS driver + PMOS current-mirror load) to take advantage of its high output impedance (Ro>100k Ω) to achieve gain enhancement Converts high impedance differential signals at the input stage to low impedance single-ended signals. Transconductance-enhanced design: gm>8mS by aspect ratio optimisation (e.g. NMOS W/L=200 μ m/0.18 μ m) PSRR boost: >60dB power supply noise rejection through symmetrical design of current mirror loads, Linearised design: common source and common gate (Cascode) structure or gain bootstrap technology to reduce THD to less than -70dB,Contributes 60%-70% of full circuit voltage gain， The second stage is used to further amplify the signal. In this stage, multiple transistors are employed to increase the amplification factor.As shown in Figure 4 The second-stage differential amplifier helps improve the frequency response and stability of the op-amp. In high-frequency applications, the second-stage design controls the gain-bandwidth product, avoiding bandwidth limitations and instability.

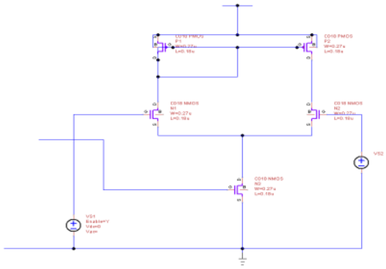

Fig. 4. Second stage

2.3.4 Third-Stage Amplification.

The third stage (output stage) of a high-gain operational amplifier serves as a critical functional module whose design directly determines the overall performance of the amplifier. Typically employing Class AB or push-pull output configurations, this stage fulfills three core functions:5.First, it delivers robust output drive capability through carefully designed current buffer structures capable of outputting drive currents up to several tens of milliamperes. Second, it optimizes output signal quality by utilizing advanced distortion cancellation techniques to maintain total harmonic distortion below 0.01%. Third, it ensures system stability under various load conditions through built-in compensation networks.The output circuit as shown in Fig 5.

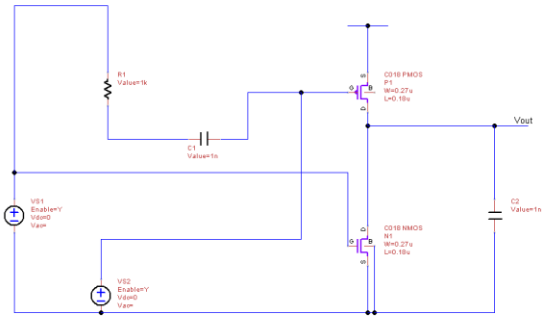

Fig. 5. Output

3 Conclusion

This paper has explored the application and optimization of cascode, two-stage, and three-stage operational amplifiers in high-gain circuits. The cascode structure combines the high gain of the common-source amplifier with the wide bandwidth of the common-gate amplifier, demonstrating excellent performance in high-frequency signal processing. The two-stage op-amp, using the folded-cascode structure and gain-boosting techniques, achieves large output swing and optimized gain, making it suitable for low-power, high-gain applications. The three-stage op-amp, through more complex cascaded amplification, improves system stability, output drive capability, and frequency response, enabling it to adapt to various load conditions.

By comparing and analyzing different architectures, it is evident that selecting the appropriate circuit architecture and incorporating gain-boosting techniques are essential for achieving high-performance analog signal processing in high-gain op-amp design. These technological innovations have significantly enhanced the signal processing performance.

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