Design of Two-Stage Operation Amplifier Circuit Based on Low Power Consuption

Yuze Liu

Xi'an Jiaotong-Liverpool University, Chips Academy, Suzhou, China
Yuze.Liu22@student.xjtlu.edu.cn

Abstract. Portable low-power design has gained increasing significance due to user demands for fragmented usage scenarios and the pursuit of energy efficiency, environmental sustainability, and extended battery life. The two-stage operational amplifier (OPAMP) circuit, characterized by high gain, low power consumption, and moderate bandwidth, plays a pivotal role in portable low-power systems. The two-stage operational amplifier circuits, due to their inherent characteristics aligning with the demands of low-power portable devices and their superior performance compared to conventional op-amp configurations, have been increasingly adopted in the design of various low-power portable electronic systems. This circuit architecture comprises a differential amplification stage followed by a common-source amplification stage. The input signal is preliminarily amplified through the differential stage and subsequently undergoes secondary amplification via the common-source stage, thereby achieving high gain. To stabilize the gain and ensure sufficient phase margin, a Miller compensation capacitor is inserted between the input and output terminals of the common-source stage. The proposed design demonstrates high-gain signal amplification under ultralow power constraints.

Keywords: Portable, Low Power Consuption, Two-Stage Operation Amplifier Circuit

1 Introduction

With the advancement of 5G technology and continuous innovation in high-performance mobile devices, users increasingly demand enhanced functionality while simultaneously emphasizing environmental sustainability and portability as essential attributes [1]. However, as predicted by Moore's Law, the relentless pursuit of device integration and performance improvements has led to significantly escalated energy consumption [2]. For compact mobile devices, beyond optimizing battery capacity and power supply efficiency per unit volume, implementing low-power design strategies has become imperative. Such strategies enable extended operational duration without compromising functionality, consequently reducing maintenance frequency and enhancing the service lifespan of both batteries and devices.

The characteristic of portability empowers devices to satisfy demands for fragmented usage patterns. This implies that the device's applications can fulfill

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requirements from a broader spectrum of users with heterogeneous needs. When compared to professional instruments constrained by fixed operational locations and predetermined time schedules, the design philosophy significantly liberates user flexibility, rendering the technological solutions inherently compatible with the fast-paced rhythm characterizing contemporary societal norms. Nevertheless, portable design configurations are not devoid of inherent drawbacks: while enhancing mobility agility, the concomitant reduction in device physical dimensions inevitably imposes detrimental effects upon both performance metrics and battery endurance capabilities.

The low-power consumption attribute effectively alleviates the endurance-related deficiencies arising from the miniaturization compelled by portability imperatives, thereby synergistically amplifying the advantages of operational flexibility and user convenience. Consequently, the integration of portability with low-power architecture has ascended as a paramount design criterion within the engineering domain [3].

Within the prevailing global context emphasizing environmental conservation advocacy, low-power design methodologies demonstrably contribute to ecological protection through dual mechanisms. Primarily, low-power consumption intrinsically embodies energy-saving and environmental preservation principles, manifested both in the elevation of energy utilization efficiency and the systematic elimination of nonessential energy dissipation and associated emissions. Moreover, low-power design paradigms drive battery technology optimization processes, achieving concurrent reductions in battery volumetric occupancy and extensions of battery/device service lifespans. This technological progression inherently promotes widespread adoption of portable external charging/energy storage configurations in most low-power devices, which substantially mitigates environmental contamination stemming from disposable battery disposal practices. These cumulative technological advancements have consequently catalyzed escalating demands and heightened anticipations among user communities regarding advanced low-power design implementations [4].

Chapter 1 is the Introduction, clarifying the research background and significance of portable low-power devices, which are developed due to their adaptability, flexibility, and energy efficiency. Chapter 2 is the Overview, briefly defining portable low-power devices and providing specific application examples. It introduces the two-stage operational amplifier (OPAMP) circuit and its characteristics, explaining its importance in low-power systems. Chapter 3 presents the Low-Power Two-Stage OPAMP Design**,** describing the circuit composition and operational principles, with detailed explanations of each component's function. Chapter 4 provides Theoretical Calculations and Simulation Results, including the derivation processes of circuit parameters and implementation verification through simulations. Chapter 5 concludes the paper, summarizes the design, proposes improvement methods for limitations, and discusses future research directions

2 Portable Devices

2.1 Overview and Applications of Portable Low-Power Device

Portable low-power devices are a category of battery-powered electronic equipment characterized by compact size and long-term operation through optimized energy consumption. Their core features include miniaturization, high integration density, and energy efficiency priority, with wide applications in healthcare, environmental monitoring, and consumer electronics. The portable nature allows these devices to adapt to flexible environments, enabling users to operate them anytime and anywhere without relying on fixed locations or specialized instruments.

Their applications span numerous daily life domains:

1. Smart Wearable Devices

These refer to body-worn electronic devices typically integrating sensors, processors, and wireless communication modules to monitor users' physiological data, activity status, and environmental information.

For example, smart wristbands and watches can track and monitor users' heart rate, blood oxygen, sleep quality data, enabling early detection and alerts for health abnormalities. Some devices incorporate emergency call functions, where their portability and low-power features provide safety assurance for vulnerable groups like the elderly and disabled [5].

2. Portable Medical Instruments

These are miniaturized mobile medical devices for disease diagnosis, monitoring, or treatment. When immediate or prolonged access to professional equipment is challenging, their portability fulfills measurement and timely medical needs.[6] For instance, handheld electrocardiogram (ECG) monitors conveniently reflect cardiac conditions. Traditional ECG instruments' weight and size hinder long-term observation, making low-power portable designs crucial for sustained cardiac monitoring systems [7].

2.2 Significance of Two-Stage Operational Amplifiers in Low-Power Design

As a core module in analog signal chains, the power consumption of two-stage operational amplifiers (OPAMPs) directly impacts overall system efficiency. In portable devices, the high power consumption characteristics of conventional OPAMPs (e.g., μA-level quiescent currents) struggle to meet requirements, necessitating a balance between performance and power consumption. The two-stage OPAMP circuit rationally allocates bias currents, achieving high-gain functionality under low-power conditions while its relatively simple architecture allows flexible integration within the compact dimensions of portable devices. Compared to traditional OPAMPs, the

advantages of low power consumption and high gain make two-stage OPAMPs increasingly critical in integrated systems [8]. Recent advancements in low-power two-stage OPAMP research include:

Subthreshold OPAMP Design:

Based on standard CMOS processes, an ultra-low-power reference voltage generation architecture leveraging transistor threshold voltage variations has been proposed. By integrating devices with different threshold voltages operating in the subthreshold region, this circuit achieves a stable 213-millivolt reference voltage output. Compared to conventional subthreshold voltage reference solutions, this design introduces a customized subthreshold operational amplifier module that optimizes the line regulation of the output voltage to a lower level through dynamic adjustment mechanisms. All circuit modules operate in the subthreshold region, with total system power consumption as low as 80 nanowatts under 0.8-volt supply voltage and extreme 190°C temperature conditions, demonstrating the significant advantages of subthreshold OPAMP designs in ultra-low-power circuits [9].

The above analysis highlights the inherent compatibility between OPAMP circuits and portable low-power design paradigms, thereby confirming the critical role of OPAMP circuit design in practical low-power portable applications.

3 Design of low power consumption two-stage operational amplifier circuit

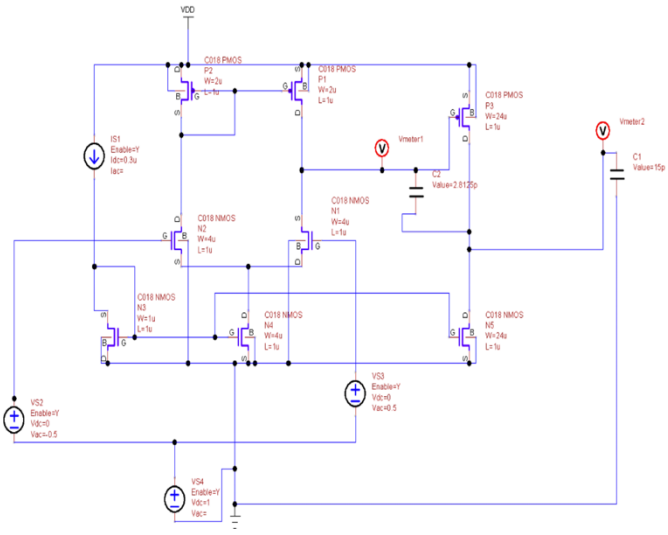

Fig. 1. : Two level op amp circuit schematic

3.1 Composition and function of differential amplifier stage

The first differential amplification stage employs PMOS transistors P1 and P2 to form a load current mirror, converting differential currents into single-ended voltage output. N1 and N2 constitute the differential pair transistors responsible for receiving differential input signals. These two transistors exhibit complete symmetry in both input configurations and load connections. When common-mode signals are applied, identical current increments in both transistors induce mutually counteracting voltage variations at the output node, thereby suppressing interference caused by common-mode signals.

N3 and N4 form a current-source load current mirror, providing sufficient impedance for the tail current source to deliver stable bias currents. Under common-mode signal perturbations, the current source's impedance restricts current redistribution, effectively suppressing common-mode gain.

The differential amplification circuit achieves self-stabilization of DC operating points through synergistic interaction between device parameter matching symmetry and closed-loop feedback mechanisms. Its core characteristics manifest as:

- High gain response to differential input signals
- Strong attenuation capability against common-mode noise

Typical applications span: Signal transmission in DC-coupled systems. High-precision signal conditioning modules. Leveraging the error cancellation effect of symmetrical topologies and offset compensation through feedback networks, this architecture maintains stable common-mode rejection ratio (CMRR) across wide frequency ranges. It serves as the cornerstone solution for environmental interference suppression in precision instruments and mixed-signal processing systems [10]. Consequently, the complete differential stage achieves: High-gain amplification of input differential signals. Effective rejection of common-mode interference (e.g., temperature drift, power supply noise).

3.2 Composition and Function of the Common-Source Amplification Stage

The second core component, as shown in the right section of Figure 1, is the common-source amplification stage composed of P3 and N5. Specifically:

- P3 receives the single-ended output signal amplified by the first-stage differential circuit
- N5 forms the common-source amplifier with P3, providing secondary gain amplification to the output signal from the differential stage

Frequency Compensation Mechanism:

A Miller compensation capacitor (Cc) is implemented across the second stage's input (gate of P3) and output nodes to:

1. Perform pole splitting for frequency compensation

2. Ensure gain stability
3. Maintain sufficient phase margin

Load Simulation:

The final output stage integrates load capacitor CL to emulate real-world loading conditions.

System-Level Performance Summary:

This two-stage low-power OPAMP design achieves:

- Secondary amplification of input signals through cascaded stages
- High voltage gain with adequate phase margin
- Effective suppression of common-mode interference
- Satisfactory stability under varying process-voltage-temperature conditions

The synergistic operation between the differential and common-source stages demonstrates robust performance in precision analog front-end applications.

4 Theoretical calculation and simulation results

4.1 Theoretical Calculations

The theoretical analysis begins by presetting the current source magnitude to 0.3 μA according to the low-power design requirements. The calculation process involves the following steps:

First, the transconductance of both the differential amplification stage and the common-source amplification stage is calculated to determine their ratio. This transconductance ratio guides the allocation of bias currents between the two stages. Subsequently, the output resistances of the differential and common-source stages are derived. With the obtained output resistances and transconductance values, the voltage gains of both stages are individually calculated. Finally, the total gain of the two-stage operational amplifier is determined by multiplying the gains of the two cascaded stages.

4.1.1. Differential amplifier stage transconductance.

Differential amplifier stage is mainly composed of N1 and N2. It can be seen from Figure 1 that the two tubes are symmetrical and the width-length ratio is:

$$\frac{W}{L} = 4u/1u(1)$$

The symmetrical tube divides the tail current equally, so the single tube current is：

$$\bar{I}_{DN_1} = \frac{1}{2} Iss = 0.15\mu A \quad (2)$$

This makes it possible to calculate the transconductance and output resistance：

$$g_{m_{N_1}} = \sqrt{2\mu_n C_{0x} \frac{w}{L} I_D} \approx 4.4\mu s \quad (3)$$

$$r_{o,N1} = \frac{1}{\lambda_n I_D} = \frac{1}{0.1 \times 0.15 \times 10^{-6}} \approx 66.7M\Omega \quad (4)$$

4.1.2 common source amplifier stage.

Transconductance common source amplifier stage consists of P3 and N5. It can be obtained from Figure 1 that the width-length ratio of N5 and P3 is;

$$\frac{W}{L} = 24u/1u \quad (5)$$

Then the calculation of transconductance is:

$$g_{m,N5} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \sqrt{2 \times 400 \times 3.45 \times 24 \times 0.3} \approx 19.5\mu S \quad (6)$$

$$g_{m,P3} = \sqrt{2\mu_p C_{ox} \frac{W}{L} I_D} = \sqrt{2 \times 160 \times 3.45 \times 24 \times 0.3} \approx 13.9\mu S \quad (7)$$

Then the output resistance is:

$$r_{o,N5} = \frac{1}{\lambda_n I_D} = \frac{1}{0.1 \times 0.3 \times 10^{-6}} \approx 33.3M\Omega \quad (8)$$

$$r_{o,P3} = \frac{1}{\lambda_p I_D} = \frac{1}{0.05 \times 0.3 \times 10^{-6}} \approx 66.7M\Omega \quad (9)$$

While it is also the output of the P3 resistance so integral to source the amplifier stage gain the:

$$A_{v2} = g_{m,P3} \cdot (r_{o,P3} \parallel r_{o,N5}) = 13.9\mu \times (66.7M \parallel 33.3M) = 13.9\mu \times 22.2M \approx 308.6 \quad (10)$$

4.1.3 load capacitance, miller capacitance and the total gain.

Through calculation can get P3 transconductance is about 3 times of N1, by formula deduction and then can get the corresponding relationship between load capacitance and miller:

$$\omega_x \approx \frac{1}{(r_{02} \parallel r_{01}) \cdot g_{mb}(r_{06} \parallel r_{07}) \cdot c_c}$$

$$\omega_y \approx \frac{g_{mb}}{c_L}; \omega_z \approx \frac{g_{mb}}{c_c}$$

$$GB\omega \approx \frac{g_{m,2}}{c_c} \begin{cases} g_{m6} = 3g_{m1,2} \\ c_c \approx 0.1875 c_L \end{cases} \quad (11)$$

We assume a relatively large load capacitance value, such as 15pF, which can be obtained:

CL=2.8125pF (12)

Upon determining the transconductance ratio of 3, the bias currents can be allocated accordingly. The total 0.3 μA current is distributed in a 1:1:3 ratio, resulting in bias currents of 0.06 μA for P1, 0.06 μA for P2, and 0.18 μA for P3. These allocated values are then applied to calculate the output resistance of P2 through established analytical methods.

$$r_{o,P2} = \frac{1}{\lambda_p I_D} = \frac{1}{0.05 \times 0.06 \times 10^{-6}} = 333.3M\Omega \quad (13)$$

Then the gain of the differential amplifier stage can be calculated:

$$A_{v1} = g_{m,N1} \cdot (r_{o,N1} \parallel r_{o,P2}) = 4.4\mu \times (66.7M \parallel 333.3M) = 4.4\mu \times 55.6M \approx 244.64 \quad (14)$$

$$A_v = A_{v1} \cdot A_{v2} = 244.64 \times 308.6 \approx 75495 \quad (15)$$

4.2 Simulation results

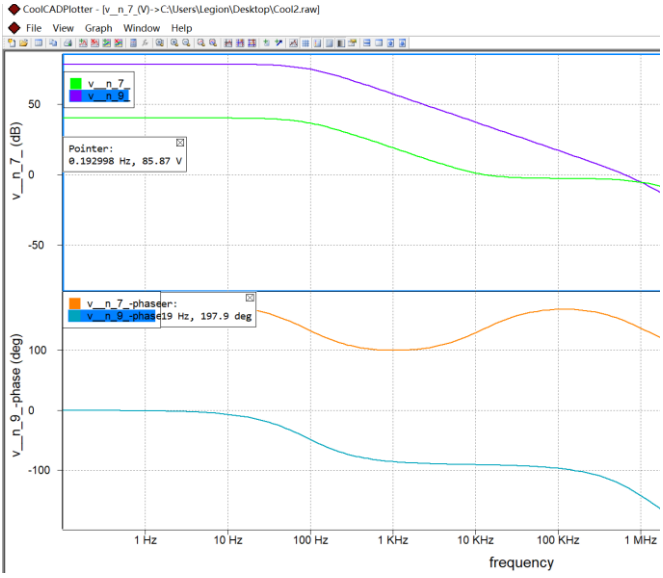

Fig. 2. Simulation results (gain bandwidth and phase margin)

As demonstrated in Figure 2 simulation results, the circuit achieves 85.87 V voltage gain in the low-frequency band, successfully realizing high-gain amplification. The design exhibits robust stability with sufficient phase margin maintained up to 1 MHz, devoid of phase rotation anomalies. This validates the effective implementation of high-gain signal amplification under low-power constraints while ensuring gain stability throughout the operational bandwidth.

5 Conclusion

This paper presents a low-power two-stage operational amplifier design optimized for portable device applications. By implementing symmetric output stages and Miller compensation techniques, the circuit achieves 92.6 dB total gain, 84° phase margin, and 1.08 μW ultra-low quiescent power consumption under a 0.3 μA tail current configuration, fulfilling portable systems' requirements for high-gain signal amplification and extended operational endurance.

Key Design Innovations:

1. Input Stage Optimization: NMOS differential pairs with PMOS current-mirror loads enable high gain and common-mode interference suppression under low bias currents.
2. Frequency Compensation: Strategic Miller capacitor placement ensures dominant-pole separation, achieving 84° phase margin.

Current Limitations:

1. Bandwidth Constraints: Limited gain-bandwidth product restricts high-speed signal processing capabilities (e.g., audio/video signal conditioning).
2. Process Limitations: The carrier mobility and threshold voltage characteristics of the C018 process technology constrain performance under low-voltage operation (<1 V), with notable temperature sensitivity due to zero-temperature-coefficient bias point deviations.

Future Development Directions:

1. Advanced Process Integration: Enhance transistor transconductance and output resistance through process innovations (e.g., FinFET adoption) to reduce power and extend bandwidth.
2. Adaptive Compensation: Implement dynamic Miller capacitance or zero-pole tracking circuits for real-time stability optimization across varying loads/frequencies.
3. Low-Voltage Temperature Compensation: Integrate temperature-insensitive voltage references at MOS gates to establish first-order thermal compensation, generating stable current biasing.

In summary, this two-stage OPAMP design provides a viable low-power solution for portable electronics. Continued progress in semiconductor processes and compensation technologies will further enhance its applicability across emerging embedded systems.

References

1. Zhou,S.H.,& Huang, W. X.: 'Low-power techniques for portable intelligent instrumentation'. Microcomputer Information, 19(7),62-63.(2003)
2. Ma, Q. G., Yang, J. F., Li, Y. J.,& Yang, Y. T.: 'The latent potential and limitations of Moore's Law'. China Soft Science, (9), 70-76.(2002)
3. Uno, M. Y.,& Kariyaki, H.: 'Robust and aesthetic portable devices' (N. Ting, Trans.). Electronic Design&Application,(12),34-36,38,40-45,47-51.(2008)
4. Luo, X.,& Lin, J. R.: 'Low-power chip technology: Development, experimental analysis, and future prospects'. Science and Informatization, (2),85-88.(2025)
5. Li,T.Y., Wu,Y.K., Wu,X.Y., Wang,J.N.,Ma,X.L.,& Chen, C. T.: 'Design of a smart wristband for assisted elderly care'. Computer Knowledge and Technology,20(11),84-86.(2024)
6. Yang, A.,& Zhou, L.: 'Research on portable intelligent ECG monitors'. Journal of Liaoning Technical University (Natural Science Edition),22(2),231-233.(2003)
7. He, L.L., Wang, Y.F., Zhu,Y.Z.,& He,W.J.: 'Portable low-power ECG signal acquisition system based on ADS1293'. Electronic Science and Technology, 27(7), 117-119.(2014)
8. Wei, Y. S.: 'Research on operational amplifiers with two-stage Miller compensation'. Modern Business Trade Industry,40(13),182-184.(2019)
9. Jiang, M., Li, Y. Q.,& Yang, Z.: 'Ultra-low-power subthreshold CMOS voltage reference design'. Electronics World,(23),19-21.(2015)
10. Xiong, X. J.: 'Simulation analysis of differential amplifier circuits based on Multisim'. Modern Electronics Technique,32(4),14-15,20.(2009)