# Design and Optimization of Two-Stage CMOS Amplifier

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**Abstract.** The two-stage Complementary Metal Oxide Semiconductor（CMOS) amplifier features high gain, low power consumption and excellent stability, playing an irreplaceable role in modern communication, audio processing and other fields. This paper designs and analyses a CMOS two-stage amplifier that meets specific performance indicators, including a direct current (DC) gain greater than 80 dB, a -3 dB bandwidth of 3 kHz, and a total current consumption not exceeding 6μA. By adopting a cascade of common-source amplifiers, current-mirror biasing, and a differential input topology, the gain and linearity of the amplifier have been enhanced. Capacitance compensation technology has also been employed to optimize the phase margin to 83.03°, far exceeding the stability requirement of 40°. According to the simulation results, this amplifier effectively resolves the issues of gain and power consumption limitations, while achieving a strong phase margin and bandwidth control, making it a feasible option for low-power and high-gain applications. The theoretical values are compared with actual data. Finally, the paper points out the improvement of the two-stage CMOS amplifier, and the prospect of future development is presented.

**Keywords:** Two-Stage CMOS Amplifier, High Gain, Low Power Consumption, Phase Margin, Capacitance Compensation

## 1 Introduction

As integrated circuits have advanced, CMOS amplifiers have become increasingly significant in the domains of data conversion, biological signal detection, and audio signal processing. According to Thulasi et al. operational amplifiers are essential in miniaturized integrated circuits for various applications [1]. In order to minimize power consumption while maintaining high gain, a CMOS two-stage amplifier is constructed and improved in this study.

The purpose of this study is to design and optimize two-stage CMOS amplifier. The report is structured as follows: First, the background is included in the introduction. After the introduction, this paper is divided into four parts, the first of which will cover the capabilities and weaknesses of the basic components. Next, the paper will introduce the circuit designed on the basis of the basic components. Then, the theoretical value


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and the actual situation of the analog circuit will be given. Finally, the results and conclusions will be presented.

## 2 Basic Component

Common single-stage amplifiers are common-gate amplifiers, common-source amplifiers and common-drain amplifiers. In Luzhaitsev 's study, it was found that devices that include a power limiter in an integrated circuit reduce the amplitude of the input signal [2]. Figures 1 and 2 show data related to common source amplifiers. Although single-stage amplifiers have low power consumption and low noise, their gain is limited, and it is difficult to meet both high input impedance and low input impedance.

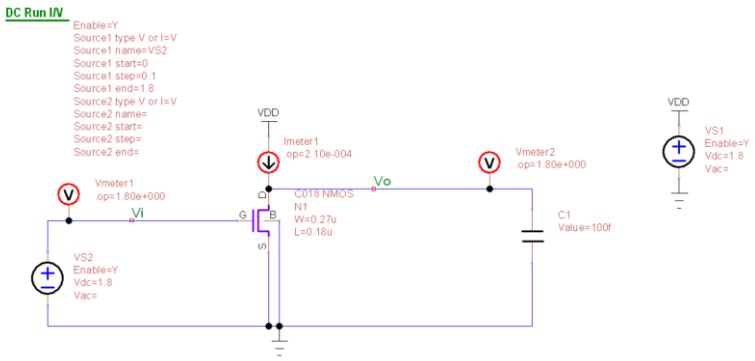


**Fig. 1.** Common-source amplifiers

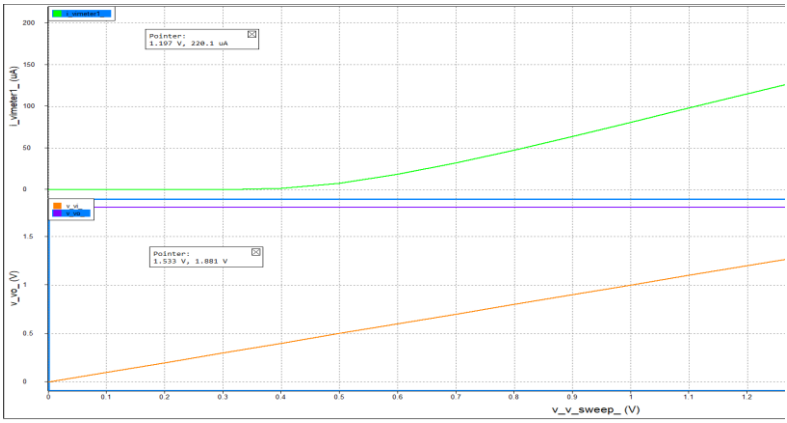


**Fig. 2.** Data from common-source amplifier

It is known that pre-charging the gate of the current mirror can significantly reduce the on-time of a single transistor, resulting in a significant reduction in the delay from off to on-time [3]. The current mirror mainly provides a constant current source to ensure the paranoid stability of the circuit, and accurately replicates the current between different circuit components, thereby improving the stability of the circuit and reducing power consumption. However, it is necessary to constantly adjust the corresponding output impedance to make the circuit more perfect and reduce unnecessary errors. The circuit is shown in Figure 3.

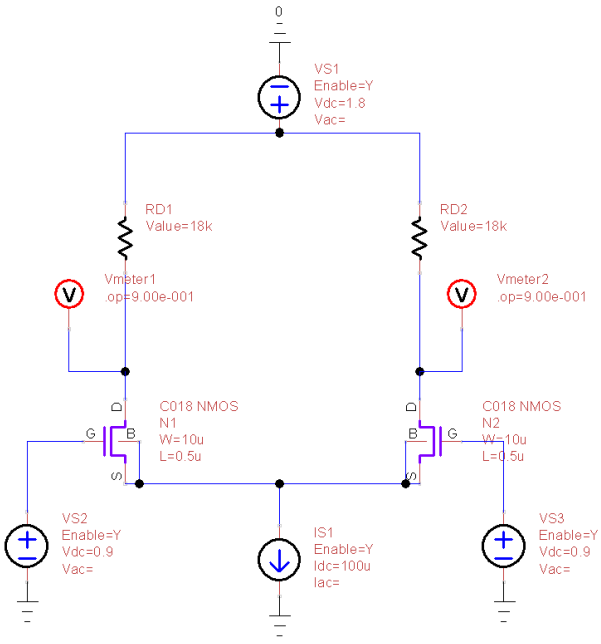


**Fig. 3.** Current mirror

## 3 Circuit Design

It is mainly use $C018\,NMOS - TSMC$ 0.18μ$m$ and $C018\,PMOS - TSMC$ 0.18μ$m$ transistors from the N-Metal-Oxide-Semiconductor (NMOS) and Positive channel Metal Oxide Semiconductor (PMOS) symbols in $CoolSpice$.

According to the demand, the DC gain needs to exceed 80dB, that is, the voltage gain $A_v > 10^4$. Because it is a two-stage amplifier, the gain of each stage is multiplied. Assume that the first stage gain is $A_{v1}$, the second stage $A_{v2}$, and the total gain $A_v = A_{v1} \times A_{v2}$. So, it may be necessary to gain at least 100 or so per stage, so that the two stages can reach 10000 (80dB). In terms of bandwidth, the bandwidth of -3dB is 3kHz. However, the bandwidth of the amplifier is mainly determined by the main pole, which may need to be analyzed by Miller compensation. In an empirical investigation, Thulasi et al. pointed out that it was important to include a frequency compensation circuit in

the operational amplifier (op amp) [1]. Finally, the total current consumption is less than 6μA, so it is necessary to rationally distribute the current bias at all levels.

According to the requirements, the analog circuit in Figure 4 is designed. $P_1$ and $P_2$ constitute an active load just like a switch, provide power. Then, $N_1$ and $N_2$ constitute differential pairs, which are differential mode signals and play a stabilizing role in the operation of the amplifier. They are mainly used for accurate current replication, ensuring that the input current is consistent with the output current. $N_3$ and $N_4$ used as part of a multistage current mirror in circuits that require higher stability and common-mode rejection ratio. Width and length should correspond to each other in order to ensure the exact relationship between the input current and the output current. $P_3$ and $N_5$ are common source amplifiers, the whole amplifier can be controlled by adjusting the size of width and length. What's more, the main purpose of capacitance compensation is to ensure the stability of the circuit during operation, prevent oscillations caused by capacitance effects in the circuit and reduce noise.

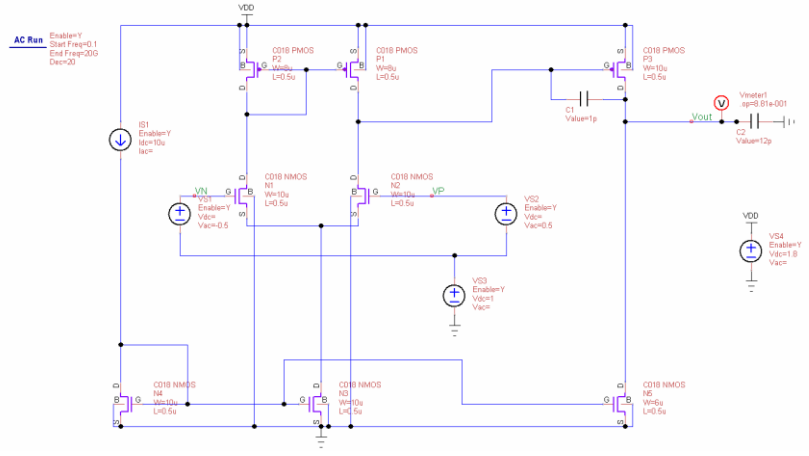


**Fig. 4.** Designed circuit

## 4 Theoretical Data and Practical

There are some formulas: $GBW = \frac{g_{m1}}{2\pi C_L} \geq 3kHz$ and $A_v = g_m R_{out}$.It is known that $g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D} = \frac{2I_D}{V_{OV}}$. And then, $arctan\left(\frac{GWB}{W_{sp}}\right) + arctan\left(\frac{GWB}{W_{sp}}\right) < 50°$. In addition, $r_0 = \frac{I}{\lambda I_D}$ and $f_{-3dB} = \frac{1}{2\pi R_{out} C}$. So, it can get a theoretical number, $C = 5pF$,$W_z = 4MHz$ and $W_{sp} = 100Hz$. However, in the actual situation, due to various reasons, the theoretical data cannot be well adapted to the required situation. The actual circuit diagram is shown in Figure 4 above. According to the analog circuit, it can solve the two projects.

The two projects contain five small questions. Figure 5 shows the answer to the first project. For DC gain >80dB， In the green curve, the smooth position at the beginning

can directly read 80.51dB, satisfying the problem. And for -3dB bandwidth at 3 kHz, it needs to be found that DC gain cannot be less than 77 at 3kHZ. The value is 78.48 so it satisfies the question. What's more, the tail current of $N_5$ is 2μA, and for the static current of $N_3$ plus $P_3$ is 4μA. So, total current consumption < 6μA. The circuit designed thus completes the first three tasks well.

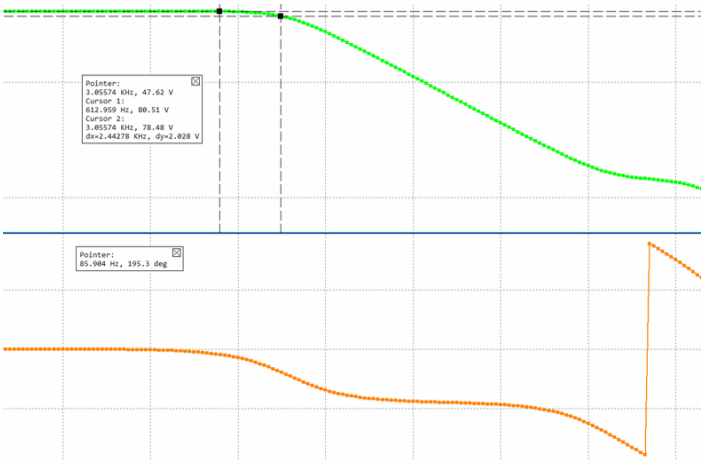


**Fig. 5.** The first part of the answer

Figure 6 shows the answer to the second part. It needs to use capacitor compensation to improve the phase margin to > 40 degrees. When the phase at 0dB, the orange curve corresponds to 83.03. Therefore, the phase margin is $83.03 + 170 = 263.03 > 40$, satisfying the problem. The phase margin is an important index to measure the stability of the feedback control system. It reflects the difference between the phase Angle and -180° when the open-loop gain reaches 1. A higher phase margin means that the system has better stability and can effectively resist external disturbances and parameter changes to avoid oscillations or instability.

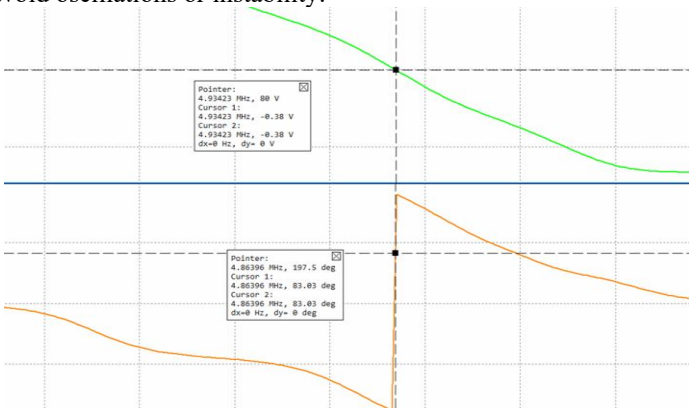


**Fig. 6.** The second part of the answer

In Mathew's study, it used a frequency compensation technique with nested Miller capacitors and zero-point resistors between the two stages [4]. Figure 7 shows an optimized circuit using a reverse-nested Miller compensation network to reduce power consumption. The increased size of the PMOS is to compensate for its mobility disadvantage ( $\mu_p \approx 0.3\mu_n$ ), while maintaining high gain, broadband width and stability. Miller capacitors have significant advantages in the design of two-stage operational amplifiers, especially in terms of frequency compensation and stability optimization. The risk of oscillation is suppressed by introducing a Miller capacitor between the first stage output and the second stage input of the amplifier. This compensation technology not only simplifies the circuit design but also reduces the chip area and cost. In addition, Miller capacitors maintain circuit stability and reliability while achieving high gain and wide bandwidth. In addition to this, the power can be reduced by reducing the size of the transistor [5]. This can be done by reducing the transistor size, such as reducing the channel width or adjusting the aspect ratio. This is mainly due to the reduction of parasitic capacitance, which reduces the charge and discharge energy during the switching process.

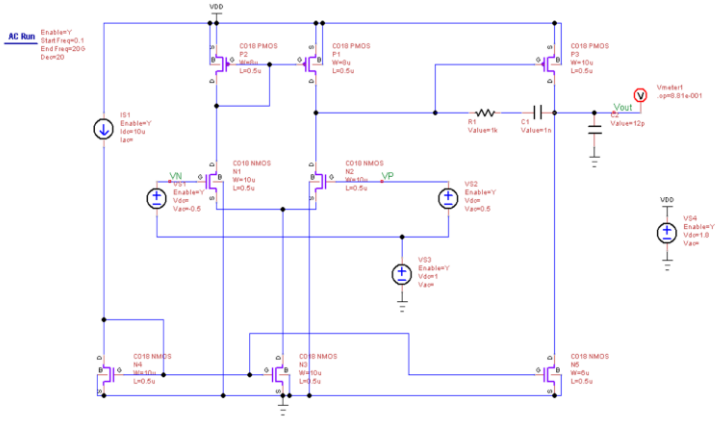


**Fig. 7.** The optimized circuit

As CMOS devices continue to scale, enabling the integration of more transistors on a single IC chip, the complexity of circuit design in advanced CMOS technology nodes is also growing significantly [6]. Because as the device size shrinks, the leakage current increases and the threshold voltage drift becomes more significant, resulting in a significant increase in design complexity and uncertainty. Second, parasitic effects on circuit performance are increasingly prominent, especially in high frequency and high-density layouts, where the management of signal integrity and power consumption becomes critical. In an empirical investigation, Farag et al. [7] pointed that Computer aided design (CAD) and Matrix Laboratory (MATLAB) can be used to reduce the difficulty of calculation and design. By introducing new transistor structures and advanced materials, the short-channel effect can be better controlled, thereby reducing leakage current and improving transconductance, achieving higher gain and bandwidth at the same power consumption. Rational use of CAD and MATLAB, to achieve

intelligent design. Through this highly automated and precise design process, designers are able to achieve high-performance, highly reliable CMOS two-stage amplifiers in less time.

In high-density layouts and high-frequency operations, noise can lead to an increase in the bit error rate, resulting in circuit performance. According to Chang et al. noise and input impedance matching networks are very important for optimizing circuit performance [5]. For most two-stage op-amps, ensuring that the signal between the two stages is fast and stable with minimal overshoot is key to the design, as this directly affects the dynamic response and stability of the circuit. The distribution of poles and zeros can be optimized to suppress high-frequency oscillations and reduce noise. At the same time, Qi [8] showed that thermal and flicker noise can be reduced by optimizing transistor size and bias conditions. And the differential signal processing is used to suppress noise interference. The stability and response speed of the circuit can be improved by selecting a reasonable transistor size and bias condition and optimizing the load capacitance and compensation capacitance. Thus, the efficient and stable operation of the two-stage operational amplifier is realized.

With the continuous progress of science and technology, both materials and circuits are constantly developing. In Das's study, analog and mixed-signal circuits have a long design process and are somewhat challenging [9]. What's more, Jin [10] pointed out that the two-stage operational amplifier system consists of five modules, namely differential input, high gain stage, output buffer stage, bias circuit and compensation circuit. In practical applications, most of the performance indexes of operational amplifiers will restrict each other, resulting in the design becoming a multidimensional optimization problem. As the core module of analog integrated circuit, two-stage CMOS amplifier has a broad development prospect in the future performance optimization and application expansion. Low power and high energy efficiency will be the focus of the design, which can improve transconductance and noise performance through subthreshold operation and dynamic power management. At the same time, the device size and bias conditions are optimized, so that the device can meet the needs of high-precision signal processing. In addition, the need to promote two-stage CMOS amplifier will develop in the direction of multi-function integration and intelligence. It is hoped that in the future, with the advancement of green design and sustainable technology, CMOS amplifiers will also combine energy harvesting technology and environmentally friendly materials to promote the development of electronic systems in a more efficient and environmentally friendly direction.

## 5 Results

In this paper, a two-stage CMOS amplifier is designed to meet specific performance requirements, including DC gain of more than 80dB, -3dB bandwidth of 3kHz, and total current consumption of less than 6μA. In order to improve the stability of the system, the capacitor compensation technology is used, so that the phase margin reaches 83.03°, far exceeding the stability requirements of 40°, so as to ensure that the

circuit can remain stable under different working conditions, and it is not easy to produce oscillation.

In the circuit design process, researchers used a differential input structure to increase the common mode rejection ratio, which provides a stable bias current through the current mirror to improve matching characteristics and temperature stability. More importantly, reasonable parameter selection and optimization make the whole amplifier meet the design requirements of low power consumption while ensuring high gain.

## 6 Conclusion

This paper focuses on the design, optimization and performance analysis of two-stage CMOS amplifiers, focusing on how to control power consumption and improve system stability while meeting high gain requirements. Through the topology of differential inputs, current mirror bias and common source amplifier cascades, the amplifier achieves all the required conditions and optimizes the phase margin through capacitance compensation to ensure its stability meets the requirements of engineering applications.

The final results show that this design can maintain good gain, bandwidth and stability under low power conditions, and is suitable for low power and high-performance applications such as communication and signal processing. But the status quo is not enough. In the future, the circuit structure can be further optimized to meet more stringent application requirements.

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