Optimization of Transient Response in LDOs: An Investigation into Digital-Analog Hybrid Control and Dynamic Gain Compensation

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Abstract. The quick transient response technology of low-voltage differential linear voltage regulators (LDO) has emerged as a research hotspot due to the growing need for dynamic power management in 5G and IoT devices. This article reviews three advanced LDO designs: 1)The dynamic high-impedance charge pump LDO , which suppresses limit cycle oscillations by connecting the output to the power tube grid via an ACHZ loop and employing a 1-bit auxiliary charge pump, achieved a sub-4-FS optimization coefficient (FoM) and a response time of 6.9 ns; 2) The load step reaction time was lowered to 68 ns by hybrid control LDO , in conjunction with digital rough tuning (DLDO) and analog fine tuning (ALDO), using the countable bidirectional binary search (CBBS) algorithm; 3) Adaptive gain layered Miller compensation NMOS LDO dynamically modifies Miller capacitance and pre-weighted reverse bias to maintain 17.5 MHz bandwidth over 0.1-300 mA load range. These solutions are superior to traditional designs in terms of process flexibility, stability, and transient responsiveness. To increase LDO performance in new applications, the future must improve high-frequency noise suppression and optimize static power.

Keywords: Low-Dropout Regulator (LDO), Fast Transient Response, Dynamic High-Impedance Charge Pump, Hybrid Control Algorithm, 5G/IOT Power Management

1 Introduction

Since LDO is the central component of highly integrated power management, the device's stability under dynamic load is directly impacted by its transient reaction speed. Traditional LDOs are costly and difficult to meet the requirements of complex operations since they rely on external capacitors [1]. At the same time, issues like high static power consumption and limited loop bandwidth further limit 5G and IoT applications [2][3]. Although capacitorless design has gained popularity in recent years, issues including low voltage swing rate and inadequate phase margin still need to be resolved [2][4]. There are still inconsistencies between reaction speed and accuracy despite the proposal of many enhancement strategies in literature [1][5] and [6], such

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as digital control and multi-loop compensation. In this regard, literature [7] [8] and [9] has become the subject of current research after achieving a breakthrough in quick reaction performance through creative architecture.

Three primary solutions are the subject of this article: First, the dynamic high-impedance charge pump LDO [10], which suppresses limit cycle oscillations via an AC high-impedance (ACHZ) loop and achieves a sub-4-fs FoM with 6.9 ns response time. Second, the hybrid control LDO [7] combines digital coarse tuning (DLDO) and analog fine tuning (ALDO) through a countable bidirectional binary search (CBBS) algorithm, reducing load step reaction time to 68 ns. Third, the adaptive compensation NMOS LDO [8] dynamically adjusts Miller capacitance and pre-weighted reverse bias to maintain 17.5 MHz bandwidth across a 0.1–300 mA load range. These innovations demonstrate significant improvements in transient response and stability compared to conventional designs.

The article shows the technological evolution path by comparing the aforesaid technique with multi-loop compensation, nonlinear control, and process adaptive design [3] [5] and [6].These innovations surpass traditional designs in flexibility, stability, and transient response.

The first chapter is the introduction, which introduces the research background and significance of the thesis; Chapter 2 details the architecture of the dynamic high-impedance charge pump LDO; Chapter 3 explores the hybrid control algorithm and its implementation; Chapter 4 analyzes the adaptive compensation NMOS LDO design; and Chapter 5 concludes with future research directions, including improvements in high-frequency noise suppression and static power optimization.

2 Dynamic high-impedance charge pump-based LDO design

Reference [10] suggests a charge-pump LDO that primarily operates in analog mode while maintaining the benefits of digital LDO, with the AC connected high impedance (ACHZ) feedback loop serving as the core (Figure 1). The arrangement uses capacitor C_C and a direct coupling of the output V_{OUT} to the power tube gate V_G to provide a quick transient response. In the dead zone between the boundaries, when the LDO is in steady state, the primary charge pump is turned off, producing a higher V_G and current. By connecting the V_{OUT} to the V_G directly through the capacitor C_C, the ACHZ loop is created. V_{OUT} experiences a decrease in direct coupling to V_G via C_C when the load changes suddenly, and the coupling efficiency is set at

$$\eta = \frac{C_C}{C_C + C_G} \tag{1}$$

where C_G is the parasitic capacitance at the gate of the power transistor. This helps to drastically cut response time by rapidly controlling the power tube current I_{MOS} and directly lowering the gate voltage of M_1. Although the ACHZ loop might not always supply all the compensating currents required to bring the LDO's output back to the center of the dead zone, the charge pump helps the V_{OUT} return to the dead zone by further discharging the V_G and raising the current flowing through the power transistor I_{MOS}. In contrast to the conventional RC feedback, the ACHZ loop does not require high

resistance, circumvents the bandwidth restriction of the RC time constant, and uses loop stability analysis to confirm its stability across the whole load range.

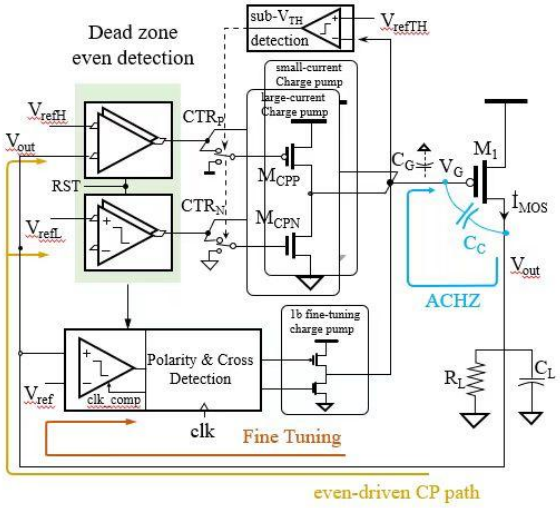

Fig. 1. Charge pump LDO architecture based on ACHZ loop [10]

2.1 Stability analysis and continuous time dead zone detection

Dead zone detection uses upper and lower limit comparators (V_{refH} and V_{refL}) to dynamically manage the charge pump's (CP) start and stop. When V_{OUT} reaches the dead zone, the main charge pump is turned off; with the aid of ACHZ, V_{OUT} will stabilize in the dead zone and maintain a constant state. When V_{OUT} surpasses the dead zone, the charge pump is activated instantly (Figure 2), and V_G is regulated by continuous integration. Experiments reveal that when the load varies at 105 mA, the output voltage lowers by only 88 mV and the steady state ripple is less than 15 mV. Moreover, a 1-bit auxiliary fine-tuned charge pump reduces limit cycle oscillations by raising the grid impedance above 4 MΩ.

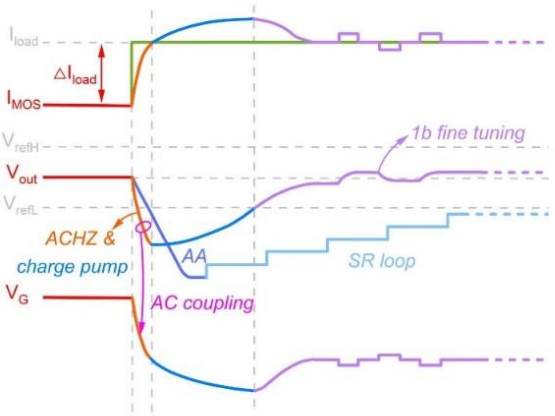

Fig. 2. Dead zone detection and transient response waveform [10]

2.2 Evaluation of performance and experimental outcomes

According to the measured data, when there is no load capacitance, the output ripple is less than 15 mV, the response time is 6.9 ns, and the FoM is as low as 1.8 fs. Compared to conventional analog assist (AA) loops, the ACHZ loop provides a 3.7-fold increase in compensation efficiency under light load (Figure 3). The charge pump and ACHZ loop work together to break the clock cycle restriction and, when paired with dynamic gain control, provide a wide load range and quick response at ultra-low static current (4.9 μA).

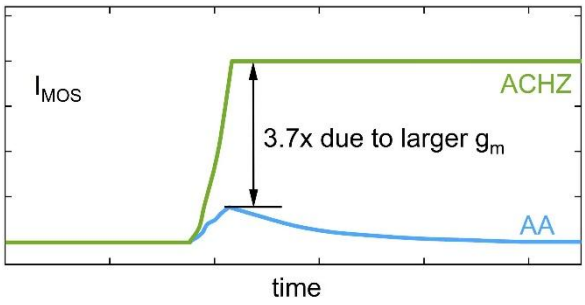

Fig. 3. Comparison of ACHZ and AA loop compensation currents [10]

3 The hybrid LDO's quick transient control algorithm

3.1 Countable Bidirectional Binary Search (CBBS) and Hybrid Architecture

According to literature [7], a hybrid design that combines digital LDO (DLDO), analog LDO (ALDO), and a hybrid controller is suggested (Figure 4). Softswitch switch (SSS) and countable bidirectional binary search (CBBS) are features of the hybrid controller. Both DLDO's coarse tuning and ALDO's fine tuning are combined in the hybrid LDO design. Fast transient response is achieved by DLDO rapidly adjusting the on-number of 256 PMOS switches using the CBBS algorithm to generate coarse modulated current (I_{COARSE}). According to experiments, CBBS responds seven times faster than the conventional shift register method, with a reaction time of 68 ns under a 40 mA load step. Additionally, by avoiding MSB priority switching, the output voltage's instantaneous peak is successfully suppressed.

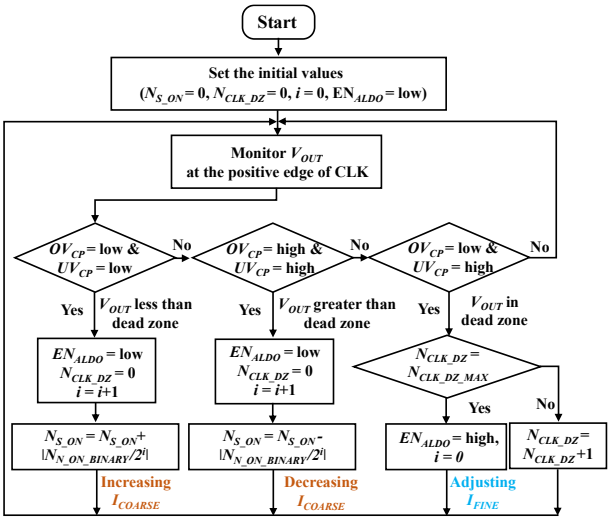

Fig. 4. CBBS control flow diagram for hybrid LDO [7]

3.2 soft swap switching (SSS) and fine regulation

The SSS module dynamically activates the ALDO when the V_{OUT} reaches the dead zone (875-925 mV). This device accurately modifies the fine-tuned current I_{FINE} through an error amplifier (EA), resulting in a highly accurate DC voltage. EA increases loop bandwidth and decreases output impedance by combining a super source follower (SSF) with a folded cascade structure. The test results demonstrate that, with a load step of 40 mA, ALDO achieves a ripple voltage of less than 10 mV and a fine tuning precision of 0.053 mV/mA. By dynamically regulating ALDO's enable signal EN_{ALDO} and only turning on when the load current margin (I_{RM} = I_{LOAD} - I_{COARSE}) surpasses ALDO's maximum capacity, SSS simultaneously prevents redundant power usage.

3.3 Stability analysis of hybrid control

The combination of SSS and CBBS accounts for the high precision of analog regulation and the speed of digital control, making it appropriate for multi-domain power supply requirements in SoC scenarios. By tracking the dead zone's residence duration, the SSS prevents ALDO's limiting oscillation and only permits ALDO there to remove mutual interference between DLDO and ALDO loops; nevertheless, the clock frequency and ripple amplitude must be matched. This design reduces the output voltage ripple to 10 mV and the FoM to 0.117 ps when compared to the typical SR DLDO without the need for an external capacitor. However, the ALDO's static power consumption of 69.1 μA still needs to be adjusted.

4 High conversion rate design with wide load range and no capacitor NMOS LDO

4.1 Wide Range Adaptive Gain Nested Miller Compensation (WAG-NMC)

Literature [8] suggests an output capacitorless NMOS LDO that can enhance transient response by increasing M_N SR and utilizing WAG-NMC technology to boost loop bandwidth (Figure 5). A variable gain amplifier (VGA) dynamically modifies the equivalent values of Miller capacitors (C_{M1} and C_{M2}).

$$C_{M1} = C_{C1}(1 + A_{V2}A_{V3}) \quad (2)$$

$$C_{M2} = C_{C2}(1 + A_{V3}) \quad (3)$$

where A_{V2} is Amp2's voltage gain, which remains constant under all I_{LOAD} circumstances. The variable gain, A_{V3} of Amp3, on the other hand, can change the effective values of C_{M1} and C_{M2} according on I_{LOAD}. Both the primary (ω_{P1}) and secondary (ω_{P2}) poles change in response to the load current (I_{LOAD}). The VGA gain (A_{V3}) drops from 28 dB to 2.9 dB as the load current (I_{LOAD}) rises from 0.1 mA to 300 mA. This causes the ωP1 to move from 5 kHz to 1.2 MHz and the bandwidth to increase to 17.5 MHz. According to experiments, the method requires 79% less compensating capacitance than the conventional approach, only 6.3pF.

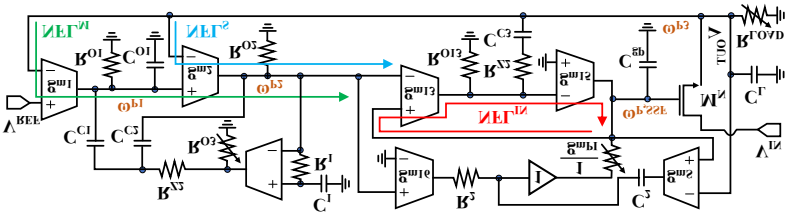

Fig. 5. Small signal model of WAG-NMC [8]

4.2 pre-emphasis inverse (PI) biasing and Supersource Follower (SSF)

PI bias Injects an adaptive bias current (I_{PI}) through an NMOS current source (M_{PI}) to increase the voltage swing rate (SR) of the power tube grid (Figure 6). When low-pass

filtering (R_2, C_2) is used to remove the power ripple path, the PSR drops to -52 dB at 10 kHz. To maintain stability, the SSF uses nested Miller compensation (C_{C3}, R_{Z2}) to drive the internal poles to high frequencies. I_{PI} and I_{LOAD} are negatively correlated, thus V_G rises more quickly at light loads when bias current rises. The bias current decreases at high load, hastening the V_G fall. According to the measured data, the pendulum time is reduced by 56% and the output voltage reduces by just 59 mV with the load step of 299 mA.

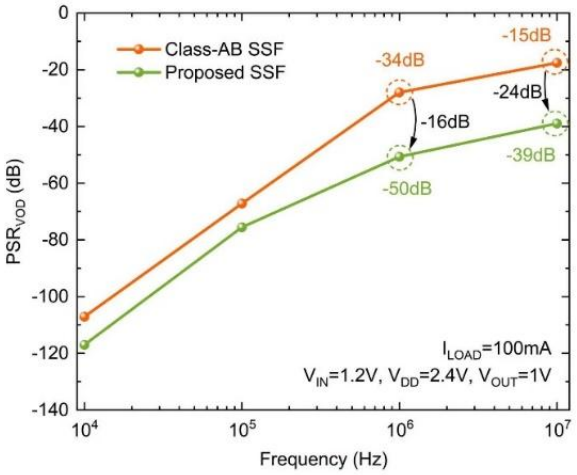

Fig. 6. Comparison graph between the class-AB SSF and the suggested SSF for the simulated PSR from V_{DD} to V_{OUT} [8]

4.3 Stability analysis and double-loop structure

The sub-loop (NFLS) generates left half plane zeros ($\omega_{Z,LHP}$) to counteract the non-dominant pole effects while the main loop (NFLM) supplies high DC gain (86 dB) by directly driving the second stage amplifier (Amp2) through a bypass error amplifier (EA). In contrast to the completely integrated FVF structure in reference [9], which uses a flipped voltage follower to improve full-spectrum power supply rejection, this design's high-frequency PSR performance (-52 dB at 10 kHz) is less reliable.

5 Conclusion

This study thoroughly examines three noteworthy developments in LDO rapid response technology: 1) Charge pump LDO minimizes FoM to 1.8fs via ACHZ loop; to meet the ultra-low power requirements, its static current (4.9μA) still needs to be further tuned.; 2)The hybrid control LDO 's CBBS algorithm increases response speed by seven times; nevertheless, the ALDO module's static power consumption restricts energy efficiency, so it must be further tuned in accordance; 3) Although NMOS LDO 's WAG-NMC

technology increases bandwidth to 17.5 MHz and reduces compensating capacitance by 79%, its high frequency power supply rejection ratio, which is -52 dB at 10 kHz, still requires improvement, though.

Despite the tremendous advancements in transient responsiveness, load range and integration, current research still faces obstacles like multi-scene compatibility and process angle robustness6. Subthreshold bias, adaptive multi-mode control and 6G communication requirements should be combined in the future to support the advancement of LDO technology toward increased intelligence and energy efficiency.

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