



Comprehensive Optimization of Voltage and Ripple of Dc-Dc Converters Based on Multi-Objective Optimization and Data Analysis

Hongxuan Hu

Department of Electrical Engineering, Shanghai Jiaotong University, Shanghai, China

jianghu0820@sjtu.edu.cn

Abstract. With the increasing demand for stable and highly efficient power supply in electronics systems, voltage stability and ripple suppression have gained more significance. For optimization in conventional topology, traditional topology is not able to balance the response speed and the accuracy and increasing switch frequency raises switching losses. The four-switch Buck-Boost converter possesses many advantages, such as a simple structure, a wide range of input and output voltage, and bidirectional voltage conversion. This paper utilizes a four-switch Buck-Boost converter with PID control and proposes an integrated multi-optimization method to help solve the conflict between voltage accuracy and ripple performance. Based on the topology of the four-switch Buck-Boost converter, this paper builds a mathematics model of the circuit and simulation model. After comparing multiple groups of data, the optimal inductor value and equivalent series resistance (ESR) under the given conditions are $470\mu\text{H}$ and 0.01Ω respectively. The ripple coefficient is reduced to 4.7%, and the efficiency reaches 85%, meeting the design requirements. This paper provides electric vehicles, and renewable energy systems with theoretical and practical optimization of voltage stability and ripple suppression.

Keywords: Voltage Stability, Ripple Suppression, Multi-Optimization

1 Introduction

DC-DC converter is an essential part of energy conversion components in power electronics systems, widely applied in the fields of renewable energy, electric vehicle systems, industrial power supply, and portable electric devices. Its performance directly affects system reliability and power stability. However, with the application scenario being more complicated and user demand being more diverse, conventional converter designs are faced with multiple challenges.

1.1 Voltage Stability

Load resistance changes and input variation are two common factors that influence voltage stability [1]. When the converter is applied to the field of electric vehicles, varied driving speed brings different loads on the motor, thereby causing the load of the converter to change simultaneously. Likely, since the input voltage of renewable energy (such as wind or photovoltaic energy) has a wide fluctuation range, the converter must maintain stable output voltage within a wide input voltage range. Approaches such as improved back-stepping control(BSC) and input-series output-parallel (ISOP) are proposed to raise the stability [2, 3]. The core of BSC is to divide the complex system, design a control algorithm for each layer, and compensate for the non-linear terms, finally, it will drive the system to reach stability. However, BSC relies heavily on a precise mathematical model of the circuit. If the precise model can not be achieved, BSC is very likely to lose its control capability, resulting in a voltage overshoot. ISOP connects the input ends of multiple converters in series and the output ends in parallel. The method must guarantee the balance of input voltage and output current, which makes the control more complicated.

1.2 Ripple Suppression

To improve the power density, modern DC-DC converters tend to apply a high-frequency switching technique. High-frequency switching will give rise to a significant increase in switching loss and electromagnetic Interference (EMI), which will generate harmonics and ripple. The common existing method for eliminating ripple is introducing a passive filtering network [4]. In order to remove the high-frequency harmonics, the low-pass filter as shown in Figure 1 is considered.

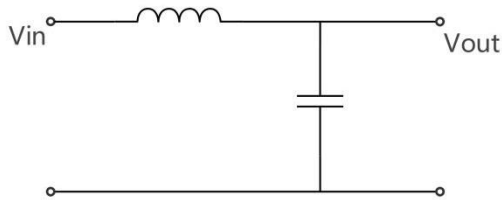


Fig. 1. LC low-pass filter

In a low-pass filter, the inductor presents a high impedance for the high-frequency signal which prevents high-frequency current from passing through while the capacitor presents a low impedance which provides a bypass path for the high-frequency component. The capability of the LC low-pass filter to eliminate ripples is determined by the inductance and capacitance, the metric is crossover frequency.

$$f_c = \frac{1}{2\pi\sqrt{LC}} \quad (1)$$

Where f_c is crossover frequency, L is inductance and C is capacitance.

Components with a frequency higher than the crossover frequency can not pass through the filter, while those with a frequency lower than it can (in ideal circumstances) [5].

1.3 Multi-Optimization

In DC-DC converter design, multi-optimization is aimed to balance and coordinate several metrics at the same time. This approach becomes significant in circumstances where conventional single-target methods (such as BSC require precise circuit modeling and ISOP demands complex voltage/current balancing) struggle to make the voltage as stable as it can be while the ripple suppression or the complexity of algorithms is ignored. Its core lies in using mathematical modeling and optimization algorithms to search for the optimal solution. This optimal solution can simultaneously optimize every metric and achieve the best balance under the constraint conditions, although every metric itself does not reach its optimal point. The specific method for finding the optimal solution is as follows: list the influential factors; by adjusting those parameters and by comparison, we can obtain the optimal solution and balance point.

2 Theory and basic principle

2.1 Voltage Stability

IEEE committee defines voltage stability as: Voltage stability is the ability of a system to maintain voltage so that, when load admittance is increased, load power will increase, and so that both power and voltage are controllable [6]. Voltage stability in power electronics systems is easily affected by a variety of factors:

Control algorithms: Different control algorithms lead to varied voltage stability performance. Two commonly used control algorithms are hysteresis control (HC) and sliding mode control (SMC). HC indicates that if the measured current or voltage is higher or lower than the determined value, the control system will switch the output voltage value until the deviation is eliminated [7]. SMC is a non-linear control method, it designs a special “sliding surface”. The controller forces the system to reach this surface within a limited time and then the system slides along the sliding surface to the balance point [8]. SMC has a chattering phenomenon, which will cause low control accuracy and high thermal loss, hence the output voltage cannot be very stable. Moreover, the main common problem of hysteresis control and sliding mode control is that they are suitable for variant systems since the frequency is variable.

Power component parameters: The basic equation of a capacitor is

$$C = \frac{\Delta Q}{\Delta U} \quad (2)$$

Where ΔQ is the change of charge and ΔU is the change of voltage applied to the capacitor.

If the load changes rapidly, there will be current flows through the capacitor, which gives rise to ΔQ and ΔU , hence the smaller the capacitance is, the more volatile the voltage fluctuates. Moreover, Every component has its parasitic parameters, such as the

equivalent series resistor (ESR) of capacitors. The value of ESR varies from the frequency and temperature. When the value of ESR increases, a voltage drop will be generated, which has a significant effect on voltage stability.

2.2 =Ripple Suppression

Ripple indicates the AC component superimposed on the DC output voltage. In buck converter, ripple is generated by the capacitor. When operating at continuous conduction mode(CCM), the inductor current completes one cycle of rising and falling within a single switching period, which also accomplish a single charge and discharge cycle on the capacitor. According to the basic equation of capacitor mentioned, there will be voltage fluctuation on output side.

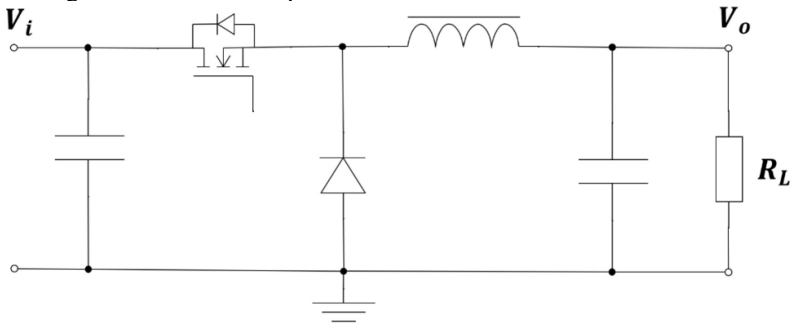


Fig. 2. Buck converter topology

Figure 2 shows the simplest DC-DC converter: Buck converter, it can be obtained that the capacitance(C), inductance(L) and ESR can all affect ripple. The ideal equation(parasitic parameters are not considered) of ripple in Buck converter is

$$\Delta V = \frac{D(1-D)V_{in}}{8LCf_s^2} \tag{3}$$

Where D is the duty cycle of the switching signal, F_s is the switching frequency of MOSFET.

Consequently, a larger inductance leads to a smaller voltage ripple. Hence, ripple can be suppressed by adjusting the inductance(when other parameters are fixed).

Ripples can also be reduced by replacing the inductor with an auto-transformer with an auxiliary filter capacitor to reach zero-voltage-ripple(ZVR) DC-DC converter, but the auto-transformers are usually too large in size, making it unsuitable for certain circumstances where compact power electronic converters are required, such as portable charge bank, laptop and Programmable Logic Controller (PLC) modules [9].

2.3 Multi-Optimization Method

Voltage stability and ripple suppression typically represent a pair of contradictory metrics, both can not be satisfied simultaneously. The analyses are as follows.

Inductance: As is analyzed, large inductance can reduce the ripple. However, when the switch is turned on and the inductance is too large because the voltage of inductance is:

$$V_L = L \frac{di}{dt} \quad (4)$$

The inductor current rises slowly, giving rise to insufficient capacitor charging. The output voltage will increase dramatically and then the energy stored in inductor cannot be released quickly, which give rise to reverse current surge, making the output voltage drop to 0.

Capacitance and ESR: High-capacitance capacitors can store more energy and reduce the voltage deviation when the load is changing, and it is also capable of reducing the ripples. However, excessively large capacitance may potentially lead to insufficient phase margin and system oscillation and the output voltage will also become zero when the system reaches its steady state. Additionally, lower ESR can suppress the ripple in the DC-DC converter [10]. However, ESR can improve the system's dynamic response since it introduces zero to the feedback system.

Control algorithms: Proportional-integral-derivative control (PID control) is widely used in the automatic control systems. Unlike HC and SMC, PID control possesses constant frequency and simple structure. As is shown in Figure 3, it includes three critical processing parts: proportional, integral and derivative [11]. The error is sent to the three data processing units and through feedback, the error will finally be eliminated or reduced to 0.

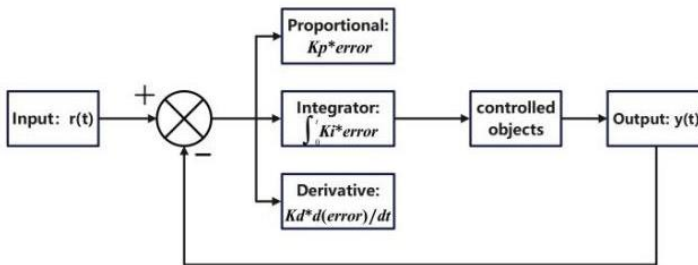


Fig. 3. Flowchart diagram of PID control

The response speed is determined by proportional gain K_p while the steady-state error is determined by integrator gain K_i . An excessively large value of K_i may lead to system overshoot or oscillation. Therefore, it is necessary to balance the steady-state error and dynamic performance.

In the design of Four-switch converters, inductance, capacitance, ESR, K_p , and K_i all require a global optimization, not just focusing on one metric. The essence of multi-optimization lies in coordinated parameter design and finding a balance among the above conflicting metrics, therefore reaching both voltage stability and small ripple. So this paper utilizes a four-switch Buck-Boost converter. It is a converter that features four switches in a DC-DC converter. It can be used as a bidirectional converter, which means that the two ports can act as an output terminal or an input terminal. Four-switch buck-boost converters have a wide range of input and output voltage, which meets the

demand for renewable power systems. The control algorithm uses PID control. PID control does not require complicated mathematical models or calculations and it has strong adaptability. Moreover, since it is easy to implement and has low hardware cost, it can be also widely applied to industrial production.

3 Methodology

3.1 Research Goals

This paper aims to use a multi-optimization method, to design a four-switch buck-boost converter, enabling it to satisfy the following core metrics under a condition of wide input voltage range and dynamic load: the voltage deviations required to be less than 5V, the ripple coefficient is restricted to be lower than 5%, circuit size determined by the inductance(L) is required to be small and the lowest efficiency is above 85%.

By quantifying the voltage stability and ripple, and combining simulation data with optimization algorithms, this study explores the globally optimal parameter combination, hence providing a multi-optimization-driven design paradigm for the power electronics system under multiple conditions.

3.2 Research Concept

The research is based on the following theoretical framework and assumptions:

Four-switch buck-boost converter: using the bidirectional DC-DC converter and its wide input and output voltage range, guarantees the converter can afford the various voltage level.

PID control theory: utilizing the robustness and fast response of the proportional-integral-derivative control, combine it with the feedback compensation to suppress the ripple, and ensure the voltage fluctuation is low.

Circuit simulation circuit: simulate the behavior of the real circuit through high-precision simulation models, and the influence of the parasitic parameters is also considered in the model.

Multi-optimization: based on the concept of the Pareto optimal solution, balance the conflicts between voltage stability, ripple, and volume.

Zero voltage switching(ZVS): ZVS techniques reduce the switching loss by optimizing the switching process, which enables the switches to be considered as ideal devices.

3.3 Research Method

This paper adopts a method that includes mathematical modeling,high-precision simulation, and multi-optimization.

Mathematical Modeling.

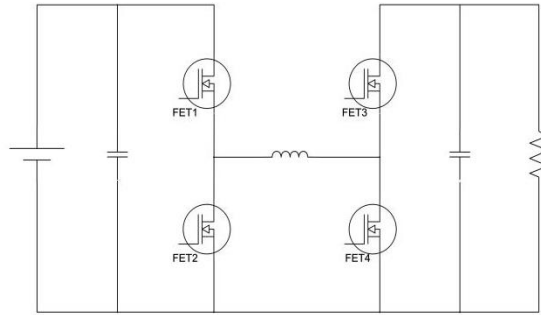


Fig. 4. Topology of four-switch buck-boost converter

The four-switch buck-boost converter topology is shown in Figure 4; it is composed of a special combination of four MOSFETs to enable both step-down(buck) and step-up(boost) operations using one single inductor. Every MOSFET has its parasitic free-wheeling diode. FET1 and FET4 share the same control signal, and FET2 and FET3 share a control signal which has a phase opposite that of the trigger signal shared by FET1 and FET4. The converter in this paper operates in buck-boost mode. FET1, FET2, and FET3, FET4 compose a bridge, respectively (Every MOSFET is considered an ideal device, which has no switching loss). There is an inductor connecting the two bridges. The input capacitor filters the input voltage ripple, and the output capacitor smooths the output voltage.

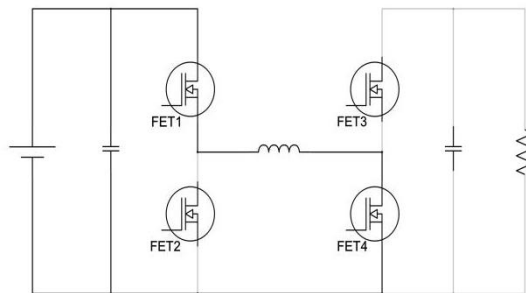


Fig. 5. FET1 and FET4 are turned on

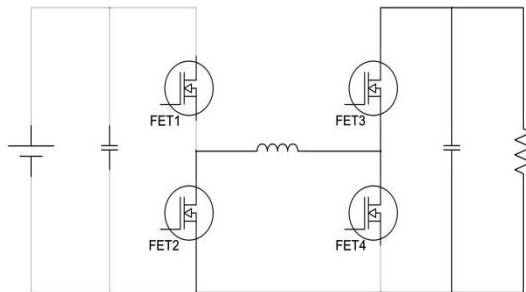


Fig. 6. FET2 and FET3 are turned on

In Figure 5, FET1 and FET4 are turned on, the voltage of the inductor

$$V_L = V_{in} \tag{5}$$

At this period, the inductor stores energy.

In Figure 6, FET2 and FET3 are turned on, the voltage of the inductor

$$V_L = V_{out} \tag{6}$$

At this period, the inductor releases the energy.

According to the basic equation of the inductor

$$V_L = L \frac{di}{dt} \tag{7}$$

Utilizing the voltage-second balance(in a stable switching cycle, the integral of voltage across an inductor over one complete period must equal zero), the relationship between input and output voltage is

$$V_{in}T_{on} = V_{out}T_{off} \tag{8}$$

Hence the voltage gain

$$K = \frac{V_{out}}{V_{in}} = \frac{T_{on}}{T_{off}} = \frac{d}{1-d} \tag{9}$$

Where d indicates the duty cycle of the control signal.

Control Algorithms. PID control is a feedback control algorithms that is widely applied on industrial automation system. By changing the parameters, it adjusts the system output to achieve target point. However, the derivative factor will enhance the high-frequency noise, so this paper use PI control as the close-loop control algorithm.

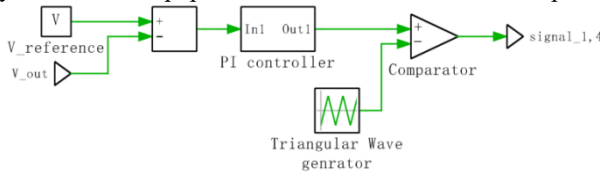


Fig. 7. Generation of the control signal

Figure 7 presents the generation of control signal. The process is that the reference voltage(\$V_{reference}\$) is compared to the actual output voltage (\$V_{out}\$) to generate an error signal, which is fed into a PI controller for dynamic adjustment. The PI controller processes the error and the result is compared with a high-frequency triangular wave. The comparator outputs pulse-width modulated (PWM) switching signals (control signals of FET1 and FET4), which drive the power switches.

Multi-Optimization. The metrics which are desired to optimize are voltage deviations, ripple coefficient, size of the converter, and efficiency. So the target functions can be obtained:

$$\text{minimize } \Delta V = V_{max} - V_{min} \tag{10}$$

$$\text{minimize } \gamma = \frac{V_{max}-V_{min}}{V_{DC}} \times 100\% \tag{11}$$

$$\text{minimize } L \tag{12}$$

$$\text{maximize } \eta = \frac{P_{out}}{P_{in}} \tag{13}$$

Where ΔV is the voltage deviation, γ is the ripple coefficient and η is efficiency.

Considering the application and real device parameters, the input or output voltage

$$20V < V_{in} < 60V \quad (14)$$

The current of the inductor

$$I_L < 30A \quad (15)$$

4 Simulation and Results

In order to minimize the size, the converter initially operates under these working conditions:

Input voltage: 50V

Output voltage: 40V

Inductance: 10 μ H

Capacitance: 100 μ F

ESR of capacitor: 0.1 Ω (aluminum electrolytic capacitor)

Switching frequency: 20kHz

K_p :0.005 K_i :0.5

Output resistance: 5 Ω

The output voltage waveform is shown in Figure 8:

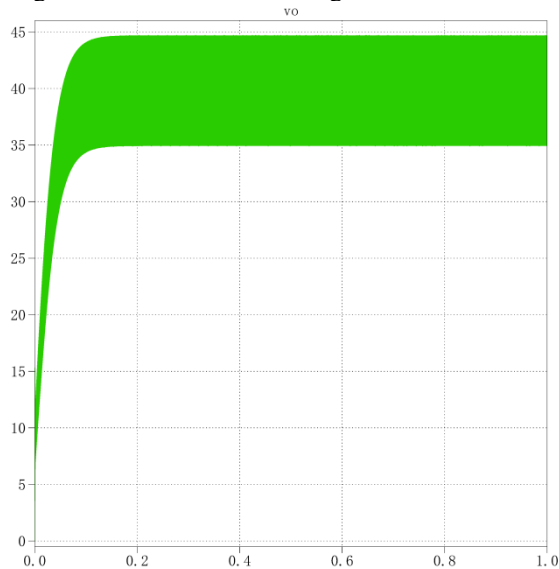


Fig. 8. Output voltage waveform ($L=10 \mu H$, $ESR=0.1 \Omega$)

Steady-state output voltages measured with the cursor function range from a minimum of 34.93V to a maximum of 44.69V, hence $\Delta V=9.76V$, $\gamma=24.4\%$, which does not satisfy the requirements.

Next, adjust the ESR to 0.01 Ω (ceramic capacitor), obtain the output voltage, the output voltage waveform is shown in Figure 9:

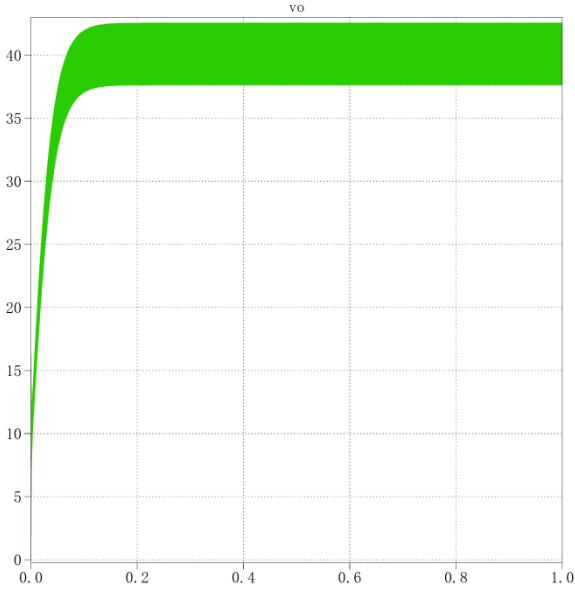


Fig. 9. Output voltage waveform ($L=10 \mu H$, $ESR=0.01 \Omega$)

$\Delta V, \gamma$ are 4.95V and 12.4%, respectively.

To reduce the ripple coefficient, the inductance has to increase, which means that the volume will increase, too. The inductance continues to be raised to $47 \mu H$ and $470 \mu H$ and under each inductance uses both the ceramic capacitor ($ESR=0.01 \Omega$) and aluminum electrolytic capacitor ($ESR=0.1 \Omega$). In the simulation model shown in Figure 10 and 11, the parameter adjustments are accomplished. Finally, a comparison table can be made.

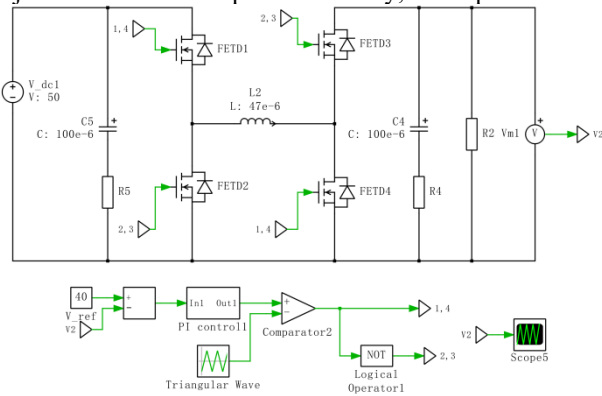


Fig. 10. Simulation model($L=47 \mu H$)

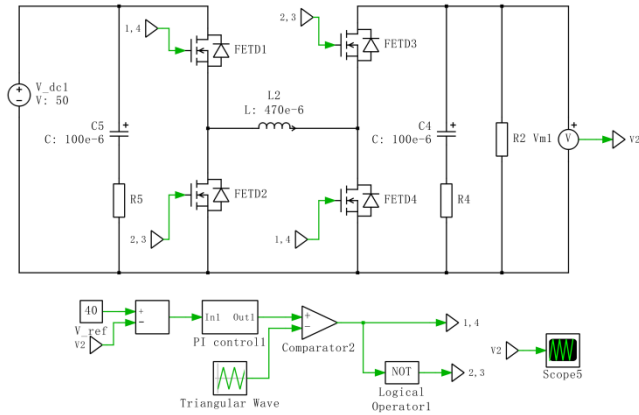


Fig. 11. Simulation model($L=470\mu\text{H}$)

Table 1. ΔV , γ and η under different operation conditions

Inductance and ESR	Voltage deviation ΔV	Ripple coefficient γ	Efficiency η
$10\mu\text{H}$, 0.01Ω	4.95V	12.4%	89.23%
$10\mu\text{H}$, 0.1Ω	9.76V	24.4%	86.23%
$47\mu\text{H}$, 0.01Ω	2.03V	5.1%	89.53%
$47\mu\text{H}$, 0.1Ω	3.13V	7.8%	88.39%
$470\mu\text{H}$, 0.01Ω	1.88V	4.7%	89.40%
$470\mu\text{H}$, 0.1Ω	3.03V	7.6%	88.77%

Table 1 indicates that the smaller ESR and the larger inductance will both reduce the voltage deviation and ripple coefficient. The only condition which satisfies the requirement is $470\mu\text{H}$, 0.01Ω and the efficiency of the circuit is 85% additionally.

As a result, under the condition that input voltage=50V, output voltage=40V, ripple coefficient<5% and the inductance should be lowest, the Pareto optimal solution is adjusting the inductance to $470\mu\text{H}$ and using a capacitor possessing ESR of 0.01Ω .

5 Conclusion and outlook

This paper proposes a multi-optimization-based method to make voltage deviation and ripple coefficient decrease. Through mathematical modeling and simulation analyses, the optimal inductance ($470\mu\text{H}$) and resistance (0.01Ω) are identified. The voltage deviation is reduced to lower than 5V and the ripple coefficient is lower than 5%, which achieves a balance between voltage stability, ripple suppression, and volume of the converter and satisfies the requirements of a wide range of input and output voltage. Future studies can focus on improved control algorithms (such as intelligent control), devices with lower loss, and experiment templates for the real circuit. This paper provides a theoretical and practical foundation for power electronics system design and enables broader application in renewable energy systems and electric vehicles.

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