



Digital Integrated Circuit Design Automation Based on Artificial Intelligence

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Abstract. Digital integrated circuit (IC) design is a laborious and intricate process that involves many processes of differing complexity. It takes a lot of time and increases the possibility of mistakes when done by hand, especially for inexperienced designers, from specification to layout and verification. A new design automation framework is needed to address the growing complexity of digital integrated circuit design. In order to maximize the burden associated with engineering design, people also want sophisticated artificial intelligence-driven technologies. Thus, the research topic of this article is that “Digital Integrated Circuit Design Automation Based on Artificial Intelligence”. This article argues and discusses various ways to achieve digital integrated circuit design automation from the perspective of digital integrated circuit design automation and digital integrated circuit design automation based on artificial intelligence. As a result, different methods have their own advantages, and there are also some future directions for AI/ML in VLSI. The digital integrated circuit automation based on artificial intelligence still holds significant potential for further development.

Keywords: VLSI, EDA, LCMs, DL models

1 Introduction

Over the past five years, the semiconductor industry has faced a supply-demand imbalance due to global events such as the Covid-19 pandemic, leading to widespread chip shortages. Meanwhile, demand for electronic devices has surged. Consequently, in order to close the gap between supply and demand and speed up time to market, electronic design automation, or EDA, has become crucial. Even with decades of progress in EDA technology, human interaction is still necessary for these time-consuming and labor-intensive jobs. The rapid advancement of machine learning (ML) and artificial intelligence (AI) has enabled a multitude of new applications in EDA tools for IC design [1]. EDA is used to design semiconductor integrated circuits (ICs) using CAD technology. It has grown to be one of the most important fields in electrical engineering over time. A crucial part of artificial intelligence, machine learning imitates human learning processes and is expected to become a significant trend. Machine learning based electrical design automation is still in its infancy and

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faces several challenges, despite the fact that machine learning approaches can improve the functionality of EDA today [2]. AI-based digital integrated circuit design automation experiences the same issue. In recent years, the rapid advancement of AI has significantly intertwined with integrated circuit technology, making their combination a key development direction in information technology. The synergy between integrated circuits and AI is profound. The continuous enhancement of ICs has fueled the rapid growth of computer technology, which is essential for AI development. AI's reliance on advanced computing capabilities means its progress is closely tied to the evolution of integrated circuits [3]. So it is very important to analyze existing methods and find the future direction of digital integrated circuit design automation based on artificial intelligence. Thus, this article will discuss about "Digital Integrated Circuit Design Automation Based on Artificial Intelligence". First of all, this article will discuss the development and application of digital integrated circuit design automation, primarily focusing on artificial intelligence and machine learning methods. Secondly, it will point out some future directions of digital integrated circuit design automation.

2 Digital Integrated Circuit Design Automation

2.1 Advancements in Machine Learning-driven EDA

EDA is a popular tool in both engineering and academia for designing integrated circuits. These days, the growth of EDA faces numerous obstacles. A fresh strategy is presented to improve EDA by applying machine learning (ML) techniques, covering almost every step of the chip design process, in order to address these difficulties with EDA development. ML approaches have recently provided exceptional modeling and search performance in a variety of applications [2]. As shown in Figure 1, there has been a significant increase in ML methods, which can be classified into various categories.

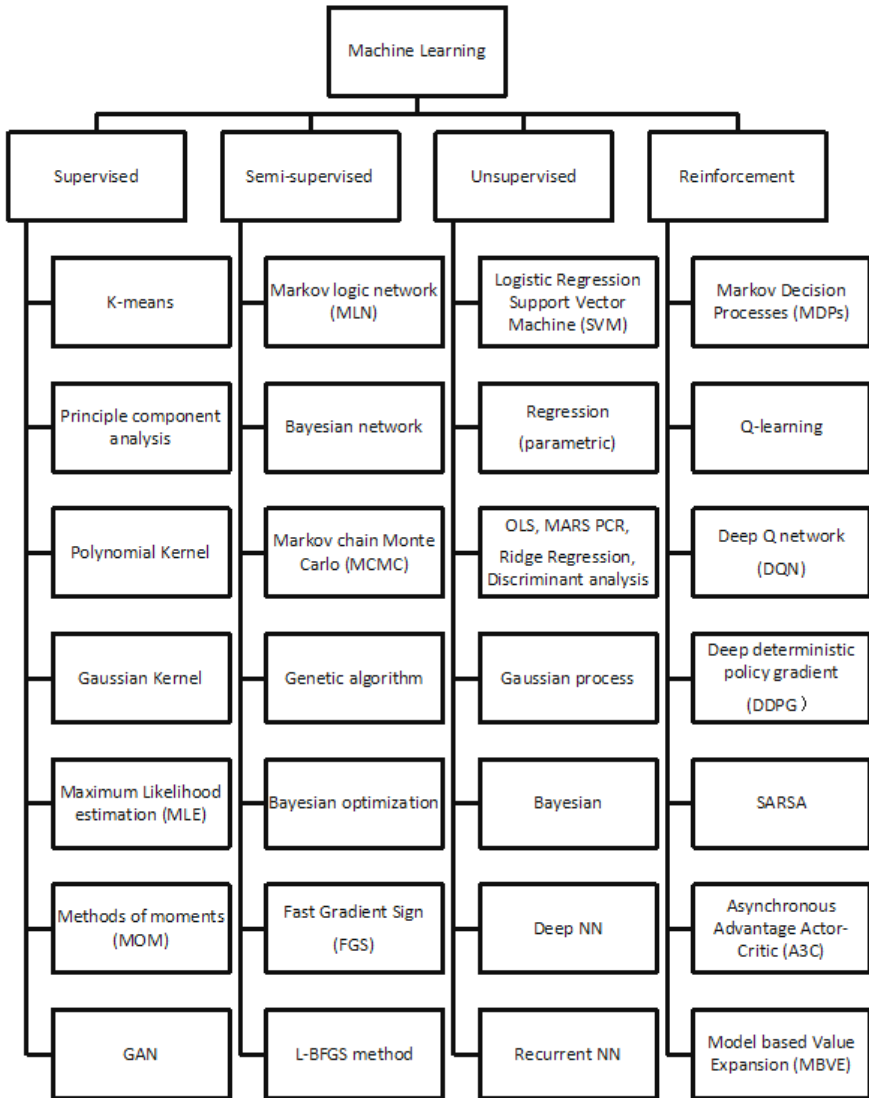


Fig. 1. Classification of ML Methods [2]

The current perspective on machine learning in EDA centers on applying ML approaches to increase the effectiveness of physical design processes like floor planning, layout routing, and clock tree synthesis (CTS). CTS is crucial for implementing the clock network in digital IC design. Conventional CTS treatments result in increased currents at the clock activity's peripheral. Machine learning approaches, such as reinforcement learning, optimize the distribution of clock arrivals to reduce these peaks. Additionally, GAN-based methods, known as GAN-CTS,

utilize neural networks to predict efficient tree structures, thereby lowering energy consumption and improving overall system performance [4].

Although distinct in the chip design process, Floor planning and Placement are two crucial back-end stages. Both involve significant algorithmic complexity and high computational demands. Finding logic blocks inside the IC and aligning them with the field-programmable gate array (FPGA) architecture is the primary responsibility of the stages. Integrating machine learning (ML), especially reinforcement learning (RL), can enhance these stages by enabling self-improving models trained on historical data [5]. Combining ML with traditional algorithms improves placement accuracy and efficiency while maintaining robustness, presenting a promising approach for optimizing modern IC design workflows.

During the final back-end design phase, EDA routing optimizes interconnects within wirelength constraints. Machine learning improves this process: a CNN called RouteNet, along with a custom FCN, predicts routing paths, while an 18-layer ResNet forecasts design rule violations (DRVs), speeding up error detection and route optimization. Beyond routing, ML extends to lithography simulation, mask synthesis, and front-end circuit design using CNNs and GNNs, enhancing overall EDA efficiency by automating traditionally labor-intensive tasks [6].

2.2 Large Circuit Models

AI is now the primary force behind electronic design automation, replacing task-specific AI-augmented EDA (AI4EDA) with AI-native EDA. The development of LCMs, which are fundamental models pre-trained on multimodal circuit data like as specifications, RTL designs and netlists, is essential to achieving this goal. Unlike current methods that adapt generic AI tools, LCMs are specifically designed to handle the unique complexities of circuit data, effectively managing the interplay of computation, structure, and physical constraints, as supported by recent studies. By integrating AI directly into the design process, this framework enables comprehensive synthesis and optimization, bridging gaps between high-level intent and low-level implementation [7].

For the advancing multimodal circuit representation learning, the work introduces unimodal encoders tailored for specific design stages, including natural language processing for specifications, graph neural networks for RTL/netlists, and vision-inspired models for layouts. These encoders capture domain-specific semantics and structural nuances, such as logic functionality and geometric details. Building on this, there are cross-modal alignment techniques, including contrastive learning, masked modeling, and shared latent spaces, to harmonize representations across stages, such as aligning RTL with netlists or specifications with physical layouts. This multimodal fusion ensures design intent preservation and facilitates unified reasoning across abstraction levels, a critical advancement for end-to-end design automation [7].

Logic synthesis optimization, equivalency checking, physical design automation, and specialized circuit design, including standard cells, datapaths, and analog circuits, are some of the transformative applications of LCMs. Through structural and functional embeddings, case studies demonstrate how LCMs have the ability to

transform activities such as SAT-solving. This paper preliminary results from accelerating SAT-sweeping for industrial logic equivalence checking scenarios C1 through C6 using the netlist encoder are shown in Table 1, with the values shown in bold [8].

Table 1. A comparison between the runtime performance of SAT sweepers and the frequency of SAT calls [8]

Circuit	SAT calls			Total runtime (s)		
	[290]	Ours	Red. (%)	[290]	Ours	Red. (%)
C1	13826	570	95.9	7.5	3.2	57.8
C2	100	74	26.0	5.4	3.1	42.7
C3	4	1	75.0	19.1	9.1	52.3
C4	20	12	40.0	6.5	4.0	37.8
C5	6	4	33.3	0.5	0.2	56.3
C6	10	5	50.0	0.3	0.2	50.0
Avg.	-	-	53.4	-	-	49.5

3 Digital Integrated Circuit Design Automation Based on Artificial Intelligence

3.1 Image Analysis Framework Using Deep Learning

There is the first fully automated DL - based framework for analyzing Scanning Electron Microscope (SEM) images of digital integrated circuits. These steps play a crucial role in ensuring hardware assurance, covering all critical stages such as image stitching, feature extraction, and image stacking. Unlike current methods that depend on classical image processing or partial automation, this framework incorporates DL at every stage. For instance, image stitching uses phase correlation but replaces manual misalignment checks with a DL-based Faster R-CNN detector. Feature extraction leverages DL models for tasks such as standard cell detection and via segmentation. The framework's end-to-end automation significantly minimizes human intervention, addressing the inefficiencies of traditional workflows, which are slow, error-prone, and labor-intensive. This comprehensive approach establishes a new benchmark for hardware assurance pipelines by significantly reducing human intervention and improving processing efficiency [9].

There are two innovative deep learning architectures aimed at addressing hardware assurance challenges. Firstly, a Faster R-CNN model with ResNet-50 backbone automates stitching misalignment detection — a process traditionally done manually. The model was trained on synthetic data created by automatically cropping and shifting SEM image patches. It attains high accuracy (AP = 0.9334) and demonstrates robustness against noise. Secondly, a custom regression model with a VGG-16 backbone and differential learning rates is designed for stacking movement

regression, which predicts horizontal/vertical adjustments needed to align layers. This architecture achieves pixel-level precision (RMSE = 2.47) and removes the necessity for manual selection of stacking points. The advancements in Faster R-CNN and custom regression models showcase how domain-specific deep learning architectures can effectively tackle issues that classical methods find difficult to address [9].

A significant challenge in adopting DL is the cost of preparing labeled training data. It can be tackled by generating synthetic data and using preliminary model-assisted annotations. Synthetic misalignment training data are produced by algorithmically shifting image patches. On the other hand, standard cell detection data combine scrambled backgrounds with pasted cell images. In high-noise situations, a preliminary DL model trained on limited data—such as one image with extensive augmentation—generates cleaner ground truth, reducing manual correction efforts by up to 70% compared to traditional methods. This method not only speeds up data preparation but also ensures scalability across various IC image sets, making DL practical for real-world applications [9].

To enhance practicality, the framework focuses on model reusability by allowing DL models to process feature images (such as extracted vias and metal lines) rather than raw SEM images. These feature images eliminate technology-specific variations, such as SEM imaging artifacts. This enables models trained on one IC design to apply to others without needing retraining. For example, the misalignment detector maintains consistent performance across feature images from different ICs, while the stacking regression model generalizes across various layers. This strategy reduces deployment costs and addresses a key limitation of classical methods, which often require manual parameter tuning for new datasets [9].

3.2 Integration with Industrial EDA Tools

There are many types of the integration with industrial EDA tools, like co-design of algorithms and hardware, human-in-the-loop systems and yield-aware optimization. The co-design of algorithms and hardware proposes FPGA/GPU-accelerated ML pipelines, such as XT-PRAGGMA for crosstalk analysis, ensuring compatibility with existing tools like Cadence Innovus and Synopsys IC Compiler. Human-in-the-loop systems suggest hybrid workflows that use machine learning models to provide recommendations, such as DesignAdvisor for asynchronous CAD tasks, allowing engineers to iteratively refine predictions. Yield-aware optimization introduces ML-driven design-technology co-optimization (DTCO) to address manufacturing variability and performance targets simultaneously, as shown in 5nm node experiments [10].

3.3 ShortCircuit

Nowadays, there is a new integration framework between ChatGPT, a cutting-edge language model, and EDA tools like OpenLane, facilitating end-to-end automation from natural language specifications to synthesizable RTL code and OpenLane configuration files. This reduces the need for manual coding and configuration,

making it easier for non-expert designers to get started. The framework presents ShortCircuit, an open-source toolchain that integrates ASIC (SkyWater 130nm CMOS) and FPGA (such as GOWIN) design processes. The toolchain uses modular scripting and a Python-based GUI to simplify design creation, physical implementation (including GDSII/bitstream generation), and layout visualization through open-source tools like Magic and Klayout, promoting a collaborative and accessible design environment. It initiates a paradigm shift in EDA by utilizing NLP to move from expert-driven workflows to demand-driven automation. This innovation not only makes IC design more accessible but also lays the groundwork for future "Specification-to-Silicon" systems, where AI interprets high-level requirements to generate fabrication-ready outputs with minimal human involvement [1].

3.4 Co-Design Optimization of Dedicated AI Chips

The integration of AI and IC technology has led to significant advancements in the co-design of dedicated AI chips, enhancing performance, energy efficiency, and automation. A key aspect of this progress is the development of specialized hardware architectures designed for AI workloads. For example, Google's Tensor Processing Unit (TPU) uses a multiplier-accumulator (MAC) array to accelerate complex operations, such as convolutions in convolutional neural networks (CNNs). By parallelizing large-scale matrix computations, MAC arrays significantly reduce processing time and optimize energy use. Compared to traditional CPUs and GPUs, TPUs offer a 15–30× speedup and 30–80× improvement in energy efficiency, making them essential for real-time execution of AI-driven design automation tasks like layout optimization and simulation. This architectural innovation meets the increasing need for high-throughput processing in modern IC design workflows [3].

Beyond hardware acceleration, system-level optimizations are crucial for overcoming bottlenecks that impede computational efficiency. One significant challenge is the "memory wall," where memory bandwidth and latency limit the full use of processing power. To address this, dedicated AI chips incorporate high-bandwidth memory (HBM) and optimize data flow architectures. HBM's stacked design and wide interfaces boost memory throughput, while optimized data pipelines reduce redundant data transfers between memory and processing units. These improvements ensure smooth interaction between AI algorithms and hardware, enabling efficient deployment of resource-intensive tools like machine learning-based circuit optimizers. For instance, in large-scale IC designs, reduced data latency allows iterative simulations to converge more quickly, speeding up design cycles and enhancing productivity [3].

The synergy between AI algorithms and IC hardware creates a bidirectional feedback loop, promoting continuous improvements in both fields. AI-driven design tools utilize the computational power of specialized chips to iteratively refine circuit layouts, predict performance outcomes, and automate parameter tuning. Conversely, hardware architectures adapt to support emerging AI models, such as dynamically reconfiguring memory hierarchies to meet deep learning's massive data needs or enhancing parallelism for reinforcement learning-based optimization. This co-

evolution addresses challenges like non-linearity and fault tolerance, paving the way for scalable solutions in high-density, high-complexity IC designs. By aligning algorithmic intelligence with hardware capabilities, the co-design paradigm ensures that advancements in AI and IC technology mutually reinforce each other, driving the development of next-generation intelligent, energy-efficient electronic systems [3].

3.5 Future Directions for AI/ML in VLSI

There are some future directions for AI/ML in VLSI, including transfer learning and meta-learning, quantum machine learning, generative models for design automation and collaborative benchmarking [10]. For transfer learning and meta-learning, utilizing insights from established technologies, such as 7nm processes, to expedite the development of cutting-edge innovations like 3nm GAAFETs. Meta-learning frameworks can facilitate quick adaptation to new design guidelines or materials. The suggested approach for developing a learning system that uses transfer learning to examine device behavior in next technological nodes is shown in Figure 2 [10].

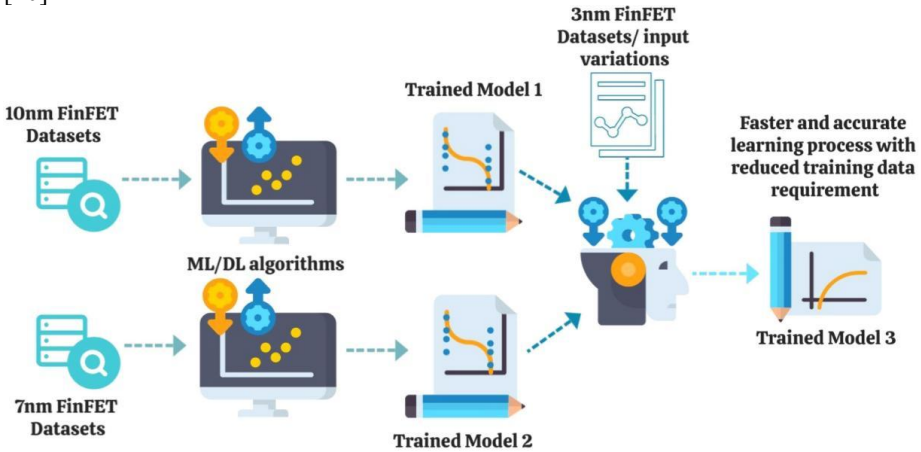


Fig. 2. The suggested inductive transfer learning block diagram for device modeling at future lower technology nodes [10]

For quantum machine learning, quantum annealing and variational algorithms, such as VQE, are suggested for addressing NP-hard placement and routing challenges, potentially surpassing classical heuristics in terms of scalability. For generative models for design automation, Generative Adversarial Networks (GANs) and diffusion models can automate tasks such as layout generation, constraint-aware floorplanning, and lithography mask synthesis, thereby decreasing dependence on human expertise. For collaborative benchmarking, there is a call for open-source datasets, such as lithography hotspot libraries and post-silicon validation logs, along with standardized metrics to promote reproducibility. Initiatives like MAGICAL, an open-source analog layout engine, illustrate this trend [10].

4 Conclusion

The integration of AI into digital integrated circuit design automation marks a significant advancement in electronics engineering. This paper have explored the development and application of digital integrated circuit design automation, and focus on digital integrated circuit design automation based on artificial intelligence, including how AI technologies are revolutionizing the design process, enhancing efficiency, accuracy, and innovation. Several key points emerge from this paper discussion.

First, EDA is expected to advance due to the quick development of machine learning. It could encourage innovation in EDA physical design and enhance almost every step of the EDA chip design process. Nonetheless, there are challenges in effectively applying ML-based EDA to handle and interpret complex legacy data sets from older EDA systems. Second, LCM leverages deep learning to capture complex dependencies and characteristics of large-scale circuit network tables. This enables more accurate and innovative design strategies. But there are still many research issues with LCM, like improving representation learning methods to fit the distinct circuit properties at every design step and creating scalable and efficient alignment models. Then, AI-driven tools such as ShortCircuit showcase the potential for automating schematic generation, layout optimization, and predictive failure analysis. These features significantly reduce the time and effort of traditional manual design processes. For example, AI algorithms can quickly generate initial schematics based on specifications. They can also optimize layouts by accounting for various constraints, leading to more compact and efficient circuits. Looking ahead, the future of AI in circuit design presents considerable opportunities for advancement. AI-driven co-design systems and generative design methods will allow engineers to concentrate on high-level innovations while AI manages complex technical details. The potential for autonomous design validation, where AI independently verifies circuit designs across various scenarios, will further speed up the design process.

In conclusion, embracing AI in digital integrated circuit design automation offers substantial benefits, including accelerated time-to-market, reduced costs, and enhanced product reliability. As AI technologies continue to evolve, their role in circuit design will become increasingly indispensable, paving the way for unprecedented innovation in the electronics industry.

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