Research on Read Circuits for Wide-temperature STT-MRAM

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Abstract. STT-MRAM is considered one of the most promising candidates for emerging memory, sense amplifier and next-generation memory. Temperature greatly affects MRAM performance: reading becomes difficult at high temperatures, and writing becomes hard at low temperatures. This article analyzes in detail the impact of temperature on STT-MRAM and explores read circuits optimized for wide temperature ranges.

Keywords: STT-MRAM , WIDE-TEMPERATURE, HIGH SENSING MARGIIN

1 Introduction

In recent years, memory has rapidly advanced because of the information age, where most information needs to be stored.Memory also serves as a foundational element in computer system design, profoundly influencing three key performance metrics: computational efficiency, hardware compactness, and energy utilization patterns. Modern computer systems use different types of memory, such as SRAM, DRAM, and NAND Flash. Each has its own strengths and weaknesses. SRAM is very fast in reading and writing, so it is often used in CPU coaches. However, it has low storage density and takes up a lot of chip space. Also, SRAM needs constant power to keep data. When the power supply is interrupted, the data will be erased. In addition, the leakage current of CMOS transistors increases as the process size decreases. Therefore, SRAM has relatively high-power consumption. DRAM is cheaper than SRAM and has higher storage density, so it is widely used as main memory. But it has a big problem: it must refresh data regularly, or the data will disappear. This not only increases power consumption but also makes it less suitable for low-power applications. NAND Flash is non-volatile memory, commonly used in USB drives and SSDs. It has high storage density and low cost, but its writing speed is slow. Another issue is that it can only be written a limited number of times, usually between tens of thousands to hundreds of thousands. Sayeef Salahuddin [1] demonstrates that Spin Transfer Torque Magnetic Random Access Memory (STT-MRAM) performs well in critical metrics including access speed, storage density, endurance, and energy

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A. J. Moshayedi (ed.), *Proceedings of the 2025 2nd International Conference on Electrical Engineering and Intelligent Control (EEIC 2025)*, Advances in Engineering Research 279,
https://doi.org/10.2991/978-94-6463-864-6_30

efficiency. This makes it a mainstream alternative to traditional volatile memory technologies, particularly suitable for non-volatile cache and main memory architecture designs.

But STT-MRAM is very easy to be affected by temperature. Temperature changes the intrinsic properties of ferromagnetic materials and affects the conductive characteristics of the tunnel barrier. It also introduces thermal noise and random disturbances. This affection will cause instability in the MTJ's electrical characteristics and then changes the memory's function. For example, STT - MRAM is difficult to write at low temperatures, but it's easy to write at high temperatures. If traditional writing pulses are used, it will lead to wasted writing power consumption at high temperatures. Also, it's difficult to read at high temperatures. To reduce temperature induced instability, more researchers are now using wide-temperature MRAM to minimize temperature effects on MRAM performance. This paper investigates the effects of temperature on magnetic tunnel junction (MTJ) devices and proposes circuit solutions. The article begins with an explanation of basic MTJ operation, including its structure and functionality. Subsequently, changes in MTJ performance with temperature are examined, focusing on thermal stability and TMR ratio variations. Finally, read circuit designs suitable for high-temperature operation are presented.

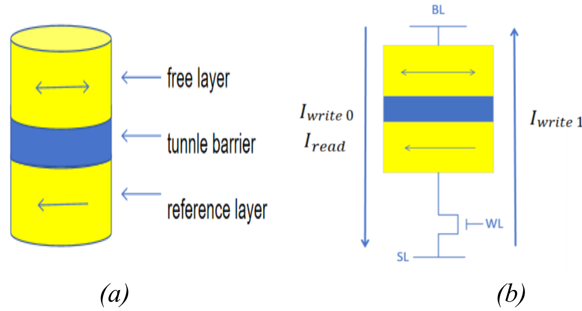
2 The basics of MTJ

2.1 Structure and Principle of the MTJ

The fundamental storage unit in STT - MRAM consists of two crucial parts. One is the spin transfer torque magnetic tunnel junction (STT - MTJ), which functions as the memory component. The other is the select transistor that controls access to the storage unit.Researchers usually refer to this structure as 1T1M（One Transistor One MTJ). The MTJ is the main part of MRAM. Two ferromagnetic layers are separated by a thin insulating layer (e.g., magnesium oxide, MgO) to form it (Fig. 1(a)). One ferromagnetic layer functions as the reference layer, the direction of its magnetization is firmly set along the easy axis. As for the other layer, it is called the free layer. The free layer's magnetization direction is not fixed but rather alterable. To store data, one ferromagnetic layer's magnetic direction (parallel or antiparallel) is changed compared to the other layer. This represents "0" or "1" [2]. The tunneling magnetoresistance (TMR) effect is employed for data reading. Specifically, in a MTJ, the resistance shifts between a high - resistance state and a low - resistance state. This shift is determined by the relative magnetization directions of the two ferromagnetic layers. The resistance difference of MTJ is typically Featured with TMR [3].

$$TMR = \frac{R_{AP} - R_P}{R_P} \quad (1)$$

For the purpose of writing and reading data bits, the read - write circuit applies voltages to the bit line (BL) and source line (SL). Meanwhile, transistors control the current passing through BL and SL (Fig. 1(b)).



(a) *(b)*

Fig. 1. (a) Main construction of MTJ, (b) Read and Write Methods of STT-MRAM.[4]

3 The effect of temperature on MTJ devices

Temperature will affect various factors such as TMR or *Critical Current Ic0* [5]. The following will explain how temperature affects different parameters of MTJ.

3.1 The Temperature Dependence of TMR

V. Drewello studies how temperature affects the TMR in MTJs through experiments and theoretical modeling [6]. The results show that the TMR ratio decreases significantly as temperature rises. This change is mainly caused by the strong temperature dependence of the resistance in the antiparallel (AP) state, while the parallel (P) state resistance changes very little [6].

Two key mechanisms explain this behavior. One is Magnon Excitation Effect, Higher temperatures increase the number of interfaces magnons, which leads to more spin-flip tunneling electrons. This greatly increases the AP state conductance and reduces TMR. A modified magnon model (with a low-energy cutoff (Ec)) [7] successfully describes this process.

The other one is Thermal Broadening Effect. The widening of electron energy distribution near the Fermi level reduces the effective barrier height. This slightly increases the P state conductance (~1.8%–4.7%). This intrinsic effect cannot be ignored in high-TMR junctions [6].

Y. Wang developed a complete TMR model [5].

$$TMR(V,T) = TMR(T) \times (1 + \frac{V^2}{V_H^2})^{-1} \tag{2}$$

3.2 Thermal Stability Factor's Response to Temperature Changes

As the temperature goes up, both the anisotropy field H_K and the saturation magnetization $M_S$decline. Δ can be calculated by using these formulas:

$$\Delta = \frac{E}{k_B T} \tag{3}$$

$$E = \frac{\mu_0 M_s \times H_K \times V}{2} \tag{4}$$

As these formulas, the temperature will affect H_K and M_s, thus indirectly affecting Δ. The higher the temperature is, the lower Δ is, thus leading to read duration and the read current decrease [5].

3.3 The Temperature Dependence of the Critical Current Ic0

When the temperature increases, the energy barrier in magnetic tunnel junctions decreases. This causes two main effects. First, the critical current becomes smaller. This makes switching easier. Second, the risk of accidental switching increases [5]. Research shows the critical current I_{co}directly relates to Δ. Specifically, a larger Δ requires a larger critical current I0 [8]. This relationship can be expressed as:

$$I_0 = \frac{\alpha}{\eta}\frac{2e}{\hbar}2\Delta K_B T \tag{5}$$

When temperature rises, both the saturation magnetizati-on M_s and the effective an isotropy H_K decrease [5]. The reduc-tion of M_s and H_K will cause I0 to decrease, this will reduce the difficulty of the MTJ write operation.

3.4 The temperature dependence of the switching delay τ

When $I > I_c$,τ can be calculated by using these formulas:[9].

$$\frac{1}{\tau} = [\frac{2}{C + \ln(\frac{\pi^2\Delta}{4})}]\frac{\mu_B P_{ref}}{em(1 + P_{ref}P_{free})}(I - I_c) \tag{6}$$

This formula shows that $\tau \propto (I - I_C)^{-1}$and pronounced temperature sensitivity.

When I< I_c,τ can be calculated by using these formulas: [10].

$$\tau = \tau_0 \exp(\Delta(1 - \frac{I}{I_c})) \tag{7}$$

Where τ_0 is the attempt time. τ is primarily determined by thermal activation and decreases exponentially with increasing temperature.

4 Summary of Readout Circuit Designs for High-Temperature Operation

At the International Solid-State Circuits Conference (ISSCC) in 2018, University of Michigan proposed an innovative single-capacitor offset-cancellation sense amplifier [11]. This circuit (see Fig.2) can eliminate voltage offset and it has only one capacitor, so the area overhead is small. It has a high sensing margin at high temperatures.

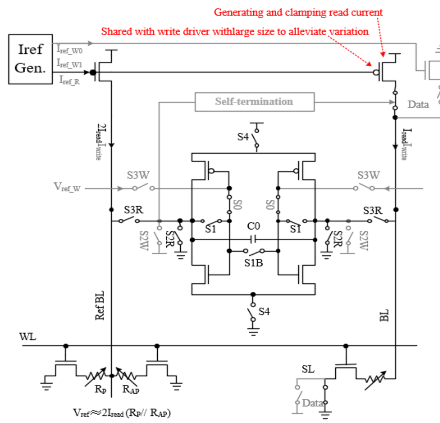


Fig. 2. The structure of the single-capacitor offset-cancellation sense amplifie [11].

At ISSCC in 2019, Intel proposed a Read Sensing circuit [12]. This Read Sensing circuit (see Fig.3) can suppress voltage offset and has double sensing margins structure. It can perform feedback. So it has a high sensing margin and can still maintain a high read accuracy at high temperatures.

At the ISSCC in 2022, National Tsing Hua University proposed a charge-recycling voltage sense amplifier (CR-VSA) [13]. This circuit (see Fig.4) can recover charge, suppress offset voltage, and provide feedback, so it has a high sensing margin at high temperatures. At the same time, It can read during both the charging and discharging phases, reducing power consumption.

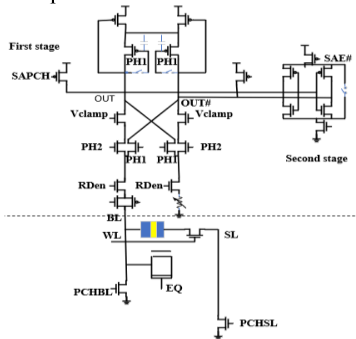


Fig. 3. Schematic of the Read Sensing circuit [12].

Fig. 4. The structure of the charge-recycling voltage sense amplifier [13].

At the ISSCC in 2018, National Tsing Hua University proposed a Continuous Record Enhancement - Voltage Sense Amplifier (CRE-VSA) [14]. As depicted in Figure 5, the proposed circuit incorporates a feedback architecture. Through this design, it effectively mitigates the offset voltage issue and enhancing its operational stability. The circuit also demonstrates remarkable energy-efficiency, characterized by low read voltage power consumption. Such attributes render it particularly well-suited for application in read circuits operating under elevated temperature conditions.

Fig. 5. The structure of the CRE-VS [14].

At the IEEE Journal of Solid-State Circuits (JSSC) in 2017, Yonsei University proposed this offset canceling current-sampling sense amplifier (OCCS-SA) [15]. Shown in (see Fig.6(a)), the circuit's double sensing margin structure, along with its feedback and offset voltage cancellation functions, serves to augment the sensing margin of the sensing circuit. This makes it suitable for data - reading operations in high - temperature environments.

At the ISSCC in 2023, Taiwan Semiconductor Manufacturing Company (TSMC) proposed a Merged reference sense amplifier [16] .This circuit (see Fig.6(b)) calculates the mean value of 36 MTJs. The default ratio of R_P to R_{AP} is set to 1:1, and the reference current is established as the average of I_P and I_{AP}. This approach enables the tracking of variations in MTJ processes and temperature fluctuations.

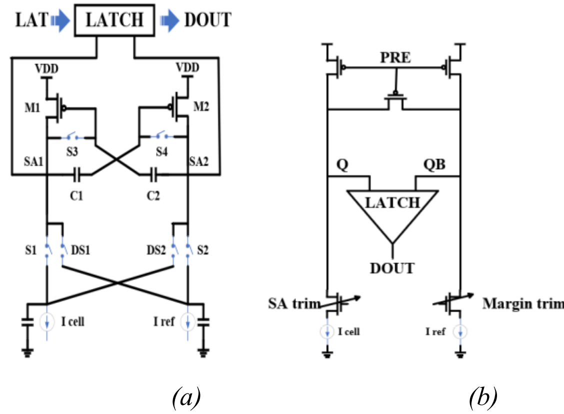


Fig. 6. (a) The schematic of the OCCS-SA [15], (b) The structure of the Merged reference sense amplifier [16].

At the IEEE Transactions on Nanotechnology in 2018, Southern University of Science and Technology proposed a Thermal-Aware Sensing Amplifier (TASA) [17]. An MTJ in the antiparallel state and an NMOS transistor are used to form the TAC. As the temperature changes, the MTJ and the NMOS transistor show opposite thermal properties. This allows the TAC to generate an output voltage that changes with the temperature. In TASA (see Fig.7), The gate voltage of the clamp transistors Nc0 and Nc1 in the PCSA is adjusted using the Vout from the TAC. In the reading process, When the temperature rises and the currents within the PCSA decreases, Vout will carry out automatic compensation for these decreased currents. For example, in the read "0" operation, even when the temperature is high, TASA is able to keep a sensing margin comparable to the one at room temperature.

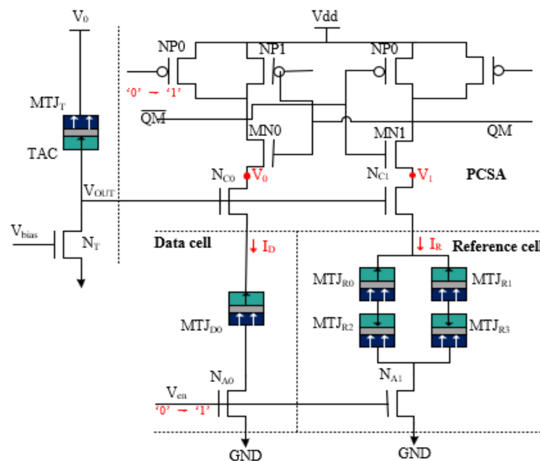


Fig. 7. The structure of the TASA circuit [17].

At the IEEE Transactions on Reliability in 2016, Nanjing University of Aeronautics and Astronautics proposed a Body biased sensing circuit [18] (see Fig.8). In order to deal with the concern of read reliability amidst temperature changes, the body biasing technique has been introduced. Body-biasing techniques work by adjusting the body voltage of the upper-level PMOS transistors. This adjustment can dynamically enhance or reduce the threshold voltage and driving capabilities of these transistors. This approach is used to expand the voltage gap between the data sensing channel and the reference channel, thereby boosting the read margin.

Southeast University proposed a high sensing margin sensing amplifier (HSM-SA) in 2023 [19]. The circuit (see Fig.9) adopts a two-step sensing method. It can eliminate the offset voltage and increase the margin. Its two-stage latch structure also cancels voltage offset and at the same time provides feedback. Then enlarge the sensing margin.

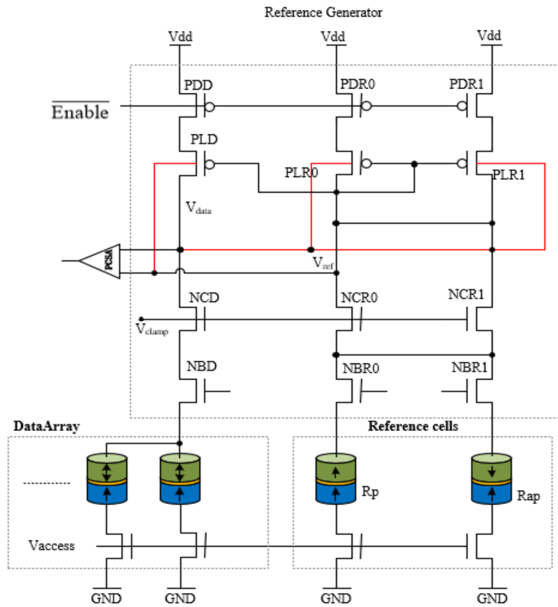


Fig. 8. The structure of the Body biased sensing circuit [18].

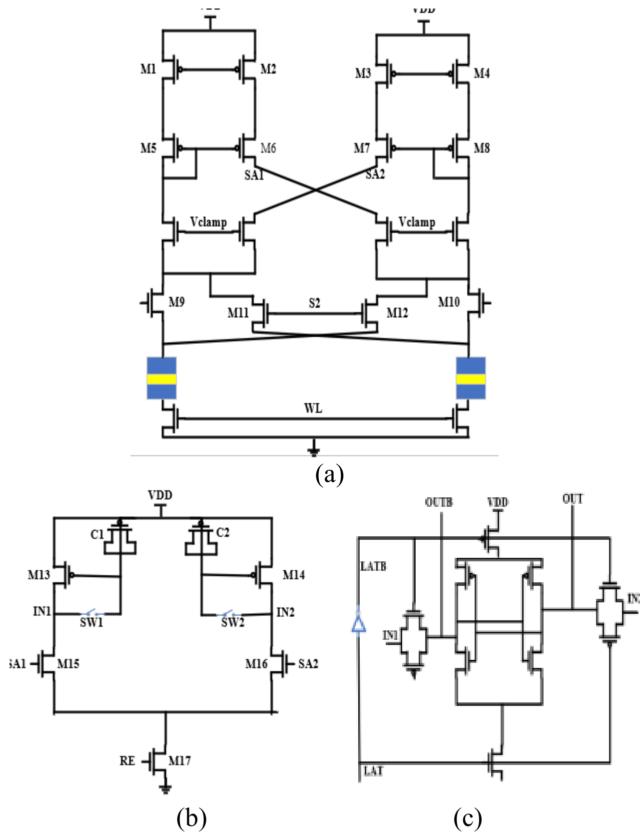


Fig. 9. The structure of the suggested HSM - SA [19]: (a) The sensing circuit contains two sensing stages. (b) The voltage sampling and amplifying circuit. (c) The voltage latched sense amplifier.

In 2018, during the IEEE Asia Pacific Conference on Circuits and Systems, Southeast University put forward a sensing block featuring high margin, speed, and stability (HMSS) [20]. This circuit(see Fig.10) has two reference structures. These structures increase the sensing margin. This makes the circuit read data more accurately at high temperatures.

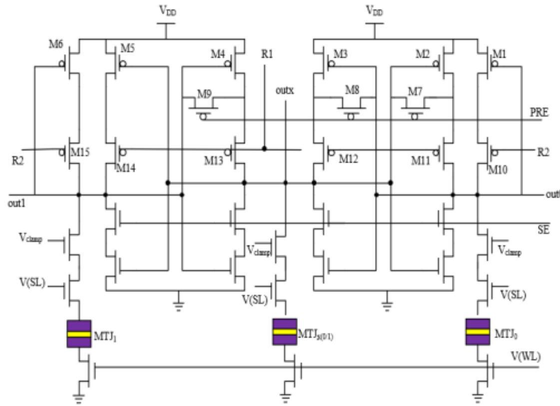


Fig. 10. The structure of the HMSS circuit [20].

At the IEEE Transactions on Very Large Scale Integration (TVLSI) Systems, Radboud University Nijmegen proposed a offset-compensated high-speed sense amplifier (OCHS-SA) [21]. This circuit (see Fig.11) can perform voltage offset compensation. It uses a feedback structure and this makes the circuit's sensing margin larger.

At the IEEE Transactions on Magnetics, Southeast University proposed a novel triple-current margin sensing amplifier (TM-SA) [22]. This circuit (see Fig.12) can suppress offset voltage and provides feedback. This achieves three times the sensing margin.

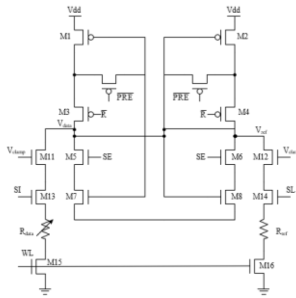


Fig. 11. The structure of the OCHS-SA circuit [21].

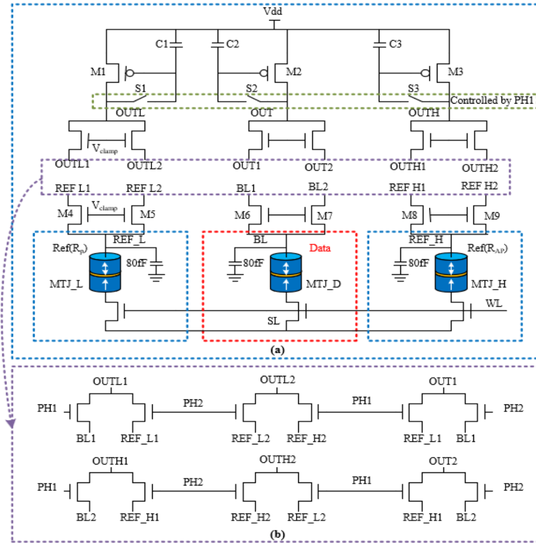


Fig. 12. The structure of the TM-SA circuit [22].

Korea University proposed an offset-canceling sensing scheme using feedback in 2021 [23]. As depicted in Fig.13, this circuit gets rid of the offset voltage by utilizing two capacitors. It also employs positive feedback to quicken the rate of change of the bit-line voltage. As a result, both the sensing margin and read speed are improved.

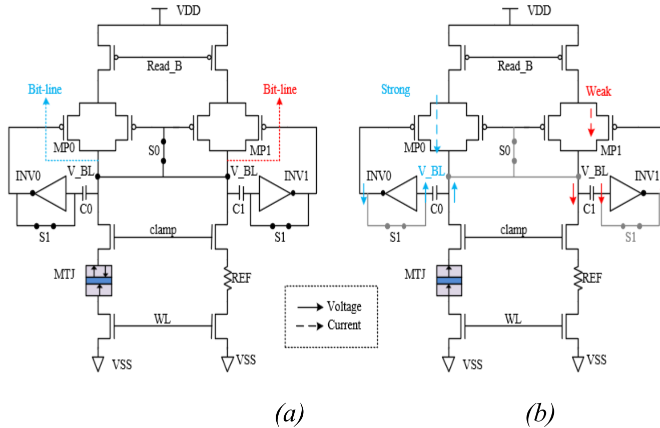


Fig. 13. Sensing Scheme for Offset Cancellation [23]. (a) Equalization Phase. (b) Sensing Phase.

At the International Conference on ASIC (ASICON) in 2021, Southeast University proposed an self-regulating dynamic reference (SRDR) sensing scheme [24]. This circuit mainly improves the sensing margin through a pre-charged feedback sense amplifier and a self-regulating dynamic reference generator (Figure 14).

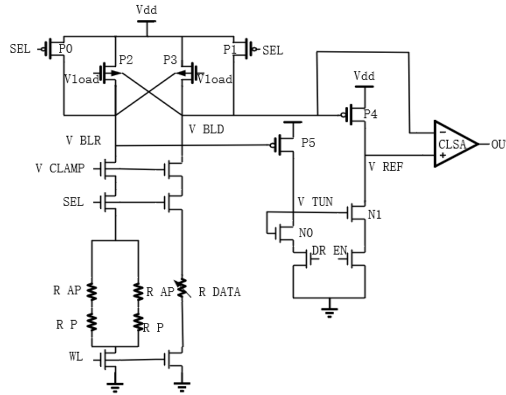


Fig. 14. The structure of the SRDR circuit [24].

At the IEEE International Symposium on Circuits and Systems (ISCAS) in 2018, Radboud University Nijmegen proposed a new sensing circuit suitable for FinFET technology [25]. This circuit (see Fig.15) has two operating stages, namely the pre-charging stage and the evolution stage. It also has a strong positive feedback. These features significantly increase the sensing margin.

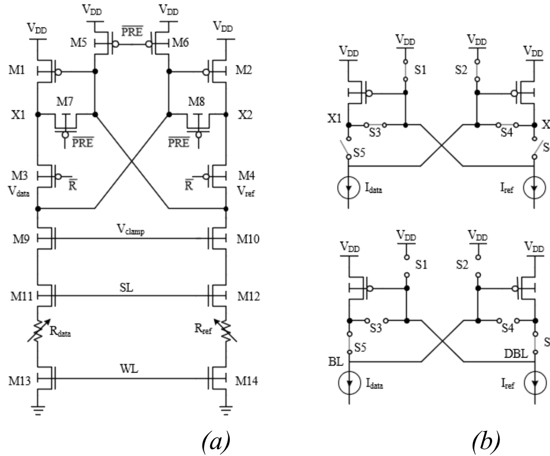


Fig. 15. (a) Sketch of the proposed approach. (b) Pre-charge phase and development phase [25].

5 Conclusion

In conclusion, STT-MRAM is a promising memory technology, but its performance is significantly affected by temperature. High temperatures make reading difficult, while low temperatures hinder writing. Temperature influences the properties of MTJs, such as the TMR ratio, thermal stability factor, critical current, and switching delay. To

address these issues, various read circuits suitable for wide temperature ranges have been developed. For example, some circuits use offset cancellation and feedback structures to improve sensing margins. Others adopt charge recycling or dynamic reference generation to enhance stability and reduce power consumption. These designs demonstrate that appropriate circuit solutions can effectively mitigate the impact of temperature on STT-MRAM, improving its reliability and performance across different temperature conditions. Further research in this area will be crucial for advancing the practical application of STT-MRAM in diverse environments.

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